IMPACT OF MOSFET GATE-OXIDE RELIABILITY ON CMOS OPERATIONAL AMPLIFIERS IN A 130-nm LOW-VOLTAGE CMOS PROCESS

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ABSTRACT

The effects of the gate-oxide reliability of MOSFETs on operational amplifiers were investigated with the two-stage and folded-cascode structures in a 130-nm low-voltage CMOS process. The tested operating conditions include unity-gain buffer (close-loop configuration) and comparator (open-loop configuration) under different input frequencies and signals. After overstress, the small-signal parameters, such as small-signal gain, unity-gain frequency, and phase margin, were measured to verify the impact of gate-oxide reliability on circuit performances of the operational amplifier. The gate-oxide reliability can be improved by the stacked configuration in the operational amplifier with folded-cascode structure. A simple equivalent device model of gate-oxide reliability for CMOS devices in analog circuits was investigated and simulated.

INTRODUCTION

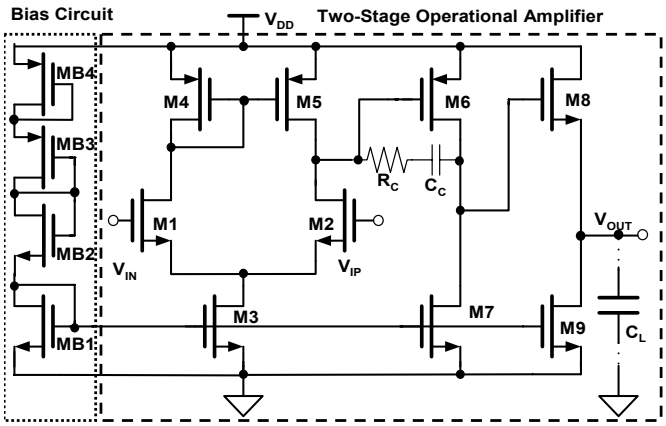
The occurrence of gate-oxide breakdown during the lifetime of CMOS circuits cannot be completely ruled out. The exact extrapolation of time-to-breakdown at circuit operating conditions is still difficult, since the physical mechanism governing the MOSFET gate dielectric breakdown is not yet fully modeled. It was less of a problem for older CMOS technologies, which have the thick gate oxide. However, because the probability of gate-oxide reliability strongly increases with the decrease of gate-oxide thickness [1], the CMOS circuits in nano-scale technologies could be insufficiently reliable.

The defect generation leading to gate-oxide breakdown and the nature of the conduction after gate-oxide breakdown has been investigated [1]-[9]. Recently, some studies on the impact of MOSFET gate-oxide breakdown on circuits have been reported [2]-[9]. In [2], it was demonstrated that the digital circuits would remain functional beyond the first gate-oxide hard breakdown. A soft gate-oxide breakdown event in the dynamic CMOS digital circuits relying on the uncorrected soft nodes may result in the failure of the circuit [3]. The gate-oxide breakdown on RF circuits was also studied [4]. Some designs of analog circuits [10], [11] and the mixed-voltage I/O interface [12] indicate that gate-oxide reliability is a very import design consideration in CMOS circuits. However, the impact of MOSFET gate-oxide breakdown on the CMOS analog circuits is still not well studied. The CMOS analog circuits are sensitive to the small-signal parameters of MOSFET. Therefore, the gate-oxide breakdown is expected to have severe impact on the circuit performances of analog circuits, such as transconductance (g_m), output resistance (r_o), threshold voltage (V_{th}), and phase margin.

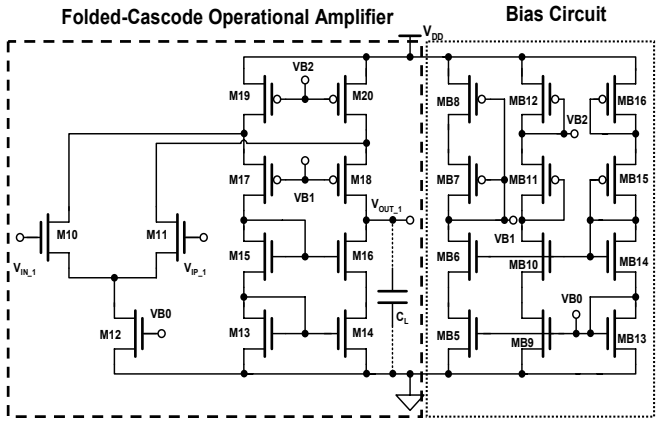
In this work, the effect of MOSFET gate-oxide reliability on the operational amplifiers with the folded-cascode (stacked) and two-stage (non-stacked) structures was investigated in a 130-nm low-voltage CMOS process. The small-signal gain, phase margin, unity-gain frequency, and power supply rejection ratio (*PSRR*) of these operational amplifiers with different configurations were measured and compared after different stresses.

ANALOG CIRCUITS

The operational amplifier is a basic unit in many analog circuits and systems, such as output buffer, sample-and-hold circuit, and analog-to-digital converter. The operational amplifiers with the two-stage and folded-cascode structures were selected to verify the impact of MOSFET gate-oxide reliability on analog circuits. The complete circuits of the operational amplifiers are shown in Figs. 1(a) and 1(b). The normal operating voltage and the gate-oxide thickness (t_{ox}) of all MOSFET devices in these two operational amplifiers are 1 V and 2.5 nm, respectively, in a 130-nm low-voltage CMOS process.



(a)



(b)

FIGURE 1. THE COMPLETE CIRCUITS OF THE OPERATIONAL AMPLIFIERS WITH THE (a) TWO-STAGE, AND (b) FOLDED-CASCODE, CIRCUIT STRUCTURES.

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IEEE 05CH37616 43rd Annual International Reliability Physics Symposium, San Jose, 2005

The digital circuits are usually designed to work with high-speed operation and low-power consumption in the small chip area. The MOSFET with the minimum channel length is usually used to realize the digital circuits. However, the MOSFET with the minimum channel length in the nanoscale CMOS processes has many issues, such as threshold variation, drain-induced barrier lowering (DIBL) effect, hot-carrier effect, velocity saturation, and mobility degradation effect. The performances of CMOS analog circuits will be degraded by those non-ideal effects of MOSFET in the nanoscale processes. Therefore, the MOSFET with the minimum channel length is seldom used to design CMOS analog circuits. The device channel length of 0.5 μm or 1 μm in a 130-nm low-voltage CMOS process is used to draw the MOSFET in the operational amplifiers.

If the critical terminal voltage of the device is kept within the normal operating voltage V_{DD} of the technology, the electric fields across the device will not over stress the device. Therefore, the bias circuit of the operational amplifiers is designed with stacked structure to avoid the gate-oxide reliability. The capacitance C_C of the two-stage operational amplifier in Fig. 1(a) is realized by the metal-insulator-metal (MIM) structure which has no gate-oxide reliability problem. The bulk terminals of the PMOS and NMOS of the operational amplifiers are connected to V_{DD} and GND, respectively. The impact of MOSFET gate-oxide reliability on the operational amplifiers is verified by using continuous stress with supply voltage of 2.5 V. The common-mode voltage of the operational amplifiers was set to 1.25 V. Simulated by HSPICE, the open-loop gain and phase margin of the two-stage operational amplifier are 64.7 dB and 47.8 degree, respectively, under output capacitance load of 10 pF. The open-loop gain and phase margin of the folded-cascode operational amplifier are 61.9 dB and 89 degree, respectively, under output capacitance load of 10 pF. The small-signal gain (A_V) and dominant pole (ω_{pole}) of the operational amplifiers are given by

$$A_{V\_two-stage} \cong -g_{m2}g_{m6}g_{m8}(r_{O5} // r_{O2})(r_{O6} // r_{O7})(r_{O8} // r_{O9}), \quad (1)$$

$$\omega_{pole\_two-stage} \cong \frac{1}{C_L(r_{O8} // r_{O9})}, \quad (2)$$

$$A_{V\_folded-cascode} \cong -g_{m11}\left[(r_{O20} + r_{O18}) // (r_{O16} + r_{O14})\right], \text{and} \quad (3)$$

$$\omega_{pole\_folded-cascode} \cong \frac{1}{C_L\left[(r_{O20} + r_{O18}) // (r_{O16} + r_{O14})\right]}. \quad (4)$$

The short-channel effect and body effect of MOSFETs are ignored in these equations (1), (2), (3) and (4). The g_m and r_o are the transconductance and small-signal output resistance of the corresponding MOSFET in the operational amplifiers. The C_L is the output capacitance load of the operational amplifiers, which was set to 10 pF in simulation.

OVERSTRESS TEST

The operational amplifiers with the close-loop (unity-gain buffer) and open-loop (comparator) structures are selected to verify the impact of MOSFET gate-oxide reliability on the circuit performances of the operational amplifiers in a 130-nm low-voltage CMOS process. The small-signal gain, phase margin, output-signal swing, *PSRR*, and rise and fall times of the operational amplifiers varied with gate-oxide breakdown will be measured and analyzed. Because the MOSFET devices in analog circuits usually work in the saturation region, the gate-oxide breakdown is more likely to occur as the conventional time-dependent dielectric breakdown (TDDB). High gate-to-source voltage (V_{GS}), gate-to-drain voltage (V_{GD}), and drain-to-source voltage (V_{DS}) of the MOSFET are used to get a fast and easy-to-observe breakdown occurrence for investigating the impact of the gate-oxide reliability on the operational amplifiers. The advantages of using static stress are the well-defined distributions of the voltages on the devices in the operational amplifiers and the better understanding of the consequences of this overstress. After overstress, the small-signal parameters of the operational amplifiers are re-evaluated under the same operating condition.

A. Unity-Gain Buffer (DC Stress)

The output node of the operational amplifiers was connected to the inverting input node to form the configuration of a unity-gain buffer. The non-inverting node of the operational amplifiers was biased at 1.25 V, the output capacitance load was set to 10 pF, and the supply voltage V_{DD} was set to 2.5 V. The operational amplifiers under the configuration of the unity-gain buffer are continuously tested in this DC overstress, as shown in Fig. 2. The measured results of the fresh frequency responses before any stress are shown in Figs. 3(a) and 3(b), where the operational amplifiers operate in the unity-gain buffer. The small-signal gain, unity-gain frequency, and phase margin of the operational amplifier with the two-stage structure are 0.48 dB, 2.3 MHz, and 168 degree, respectively, under output capacitance load of 10 pF. Those of the operational amplifier with the folded-cascode structure are -0.4 dB, 1 MHz, and 163 degree, respectively, under output capacitance load of 10 pF.

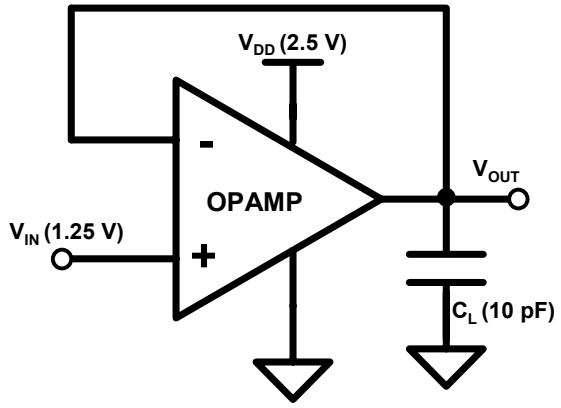
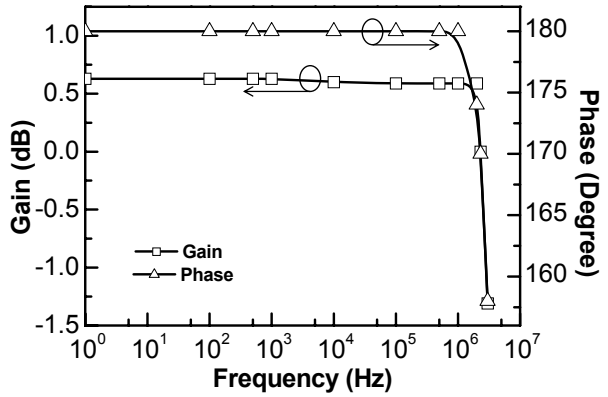


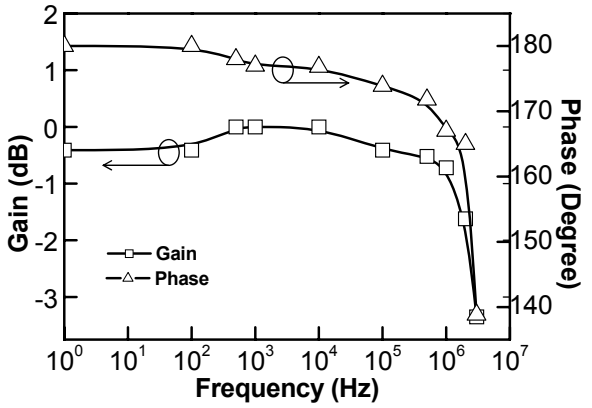
FIGURE 2. THE UNITY-GAIN BUFFER CONFIGURATION FOR OPERATIONAL AMPLIFIERS UNDER DC STRESS TO INVESTIGATE THE IMPACT OF GATE-OXIDE RELIABILIITY ON CIRCUIT PERFORMANCES.

During this DC overstress, the small-signal gain, unity-gain frequency, phase margin, offset voltage, *PSRR*, and rise and fall times of the operational amplifiers operating in the unity-gain buffer configuration will be measured. When those parameters are measured, the input signal of 1.25 V at the non-inverting node (V_{IN}) is replaced by the AC small signal (100-mV sine wave) at the input pin with a common-mode voltage of 1.25 V. About the measurement setup for power supply rejection ratio (*PSRR*), a sinusoidal ripple of 100 mV is added to the power supply to measure the small-signal gain between the supply voltage and output pin voltage (V_{OUT}). The AC input signal at the power supply pin must include a DC bias that corresponds to the normal power supply voltage (2.5 V), so that the operational amplifiers operating in the unity-gain buffer remains powered up. The offset voltage of operational amplifiers operating in the unity-gain buffer can be measured from the voltage difference between the inverting and non-inverting nodes of the operational

amplifiers, when the input pin (V_{IN}) was set to common-mode voltage of 1.25 V. About the measurement setup for rise and fall times of the operational amplifiers operating in the unity-gain buffer, the square voltage waveform from 1 to 1.5 V is applied to the input pin to measure the rise and fall times of the signal at output pin. The rise and fall times were defined as the times of the output signal rise and fall edges from 10 % to 90 %, when the square waveform of input signal has the rise and fall times of 1 ns.



(a)



(b)

FIGURE 3. THE FRESH FREQUENCY RESPONSES OF THE OPERATIONAL AMPLIFIERS WITH THE (a) TWO-STAGE, AND (b) FOLDED-CASCODE, STRUCTURES OPERATING IN THE UNITY-GAIN BUFFER.

The dependence of the small-signal gain on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Fig. 4. The small-signal gain of the operational amplifiers with the two-stage and folded-cascode structures under the DC stress is not changed; even through the stress time is up to 4000 minutes. The dependence of the unity-gain frequency on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Fig. 5. The unity-gain frequency of the operational amplifier with the two-stage structure under the DC stress is decreased, but that of the operational amplifier with folded-cascode structure is not obviously changed under the same condition. The dependence of the phase margin on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Fig. 6. The phase margin of the operational amplifier with the two-stage structure under the DC stress is decreased, but that of the operational amplifier with folded-cascode structure is not obviously changed. The dependence of the offset voltage on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Fig. 7. The offset voltage of the operational amplifier with the two-stage structure under the DC stress is increased, but that of the operational amplifier with folded-cascode structure is not changed. The dependence of the output-voltage swing on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Fig. 8. The output-voltage swing of the operational amplifier with the two-stage structure under the DC stress is decreased, but that of the operational amplifier with folded- cascode structure is not changed. The dependence of the rise and fall times on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Figs. 9(a), 9(b), and 9(c). The rise and fall times of the operational amplifier with the two-stage structure under the DC stress is obviously changed, but that of the operational amplifier with folded-cascode structure is not changed. The dependence of the *PSRR* on the stress time of the operational amplifiers with the two-stage or folded-cascode structures operating in the unity-gain buffer under the DC stress is shown in Fig. 10. The *PSRR* of the operational amplifier with the two-stage structure under the DC stress is obviously changed, but that of the operational amplifier with folded-cascode structure is not changed. The detailed discussions on these results will be shown in the next section.

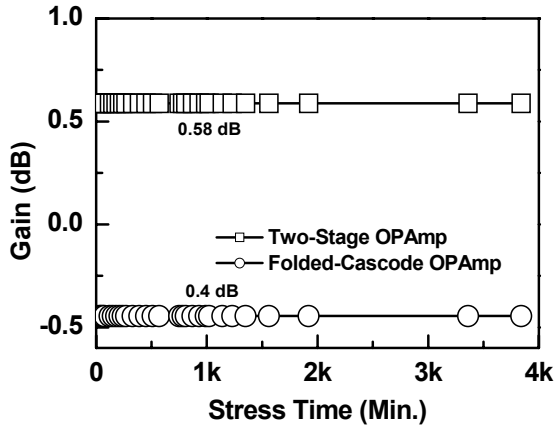


FIGURE 4. THE DEPENDENCE OF THE SMALL-SIGNAL GAIN ON THE STRESS TIME OF THE OPERATIONAL AMPLIFIERS WITH THE TWO-STAGE OR FOLDED-CASCODE STRUCTURES OPERATING IN THE UNITY-GAIN BUFFER UNDER THE DC STRESS.

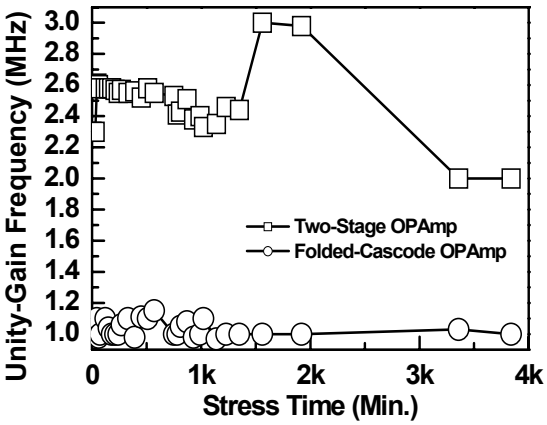


FIGURE 5. THE DEPENDENCE OF THE UNITY-GAIN FREQUENCY ON THE STRESS TIME OF THE OPERATIONAL AMPLIFIERS WITH THE TWO-STAGE OR FOLDED-CASCODE STRUCTURES OPERATING IN THE UNITY-GAIN BUFFER UNDER THE DC STRESS.

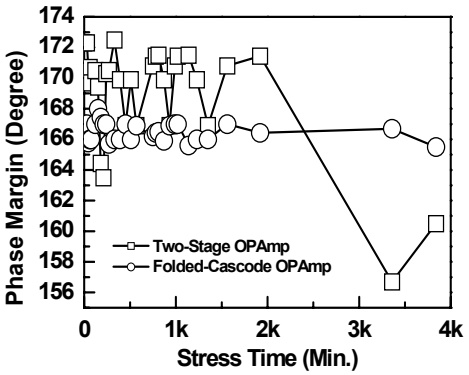


FIGURE 6. THE DEPENDENCE OF THE PHASE MARGIN ON THE STRESS TIME OF THE OPERATIONAL AMPLIFIERS WITH THE TWO-STAGE OR FOLDED-CASCODE STRUCTURES OPERATING IN THE UNITY-GAIN BUFFER UNDER THE DC STRESS.

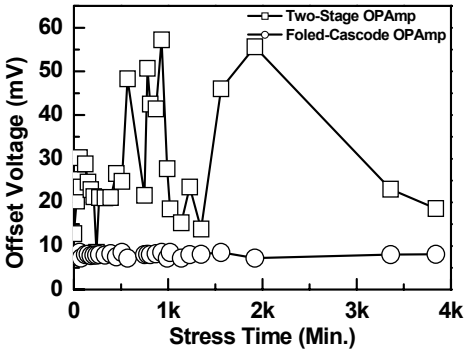


FIGURE 7. THE DEPENDENCE OF THE OFFSET VOLTAGE ON THE STRESS TIME OF THE OPERATIONAL AMPLIFIERS WITH THE TWO-STAGE OR FOLDED-CASCODE STRUCTURES OPERATING IN THE UNITY-GAIN BUFFER UNDER THE DC STRESS.

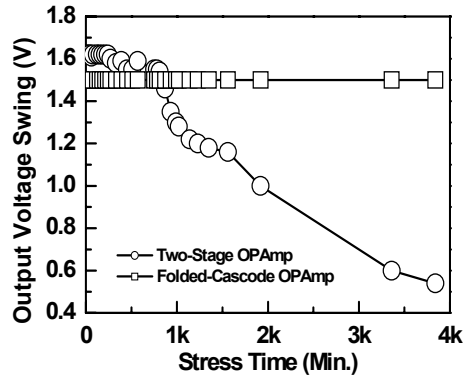
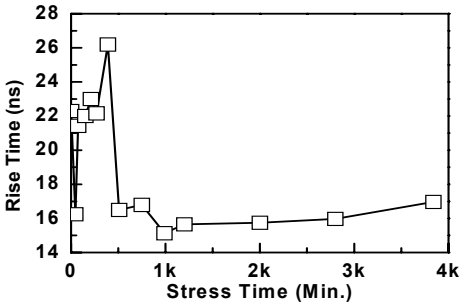
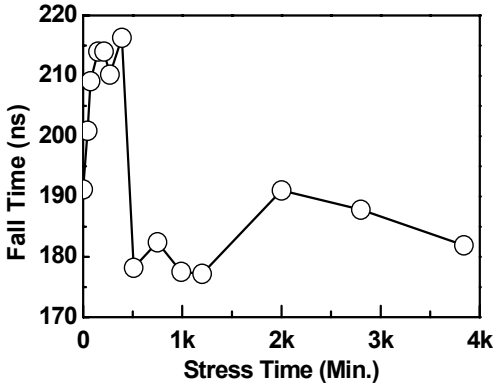


FIGURE 8. THE DEPENDENCE OF THE OUTPUT-VOLTAGE SWING ON THE STRESS TIME OF THE OPERATIONAL AMPLIFIERS WITH THE TWO-STAGE OR FOLDED-CASCODE STRUCTURES OPERATING IN THE UNITY-GAIN BUFFER UNDER THE DC STRESS.



(a)



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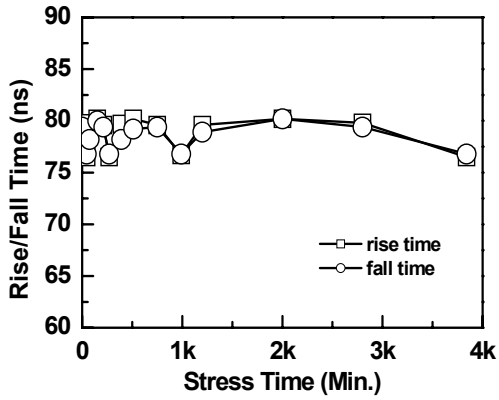


(c)

FIGURE 9. THE DEPENDENCE OF THE RISE AND FALL TIMES ON THE STRESS TIME OF THE OPERATIONAL AMPLIFIERS WITH THE (a) AND (b) TWO-STAGE OR (c) FOLDED-CASCODE STRUCTURES OPERATING IN THE UNITY-GAIN BUFFER UNDER THE DC STRESS.

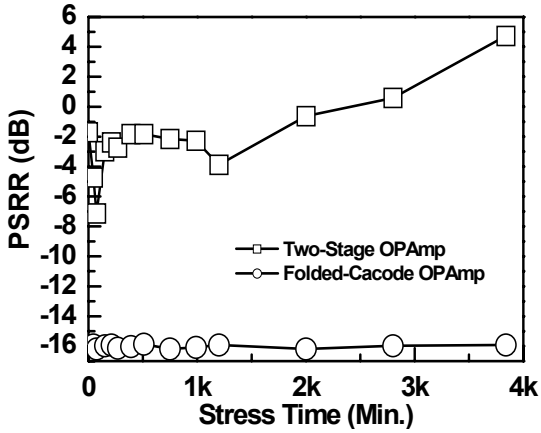


FIGURE 10. THE DEPENDENCE OF THE *PSRR* ON THE STRESS TIME OF THE OPERATIONAL AMPLIFIERS WITH THE TWO-STAGE OR FOLDED-CASCODE STRUCTURES OPERATING IN THE UNITY-GAIN BUFFER UNDER THE DC STRESS.

B. Unity-Gain Buffer (AC Stress With DC Offset)

The operational amplifiers under the configuration of the unity-gain buffer are continuously tested in the stress of the AC small-signal input with DC offset, as shown in Fig. 11. The non-inverting node of the operational amplifiers with the two-stage and folded-cascode structures was biased by the AC small-signal input (500-mV sine wave with different frequencies of 100 Hz, 500 kHz, and 1 MHz) with DC offset voltage (1.25 V). The output

capacitance load was set to 10 pF, and the supply voltage V_{DD} was set to 2.5 V. The measurement setup is used to investigate the relationship between gate-oxide reliability and different frequencies of input signals in the CMOS analog circuit applications.

The dependence of the unity-gain frequency in the unity-gain buffers on the stress time under the stress of the AC small-signal input with DC offset is shown in Fig. 12. The performances of the operational amplifier with folded-cascode structure are not degraded by the stress of the AC small-signal input with DC offset. In the operational amplifier with the two-stage structure, the high-frequency input signal causes a slow degradation on the unity-gain frequency, but the low-frequency input signal causes a fast degradation on the unity-gain frequency under the stress of the AC small-signal input with DC offset. These measured results are consistent to that report in [13]. The dependences of the small-signal gain and phase margin in the unity-gain buffers on the stress time under the stress of the AC small-signal input with DC offset are almost the same as the change under the DC stress.

As a result, the gate-oxide reliability degrades the performances of the operational amplifier with the two-stage structure under the AC stress. The operational amplifier with folded-cascode structure under the AC stress can be still functioned correctly in high supply voltage (2.5 V) to overcome the gate-oxide reliability.

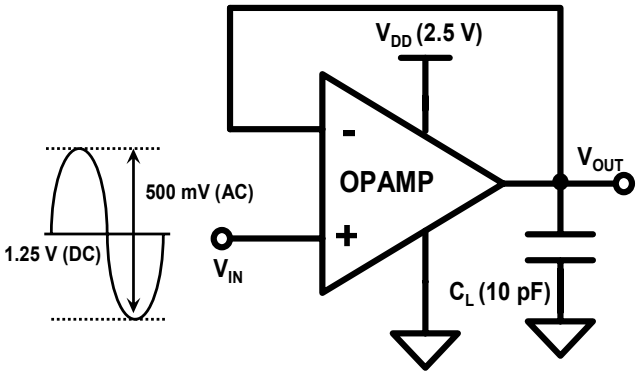


FIGURE 11. THE UNITY-GAIN BUFFER CONFIGURATION FOR OPERATIONAL AMPLIFIERS UNDER THE STRESS OF AC SMALL-SIGNAL INPUT WITH DC OFFSET TO INVESTIGATE THE IMPACT OF GATE-OXIDE RELIABILIITY ON CIRCUIT PERFORMANCES.

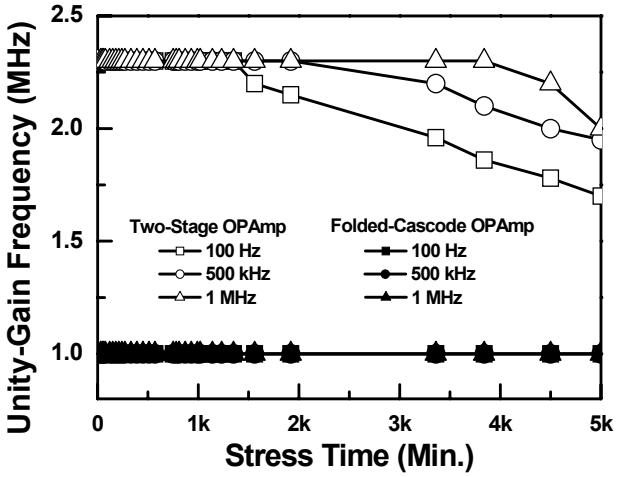


FIGURE 12. THE DEPENDENCE OF THE UNITY-GAIN FREQUENCY ON THE STRESS TIME OF THE OPERATIONAL AMPLIFIERS WITH THE TWO-STAGE STRUCTURE UNDER THE STRESS OF THE AC SMALL-SIGNAL INPUT WITH DC OFFSET.

C. Comparator (Large-Signal Transition)

The operational amplifiers under the comparator (open-loop) configuration are used to investigate the impact of gate-oxide reliability on CMOS analog circuits under the large-signal transition. The inverting input node of the operational amplifiers was biased at 1.25 V, the output capacitance load was set to 10 pF, and the supply voltage V_{DD} was set to 2.5 V. The operational amplifiers under the comparator configuration are continuously tested in this stress of large-signal transition, as shown in Fig. 13. The input square voltage waveform from 1 V to 1.5 V with frequency of 100 Hz is applied to the non-inverting input node of the operational amplifiers under the comparator configuration. The square waveform of input signal from 1 V to 1.5 V will not induce the damage on the input devices of the operational amplifiers, because the voltages across the input devices (V_{GS}, V_{GD}, and V_{DS}) of the operational amplifiers are lower than the 1 V in this measurement.

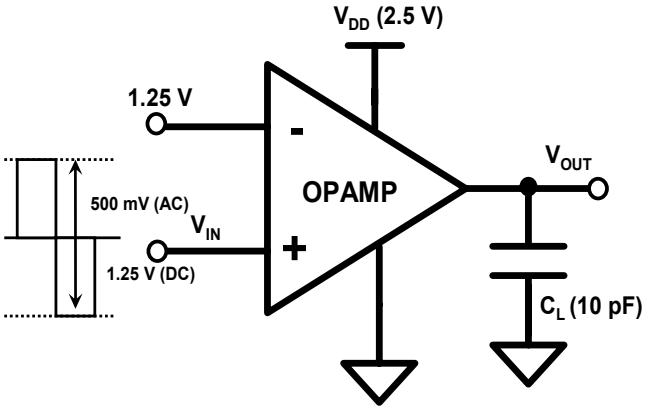


FIGURE 13. THE COMPARATOR CONFIGURATION FOR OPERATIONAL AMPLIFIERS UNDER THE STRESS OF LARGE-SIGNAL TRANSITION TO INVESTIGATE THE IMPACT OF GATE-OXIDE RELIABILIITY ON CIRCUIT PERFORMANCES.

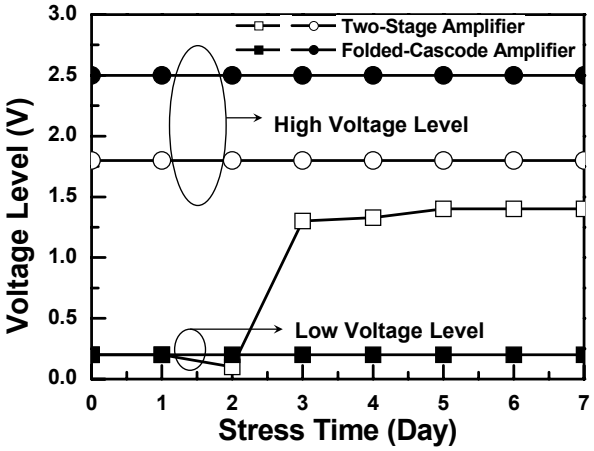


FIGURE 14. THE DEPENDENCES OF THE HIGH AND LOW VOLTAGE LEVELS AT THE OUTPUT NODE ON THE STRESS TIME UNDER STRESS OF LARGE-SIGNAL TRANSITION. THE OPERATIONAL AMPLIFIERS WITH THE TWO-STAGE OR FOLDED-CASCODE STRUCTURES ARE STRESSED UNDER THE COMPARATOR CONFIGURATION.

The dependences of the high and low voltage levels at the output node on the stress time are show in Fig. 14, where the operational amplifiers with the two-stage or folded-cascode structures in the comparator configuration are stressed by the large-signal transition. The low output voltage level of the operational amplifier with the two-stage structure under the stress of large-signal transition is increased when the stress time is increased.

But the high output voltage level of the operational amplifier with two-stage structure is not changed after the same stress condition. The high and low voltage levels at the output node of the operational amplifier with the folded-cascode structure after the 7-day stress of large-signal transition are not changed. The dependence of the unity-gain frequency on the stress time under the stress of large-signal transition is shown in Fig. 15, where the operational amplifiers with the two-stage or folded-cascode structures are connected in the comparator configuration. The unity-gain frequency of the operational amplifiers with the two-stage and folded-cascode structure connected as unity-gain buffer is degraded after the stress of large-signal transition.

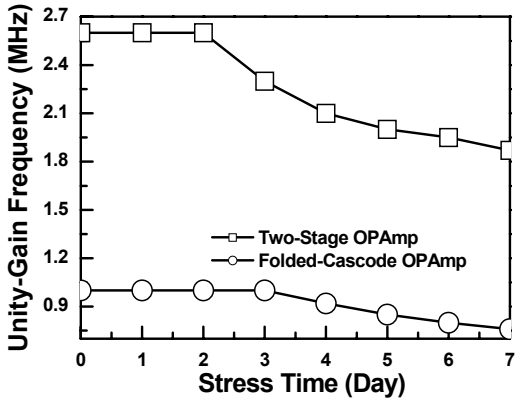


FIGURE 15. THE DEPENDENCE OF THE UNITY-GAIN FREQUENCY ON THE STRESS TIME UNDER THE STRESS OF LARGE-SIGNAL TRANSITION. THE OPERATIONAL AMPLIFIERS WITH THE TWO-STAGE OR FOLDED-CASCODE STRUCTURES ARE STRESSED UNDER THE COMPARATOR CONFIGURATION.

DISCUSSION

The gate-oxide breakdown will degrade the transconductance (g_m), output resistance (r_o), and threshold voltage (V_{th}) of MOSFET devices. After the overstress, the performances of the two-stage operational amplifiers under close-loop and open-loop configurations are degraded. Because the differential amplifier of the operational amplifier with the two-stage structure consists of three cascode MOSFET devices, the voltages across the devices in the differential amplifier of the operational amplifier with the two-stage structure do not exceed 1 V under the stress with the input common-mode voltage of 1.25 V and supply voltage of 2.5 V. The differential amplifier of the operational amplifier with the two-stage structure is not degraded under the stresses with the supply voltage of 2.5 V. However, the output stage in the operational amplifier with the two-stage structure will be degraded under the stress with the input common-mode voltage of 1.25 V and supply voltage of 2.5 V. Therefore, the open-loop gain of the operational amplifier with the two-stage structure is decreased after the stresses. The offset voltage due to the finite gain error and mismatch effect in the devices of the operational amplifier with the two-stage structure is increased after the stress.

The rise time, fall time, output voltage swing, and phase margin of the operational amplifier with the two-stage structure are also decreased after the stress. The gate-oxide reliability in the CMOS analog circuits can be improved by the stacked structure. The DC operating point is very important in the analog circuit design, because all small-signal parameters of the devices and circuits are determined by the DC operating point. If the DC operating point is changed after gate-oxide degradation, the analog circuits will not work correctly. However, the large-signal transition at input and output nodes of the operational amplifier with stacked structure still causes some degradations on circuit performances of analog circuits. As a result, the analog circuits with stacked structure are only effective to improve the gate-oxide reliability under small-signal applications at input and output node.

Under the same stress condition, the two-stage operational amplifier under close-loop (negative-feedback) configuration can be more easily stressed than that under open-loop configuration. The close-loop configuration in the operational amplifiers is used to make the circuits stable and keep the virtual short between inverting and non-inverting nodes of the operational amplifiers. As a result, the inverting, non-inverting, and output nodes of the operational amplifiers have the same DC voltage level under the configuration of negative feedback. The transconductance (g_m), output resistance (r_o), and threshold voltage (V_{th}) of MOSFET devices will be changed after the stress. In order to make the circuits stable and to keep the virtual short between the two input nodes of the operational amplifier with two-stage structure, the DC operating point of the output stage in the two-stage operational amplifier will be changed after the stress. Therefore, the power consumption (circuit performances) of the operational amplifier with the two-stage structure under the negative-feedback configuration will be increased (degraded) after the stress.

EQUIVALENT CIRCUIT MODEL OF A MOSFET AFTER GATE-OXIDE OVERSTRESS

When the NMOSFET with dimension of W = 10 μm and L = 10 μm fabricated in a 130-nm low-voltage CMOS process is stressed at V_G = 1.5 V, the transconductance (g_m) and threshold voltage (V_{th}) under the stress are shown in Figs. 16(a) and 16(b), respectively. The transconductance (g_m) and threshold voltage (V_{th}) of the device are obviously varied during the stress.

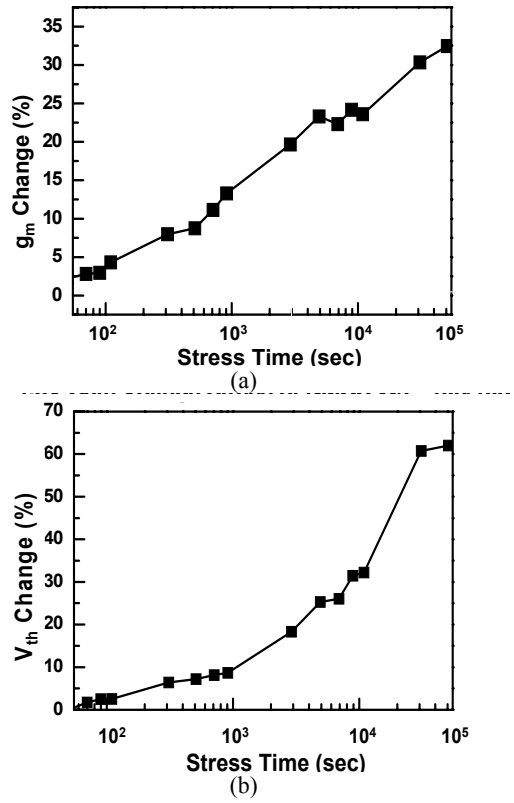


FIGURE 16. THE CHANGE ON (a) g_m , AND (b) V_{th}, OF THE NMOSFET (W = 10 μm AND L = 10 μm) FABRICATED IN A 130-nm PROCESS STRESSED BY V_G = 1.5 V.

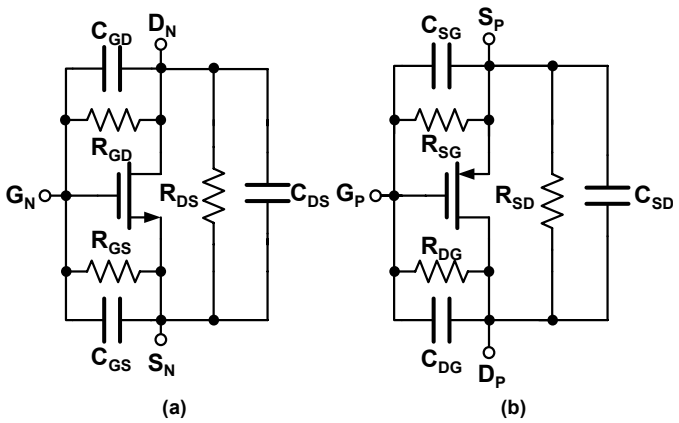


FIGURE 17. THE PRPOSED SIMPLE EQUIVALENT DEVICE MODEL FOR (a) NMOSFET, AND (b) PMOSFET, WITH CONSIDERATION ON THE GATE-OXIDE DEGRADATION IN CMOS ANALOG CIRCUITS.

The gate-oxide breakdown characteristics of MOSFET can be explained by adding a breakdown path [14]-[16]. Thus, in this work, a gate-oxide breakdown equivalent circuit of MOSFET was proposed to replace the level-1 model by adding a breakdown path (modeled as the resistor) between the gate-to-source, gate-to-drain, and source-to-drain nodes of the MOSFET devices, as shown in Figs. 17(a) and 17(b) for NMOSFET and PMOSFET, respectively. The R_{GS} (R_{SG}), R_{GD} (R_{DG}), and R_{DS} (R_{SD}) in the NMOSFET (PMOSFET) are used to model the gate-to-drain and gate-to-source leakage current under gate-oxide degradation. For normal operating condition without gate-oxide degradation, these resistances are infinite. The capacitances (C_{GS} (C_{SG}), C_{GD} (C_{DG}), and C_{DS} (C_{SD})) in the MOSFETs depend on the device fabrication processes. However, both the resistances and the capacitances of this device model are changed during the stress. In addition, all these parameters can be used to simulate the GIDL, DIBL, TDDB, and CHE effects in the CMOS analog circuits during the stress. Thus, the g_m,V_{th}, and r_o variations during the stress can be modeled by the proposed device model.

CIRCUIT ANALYSIS WITH GATE-OXIDE RELIABILITY

To investigate the impact of gate-oxide reliability on the operational amplifier with two-stage structure, the proposed simple equivalent device model in Fig. 17 is used to replace the MOSFETs of the output stage in this operational amplifier, as shown in Fig. 18. For simplicity, the gate-oxide reliability issue on the differential amplifier and bias circuit devices is not considered, because the voltage (< 1 V) across the devices does not cause the gate-oxide reliability in a 130-nm low-voltage CMOS process with the normal operating voltage of 1 V. The capacitances in Fig. 17 are not considered because the frequency response of the operational amplifier with the two-stage structure is dominated by the C_C (Miller compensated capacitance) and C_L (output capacitance load). With the proposed model to consider the gate-oxide degradation, the variations on the small-signal gain (ΔA_V) and the dominant pole ($\Delta\omega_{pole}$) of the operational amplifier with the two-stage structure can be written by

$$\Delta A_{V\_two-stage} \cong -g_{m2}\Delta g_{m6}\Delta g_{m8}(r_{O5} // r_{O2})(\Delta r_{O6} // \Delta r_{O7})(\Delta r_{O8} // \Delta r_{O9}), \quad (5)$$

and

$$\Delta\omega_{pole\_two-stage} = \frac{1}{C_L(\Delta r_{O8} // \Delta r_{O9})}. \quad (6)$$

The Δg_m and Δr_o of the corresponding MOSFET in the equations (5) and (6) are stress-time dependent, as those have shown in Fig. 16.

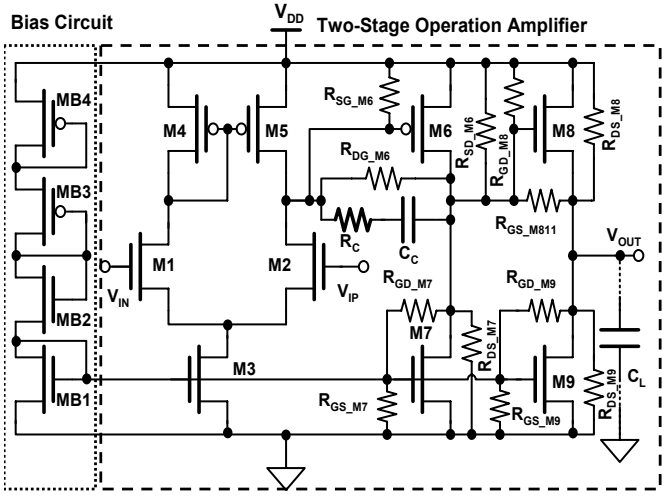
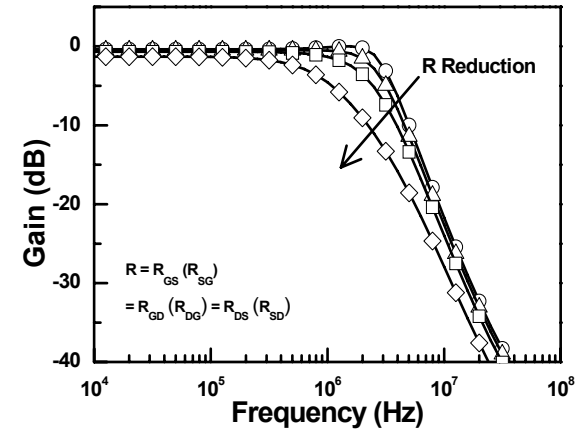
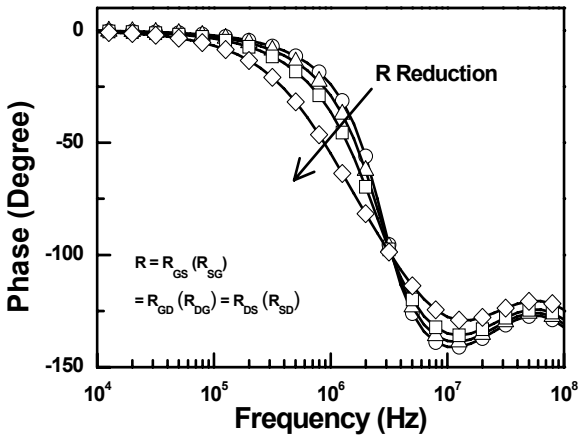


FIGURE 18. THE COMPLETE CIRCUIT OF THE OPERATIONAL AMPLIFIER WITH THE TWO-STAGE STRUCTURE INCLUDING THE DEVICE MODEL OF GATE-OXIDE DEGRADATION AT THE OUTPUT STAGE.



(a)



(b)

FIGURE 19. THE SIMULATED FREQUENCY RESPONSES ON (a) GAIN, AND (b) PHASE, OF THE OPERATIONAL AMPLIFIER WITH THE TWO-STAGE STRUCTURE OPERATING IN THE UNITY-GAIN BUFFER INCLUDING THE GATE-OXIDE DEGRATION EQUIVALENT DEVICE MODEL.

The HSPICE-simulated frequency responses of the operational amplifier with the two-stage structure under the configuration of unity-gain buffer including the device model of the gate-oxide degradation are shown in Figs. 19(a) and 19(b), where the resistances in Fig. 17 are kept at the same ($R = R_{GS}$ (R_{SG}) = R_{GD} (R_{DG}) = R_{DS} (R_{SD})). By changing the resistances in the proposed model, the small-signal performances (such as small-signal gain, unity-gain frequency, and phase) of the operational amplifier with the two-stage structure are re-evaluated with the stress time. After gate-oxide degradation, a leakage path exists across the gate oxide of MOSFET which results in an additional noise source to the transistor. If the gate-oxide degradation becomes more serious, the gate-oxide leakage current will be increased to cause a large variation on the g_m, V_{th}, and r_o of the devices after the stress. Thus, the small-signal performances (gain and phase) of analog circuits will be degraded to the unacceptable condition, when the resistance in Fig. 17 becomes smaller.

CONCLUSION

The impact of MOSFET gate-oxide reliability on CMOS operational amplifiers with the two-stage (non-stacked) and folded-cascode (stacked) structures has been investigated and analyzed. The tested structures of the operational amplifiers including both the unity-gain buffer (close-loop) and comparator (open-loop) configurations are stressed under different input frequencies and signals. Because the DC operating point of the analog circuits is changed due to the gate-oxide degradation, the small-signal performances of the operational amplifier with the two-stage structure are seriously degraded after the stress. The performances of the operational amplifier with the two-stage structure under the close-loop configuration are damaged more easily than that under the open-loop configuration after the stress. The gate-oxide reliability in the CMOS analog circuits can be improved by the stacked structure under small-signal input and output applications. But, the large-signal transition still causes some degradation on the circuit performances of the operational amplifier with the folded-cascode (stacked) structure. The optimized design solution to further overcome such degradation from the stress of large-signal transition on the operational amplifiers should be an important challenge to analog circuits in the nanoscale CMOS technology. The simple equivalent device model of gate-oxide reliability used to evaluate the performance degradation of analog circuits has been also proposed and simulated.

ACKNOWLEDGMENT

The authors would like to thank Infineon-ADMtek Corporation, Hsinchu, Taiwan, for their support of this research and chip fabrication.

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