DESIGN ON POWER-RAIL ESD CLAMP CIRCUIT FOR 3.3-V I/O INTERFACE BY USING ONLY1-V/2.5-V LOW-VOLTAGE DEVICES IN A 130-NM CMOS PROCESS

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ABSTRACT

A new power-rail ESD clamp circuit in a 130-nm 1-V/2.5-V CMOS process for application in 3.3-V mixed-voltage I/O interface is proposed. The devices used in this power-rail ESD clamp circuit are all 1-V or 2.5-V low-voltage NMOS/PMOS devices, which are specially designed without suffering the gate-oxide reliability issue under 3.3-V I/O interface applications. A special ESD detection circuit realized with the low-voltage devices is designed to improve ESD robustness of the stacked NMOS by substrate-triggered technique. The experimental results verified in a 130-nm CMOS process have proven the excellent effectiveness of this new proposed power-rail ESD clamp circuit.

INTRODUCTION

Electrostatic discharge (ESD) is an important reliability issue for IC products in the scaled-down CMOS technologies. To achieve whole-chip ESD protection, an effective power-rail ESD clamp circuit between the VDD and VSS power lines is necessary, especially under pin-to-pin and VDD-to-VSS ESD stresses [1]. In mixed-voltage I/O applications, it is required to design the power-rail ESD clamp circuit with only low-voltage devices that can sustain the high power-supply voltage without suffering the gate-oxide reliability issue [2]-[7]. Besides the gate-oxide reliability issue, the standby leakage current of the power-rail ESD clamp circuit during normal circuit operating conditions is another concern [3], especially for the portable electronic products.

To achieve a whole-chip ESD protection in mixed-voltage I/O interfaces, two modified ESD protection schemes for 1-V/3.3-V mixed-voltage I/O interfaces are shown in Figs. 1(a) and 1(b). In Fig. 1(a), an extra dummy supply line (marked as V_{ESD}) is added into the chip for cooperation with the power-rail ESD clamp circuit to achieve ESD protection in the I/O pad with 3.3-V input signals. This ESD protection scheme is suitable for ICs with power-down mode operation [7], which is an important power-saving technology in nowadays SOC or portable devices. For generic ICs without specific circuit functions such as the power-down mode operation, the whole-chip ESD protection scheme shown in Fig. 1(a) can be further simplified to Fig. 1(b), where the extra bond pad for external 3.3-V power supply (marked as VDD_h) is optional, depending on the system specification and the circuit requirement.

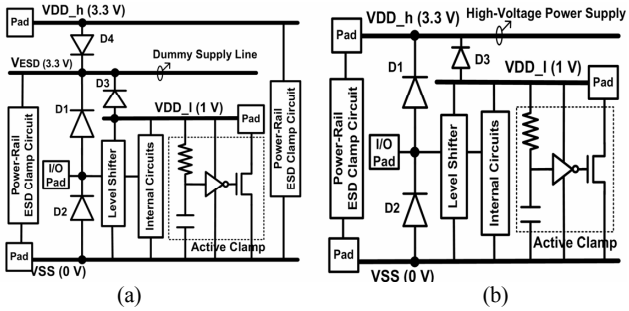

FIGURE 1. TWO ESD PROTECTION SCHEMES FOR MIXED-VOLTAGE I/O INTERFACE.

In this work, a novel power-rail ESD clamp circuit implemented with only 1-V/2.5-V NMOS/PMOS devices is designed for application in the 3.3-V I/O interfaces without suffering the gate-oxide reliability issue. This new power-rail ESD clamp circuit has an efficient ESD detection circuit to substantially enhance the turn-on efficiency of the power-rail ESD clamp device. This new power-rail ESD clamp circuit has been successfully verified in a 130-nm 1-V/2.5-V CMOS process with excellent ESD protection capability and extremely low standby current.

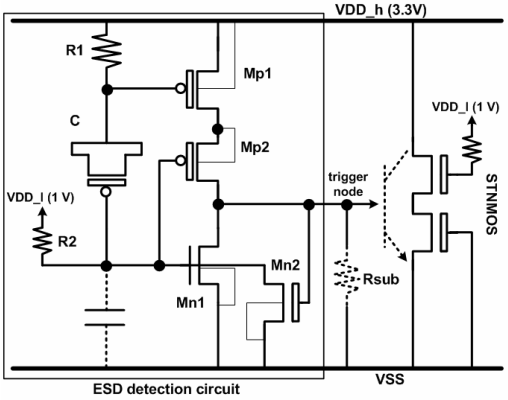

FIGURE 2. THE NEW PROPOSED POWER-RAIL ESD CLAMP CIRCUIT WITH ONLY 1-V AND 2.5-V DEVICES FOR OPERATING UNDER HIGH-VOLTAGE VDD_h OF 3.3V.

POWER-RAIL ESD CLAMP CIRCUIT FOR HIGH-VOLTAGE APPLICATIONS

The novel power-rail ESD clamp circuit contains a substrate-triggered stacked-NMOS (STNMOS) as the ESD clamp device and an ESD detection circuit. As shown in Fig. 2, the new proposed power-rail ESD clamp circuit is realized with only 1-V (Mn1) and 2.5-V (Mp1, Mp2, Mn2, C, and STNMOS) devices to operate at 3.3-V I/O interface without the risk of gate oxide reliability. Under normal circuit operating conditions, where the normal power-on transition of VDD_h and VDD_l are in the order of several milli-seconds, the gate voltage of Mp1 can follow up the voltage transient on VDD_h to keep the ESD detection circuit off. Meanwhile, the source voltage of Mp2 is biased at (VDD_l+|Vtp|), where Vtp is the threshold voltage of Mp2. Mn1 is kept on during normal operating conditions to increase the noise immunity of the power-rail ESD clamp circuit. By such arrangement with VDD_h of 3.3V and VDD_l of 1V, voltages across low-voltage devices in the new proposed power-rail ESD clamp circuit do not exceed the process given limitation, 2.75V for 2.5-V devices and 1.1V for 1V devices.

When ESD transient voltage is applied to VDD_h with VSS relatively grounded, the gate of Mp1 is initially kept at a low voltage level (around 0V) due to the RC delay of R1 and C in the ESD detection circuit. The VDD_l node is initially floating with an initial voltage level of 0V, before the ESD voltage is applied across VDD_h and VSS. Some ESD transient voltage might be coupled to VDD_l through the parasitic capacitance when ESD stress is zapped on VDD_h, but the R2 and the parasitic capacitance at the gates of Mn1 and Mp2 will keep the gate of Mp2 at 0V for a long period of time. So, Mp1 and Mp2 with initial gate voltages at ~0V can be quickly turned on by the ESD energy to generate the trigger current into the trigger node of STNMOS. As long as the base-emitter voltage of the lateral n-

p-n BJT inherent in the STNMOS device is greater than 0.7V, the STNMOS can be triggered on to discharge ESD current from VDD_h to grounded VSS.

If Mn1 is turned on during ESD transition by unexpected coupling effect to its gate through the parasitic capacitance in the layout, the base voltage of the lateral BJT could be pulled down to zero to turn off the lateral BJT in the STNMOS device. To avoid such possible condition during ESD transition, the Mn2 is added in the ESD detection circuit to keep the gate of Mn1 and Mp2 at 0V, when the base voltage of lateral BJT in the STNMOS device is charged up by the current flowing through Mp1 and Mp2.

EXPERIMENTAL RESULTS

Under normal circuit operating conditions with VDD_l of 1V and temperature of 25°C (125 °C), the leakage current of the power-rail ESD clamp circuit at VDD_h of 3.3V is 283pA (19.8nA), whereas the leakage current of the stand-alone STNMOS is 153pA (11.3nA), as shown in Fig. 3. The device dimensions of Mp1, Mp2 and STNMOS in the measured power-rail ESD clamp circuit are 120μm/0.28μm, 120μm/0.28μm, and 300μm/0.3μm, respectively. With an extremely low leakage current of ~20nA at the high temperature of 125°C, the proposed power-rail ESD clamp circuit is suitable for SOC or portable electronic systems, which require small standby leakage current.

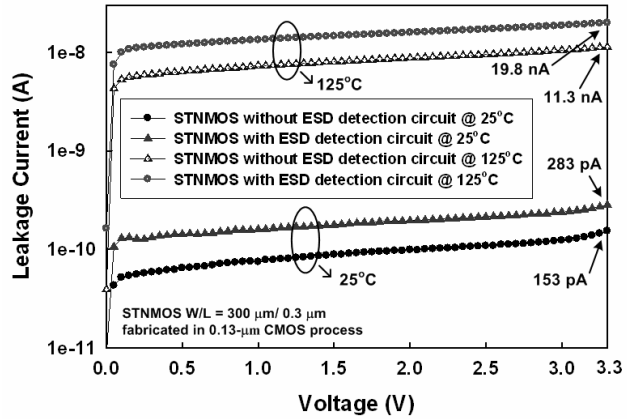

FIGURE 3. THE LEAKAGE CURRENTS OF STNMOS WITH OR WITHOUT THE ESD DETECTION CIRCUIT UNDER DIFFERENT TEMPERATURES.

To verify the effectiveness of the ESD detection circuit in the proposed power-rail ESD clamp circuit, a 0-to-7V voltage pulse with a rise time of 10ns is applied to the VDD_h pin of a specially designed testchip, which is shown in the inset of Fig. 4. In the specially drawn testchip, the substrate trigger node of a stand-alone STNMOS and the trigger node of the ESD detection circuit are separately connected to different bond pads and then wired to each other with a current probe on it for measuring the transient current. The measured substrate-triggered current almost simultaneously appears with a peak current of ~43mA when the 0-to-7V voltage pulse is applied to VDD_h pin. So, the STNMOS with ESD detection circuit can be quickly triggered on to clamp the overstress ESD voltage. Therefore, the ESD detection circuit can function properly without interfering with the input/output signals during normal circuit operating conditions.

Because the ESD detection circuit is efficient enough to trigger on the STNMOS, turn-on uniformity and turn-on speed of the STNMOS are substantially increased so that the ESD robustness of the substrate-triggered STNMOS is substantially increased. The ESD robustness of STNMOS devices with or without the new proposed ESD detection circuit is compared in Table I.

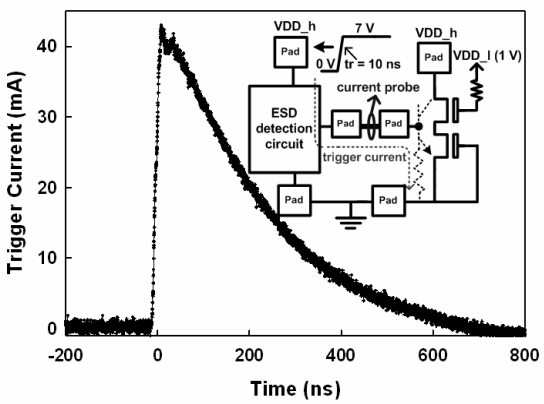

FIGURE 4. THE MEASURED SUBSTRATE-TRIGGERED CURRENT GENERATED BY THE ESD DETECTION CIRCUIT UNDER 0-TO-7V VOLTAGE PULSE WITH A RISE TIME OF 10NS ON THE VDD_h PIN.

TABLE I
ESD ROBUSTNESS OF STNMOS DEVICES
WITH OR WITHOUT THE NEW PROPOSED ESD DETECTION CIRCUIT

STNMOS W/L (μm/μm)	HBM ESD Level (kV)		MM ESD Level (V)		It2 Level (A)	
	without detection circuit	with detection circuit	without detection circuit	with detection circuit	without detection circuit	with detection circuit
300/0.3	1	3.75	150	250	2.8	3.1
400/0.3	1.5	5	175	325	3.7	4.3
600/0.3		6.5		375		5.2

CONCLUSION

A new power-rail ESD clamp circuit realized with low-voltage devices for 1-V/3.3-V mixed-voltage I/O interface has been successfully verified in a 130-nm 1-V/2.5-V CMOS process. The proposed ESD detection circuit can effectively increase the ESD robustness and the turn-on speed of the STNMOS. This new proposed power-rail ESD clamp circuit with the advantages of very low leakage current, fast turn-on speed, higher ESD robustness, and no gate-oxide reliability issue is an excellent ESD protection solution to the mixed-voltage I/O interface with high-voltage input/output signals.

REFERENCES

[1] C. Cook and S. Daniel, "Characterization of new failure mechanisms arising from power-pin ESD stressing," in *Proc. EOS/ESD Symp.*, 1993, pp. 149–156.

[2] T. Maloney and W. Kan, "Stacked PMOS clamps for high-voltage power supply protection," in *Proc. EOS/ESD Symp.*, 1999, pp. 70–77.

[3] S. S. Poon and T. Maloney, "New considerations for MOSFET power clamps," in *Proc. EOS/ESD Symp.*, 2002, pp. 1–5.

[4] L. R. Avery, "ESD protection for overvoltage friendly input/output circuits," U.S. Patent 5708550, Jan. 1998.

[5] J. Watt, "Fast turn-on silicon controlled rectifier (SCR) for electrostatic discharge (ESD) protection," U.S. Patent 5825600, Oct. 1998.

[6] E. R. Worley, C. T. Nguyen, R. A. Kjar, and M. R. Tennyson, "Method and apparatus for coupling multiple independent on-chip VDD busses to an ESD core clamp," U.S. Patent 5654862, Oct., 1996.

[7] M.-D. Ker and K.-H. Lin, "Design on ESD protection scheme for IC with power-down-mode operation," *IEEE J. Solid-State Circuits*, vol. 39, pp. 1378–1382, 2004.