THE IMPACT OF INNER PICKUP ON ESD ROBUSTNESS OF MULTI-FINGER NMOS IN NANOSCALE CMOS TECHNOLOGY

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ABSTRACT

The impact of pickup structure on ESD robustness of multi-finger MOSFET devices in the nanoscale CMOS process is investigated in this work with 1.2-V and 2.5-V devices in a 130-nm CMOS process. The multi-finger MOSFET device without the pickup structure inserted into its source region can sustain a much higher ESD level and more compact layout area for I/O cells.

[*Keywords:* electrostatic discharge (ESD), multi-finger MOSFET, layout, pickup structure.]

INTRODUCTION

As CMOS scaling towards nanoscale technologies, ESD reliability has been a major concern of integration circuits. In order to sustain the desired ESD robustness, ESD-protection MOSFET in the ESD protection circuits often has a total channel width of several hundreds micrometer. With such a large device dimension for ESD protection, the MOSFET devices in I/O cell layout are often drawn in the multi-finger structure to save layout area. When the gate-grounded NMOS (GGNMOS) is under ESD stress, the parasitic lateral n-p-n bipolar in NMOS device structure will be triggered into its snapback region to discharge ESD current [1]. However, if one of the parallel multiple fingers is first triggered on during ESD stress, the ESD current is mainly discharged through the first turned-on finger. Such non-uniform turned-on issue on multi-finger MOSFET often decreases its ESD robustness, even if the MOSFET has a large enough device dimension [2].

However, even if the layout of multi-finger NMOS is drawn uniformly, the equivalent substrate resistance of the central finger is still largest because the distance from its channel region to the guard ring is longest in I/O layout. Thus, the central finger of the multi-finger NMOS is often turned on earlier than the other fingers to cause the non-uniform turned-on issue. In order to solve this non-uniform turned-on problem, the additional pickup structure (inserting into each source region of the multi-finger NMOS layout) was reported and recommended to improve ESD robustness in a 0.35-μm CMOS technology by foundry [3], [4], because all the fingers can have equal equivalent substrate resistance. The layout top view and device cross-sectional view of the additional P+ pickup structure inserted into the source region of a multi-finger NMOS device are shown in Figs. 1(a) and 1(b), respectively. However, the impact of the pickup structures inserted into source regions of multi-finger NMOS devices on the ESD robustness of MOSFET devices should be further investigated in the nano-scale CMOS process.

DEVICE STRUCTURE

The 1.2-V and 2.5-V devices in a 130-nm salicided CMOS process with different gate-oxide thicknesses are drawn and fabricated in silicon chip. The layout structures of the NMOS, including 1.2-V and 2.5-V NMOS devices with different numbers (0, 1, 2, and 5) of the P+ pickup structures inserted into source regions (called as number of pickups for NMOS) of multi-finger NMOS devices, are drawn in Figs. 2(a), 2(b), 2(c), and 2(d), respectively. Each multi-finger NMOS device has 12 parallel fingers, and every finger is drawn with a finger length of 40 μm. So, the total channel width for each multi-finger NMOS device is 480 μm, and a P+ guard ring is surrounding the whole finger-type NMOS in the layout.

EXPERIMENTAL RESULTS

The parasitic lateral bipolar trigger current (It1), and the snapback holding voltage (Vh) of fabricated MOSFET devices with different number of pickups, are measured by the transmission line pulse (TLP) generator with low energy. The It1 and Vh of the 1.2-V and 2.5-V GGNMOS with different number of pickups are compared in Figs. 3 and 4, respectively. When the number of pickup structures are increased from 0 to 5, the It1 (Vh) is increased in both 1.2-V and 2.5-V devices. The base resistance (Rsub) of the parasitic lateral bipolar is reduced by the increase of the additional pickup structures, where the distance between the channel regions to the substrate contact becomes shorter. With a low base resistance (Rsub), the parasitic lateral bipolar in the multi-finger MOSFET needs higher trigger current (It1) to trigger it on. With an increased snapback holding voltage (Vh), the power dissipation generated by ESD current on the multi-finger MOSFET becomes higher. These mechanisms cause ESD performance of multi-finger MOSFET to be seriously decreased when the number of pickup structures increased. TLP-measured secondary breakdown current (It2) for 1.2-V and 2.5-V multi-finger GGNMOS with different number of pickup structures are compared in Fig. 5. The dependences of HBM and MM ESD levels (measured by a *Zapmaster* ESD tester) on different number of pickup structures in the multi-finger MOSFET are compared in Figs. 6(a) and 6(b), respectively. The TLP-measured It2, HBM, and MM ESD levels are confirmed that the increase on the number of pickup structures causes a lower ESD robustness on both 1.2-V and 2.5-V multi-finger devices.

CONCLUSION

The degradation of ESD performance due to pickup structures inserted into source regions of multi-finger NMOS devices has been studied in a 130-nm CMOS process. The MOSFET devices with the pickup structures inserted into the source region are not recommended in the nanoscale CMOS technology. Without adding the pickup structures in the source regions, the I/O cell can be realized with more compact silicon area and higher ESD robustness in IC products.

REFERENCES

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[3] J.-H. Lee et al., *Proc. IPFA*, 1999, pp. 162-167.
[4] J.-H. Lee, US patent # 5,811,856, 1998.

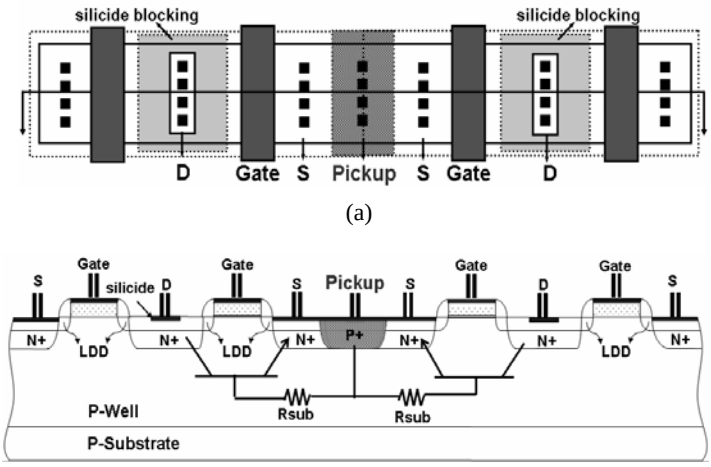

FIGURE 1. THE (a) LAYOUT TOP VIEW, AND (b) DEVICE CROSS-SECTIONAL VIEW, OF THE NMOS DEVICE WITH THE ADDITIONAL PICKUP STRUCTURES INSERTED INTO ITS SOURCE REGIONS.

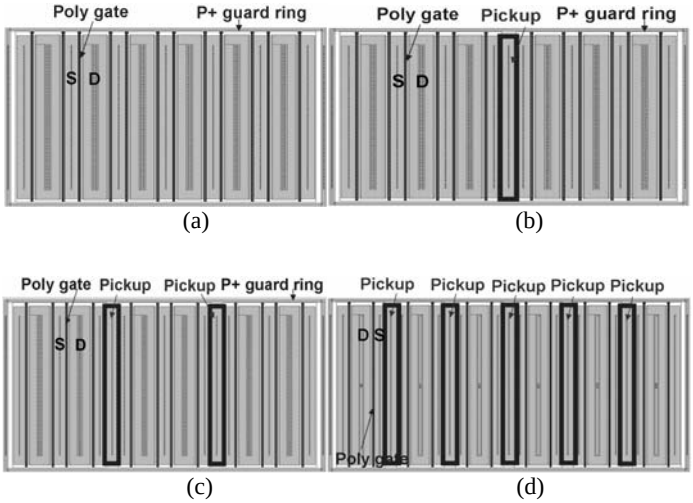

FIGURE 2. THE LAYOUT TOP VIEW OF THE MULTI-FINGER MOSFET WITH DIFFERENT NUMBER OF ADDITIONAL PICKUP STRUCTURES INSERTED INTO SOURCE REGIONS, (a) PICKUP = 0, (b) PICKUP = 1, (c) PICKUP = 2, AND (d) PICKUP = 5.

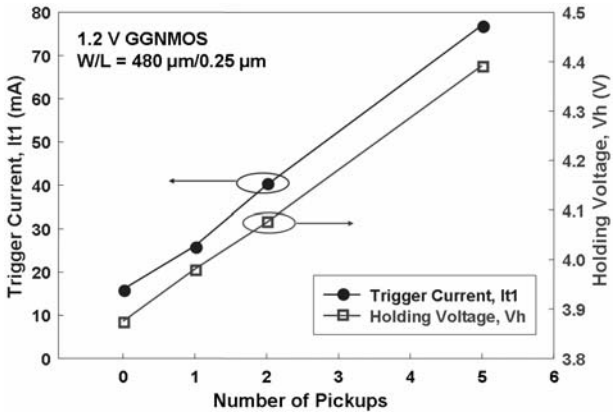

FIGURE 3. THE PARASITIC LATERAL BIPOLAR TRIGGER CURRENT (IT1) AND THE SNAPBACK HOLDING VOLTAGE (VH) OF THE 1.2-V NMOS WITH DIFFERENT NUMBER (0, 1, 2, 5) OF PICKUPS.

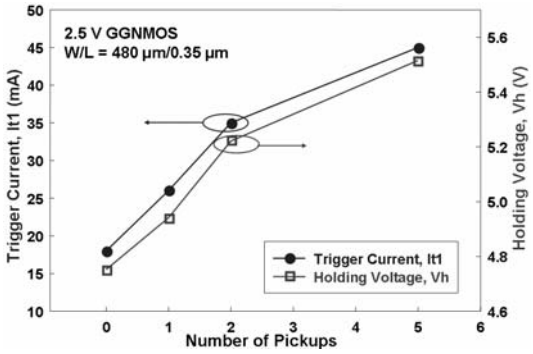

FIGURE 4. THE PARASITIC LATERAL BIPOLAR TRIGGER CURRENT (IT1) AND THE SNAPBACK HOLDING VOLTAGE (VH) OF THE 2.5-V NMOS WITH DIFFERENT NUMBER (0, 1, 2, 5) OF PICKUPS.

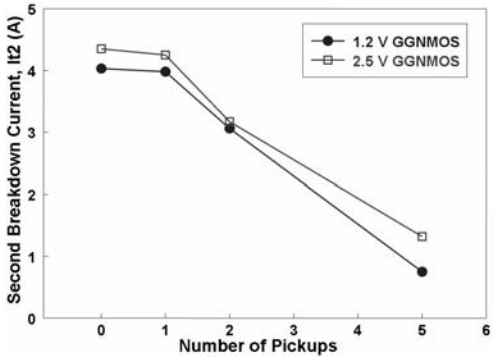

FIGURE 5. DEPENDENCE OF IT2 LEVEL ON DIFFERENT NUMBER OF PICKUP STRUCTURES OF 1.2-V AND 2.5-V MULTI-FINGER NMOS.

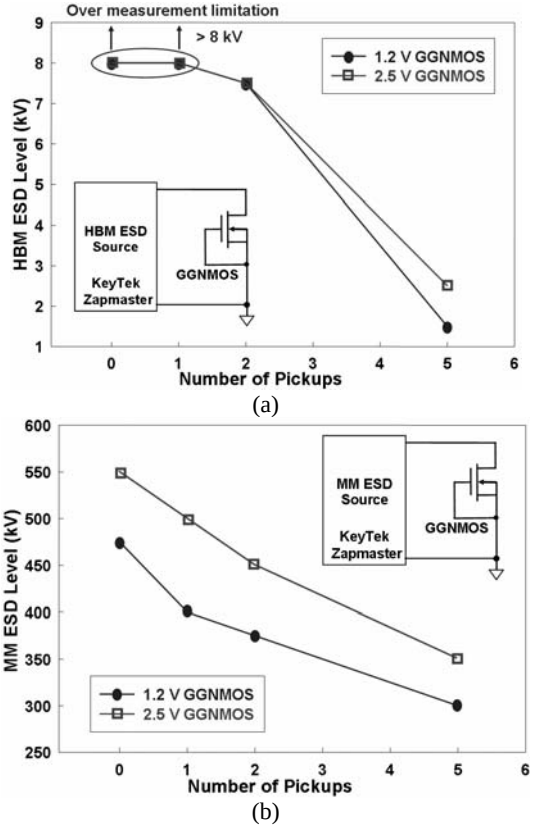

FIGURE 6. DEPENDENCE OF (a) HBM ESD LEVEL, AND (b) MM ESD LEVEL, ON DIFFERENT NUMBER OF PICKUP STRUCTURES OF 1.2-V AND 2.5-V MULTI-FINGER NMOS.