EXPERIMENTAL EVALUATION AND DEVICE SIMULATION OF DEVICE STRUCTURE INFLUENCES ON LATCHUP IMMUNITY IN HIGH-VOLTAGE 40-V CMOS PROCESS

Sheng-Fu Hsu, Ming-Dou Ker, Geeng-Lih Lin*, and Yeh-Ning Jou*

Nanoelectronics and Gigascale Systems Laboratory
Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan
* Reliability Assurance Department
Vanguard International Semiconductor Corporation, Hsinchu, Taiwan

ABSTRACT

The dependence of device structures and layout parameters on latchup immunity in high-voltage (HV) 40-V CMOS process have been verified with silicon test chips and investigated with device simulation. It was demonstrated that a specific test structure considering the parasitic silicon controlled rectifier (SCR) resulting from isolated asymmetric HV NMOS and HV PMOS has the best latchup immunity. The test structures and simulation methodology proposed in this work can be applied to extract safe and compact design rule for latchup prevention in HV CMOS process. All the test chips are fabricated in a 0.25-μm 40-V CMOS technology.

INTRODUCTION

High-voltage (HV) CMOS process has been widely used in driver circuits, telecommunication, power switch, motor control systems, etc [1]. One tough challenge on reliability issue in HV CMOS process is to eliminate the possible occurrence of latchup [1]-[6]. However, due to an ultra-high operating voltage, it's rather difficult to achieve the latchup-free purpose in HV CMOS ICs by raising the latchup holding voltage to exceed the normal circuit operating voltage. HV CMOS ICs are always inevitable to be damaged by latchup-generated high power. Thus, how to improve the latchup immunity in HV CMOS process is indeed a crucial reliability issue.

In this paper, latchup immunity in HV 40-V CMOS process is investigated under different test structures. These test structures are used to consider each possible case of the parasitic silicon controlled rectifiers (SCR) in HV CMOS process with different device structures, including isolated or non-isolated, symmetric or asymmetric device structures. In addition, layout parameters such as spacing from anode to cathode, as well as guard ring width, are also investigated to find their dependence on latchup immunity. All the test chips are fabricated in a 0.25-μm 40-V CMOS technology. Moreover, the measured latchup characteristics on different test structures in HV CMOS process can be qualitatively and quantitatively verified by device simulation.

DEVICE STRUCTURES OF HV MOSFETS

The device structures of HV MOSFETs, which have drain-extended structures [7], can be classified into two major parts: (1) isolated or non-isolated, and (2) symmetric or asymmetric, device structures in a given HV 40-V CMOS process.

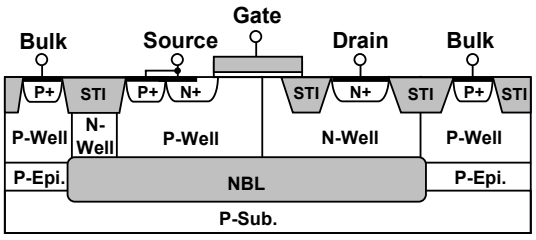
A. Isolated and Non-Isolated Device Structures

The device cross-sectional views of isolated and non-isolated HV NMOS are depicted in Figs. 1(a) and 1(b), respectively. The term "isolated" means that there is an additional N+ buried layer (NBL) beneath the N-well (P-well) region in device active region. So, the NBL can combine its peripheral N-well regions to "isolate" the whole device active region, as shown in Fig. 1(a). In contrast with the isolated HV NMOS, there is no NBL in non-isolated HV NMOS. Instead, whole device is fabricated on a thin P-epitaxial (P-epi.) layer above the P-substrate, as shown in Fig. 1(b).

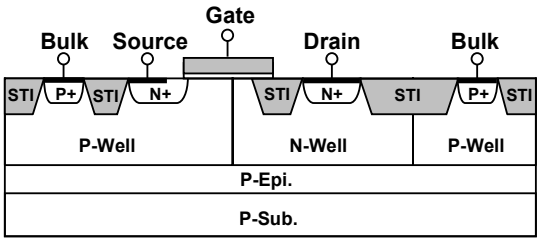
The device cross-sectional view of an isolated HV PMOS is depicted in Fig. 2. For HV PMOS, such isolated device structure is necessary, because it can provide an isolation region, which consists of NBL and peripheral N-well regions, to prevent the possible leakage current path from P+ source terminal of HV PMOS (+40V) to P+ pickups (0V) outside the isolation region.

B. Symmetric and Asymmetric Device Structures

The device cross-sectional views of non-isolated symmetric and non-isolated asymmetric HV NMOS are depicted in Figs. 3 and 1(b),



(a)



(b)

FIGURE 1. THE DEVICE CROSS-SECTIONAL VIEWS OF (A) ISOLATED, AND (B) NON-ISOLATED, HV NMOS.

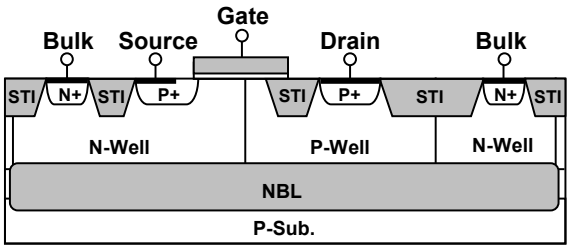


FIGURE 2. THE DEVICE CROSS-SECTIONAL VIEW OF AN ISOLATED HV PMOS.

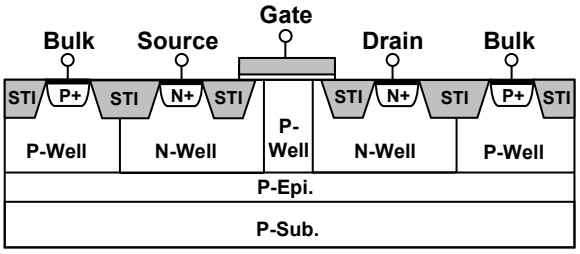


FIGURE 3. THE DEVICE CROSS-SECTIONAL VIEW OF A NON-ISOLATED SYMMETRIC HV NMOS.

respectively. The term "symmetric" means that both drain and source N+ diffusions are enclosed with N-well regions, which are used to sustain high operating voltage (+40V), as shown in Fig. 3. For asymmetric HV NMOS, however, such N-well region to sustain high voltage is only implemented on drain side, as shown in Fig. 1(b). Symmetric device has the advantage of high-voltage sustainability on both drain and source sides. However, it must suffer larger turn-on resistance and larger layout area.

LATCHUP TEST STRUCTURES

In HV CMOS ICs, latchup can be triggered on due to the existence of the parasitic SCR between HV PMOS and HV NMOS. The device cross-sectional view of an inverter logic circuit, which consists of non-isolated asymmetric HV NMOS and isolated asymmetric HV PMOS, is shown in Fig. 4. The parasitic SCR composed of two cross-couple bipolar junction transistors (BJTs) is also depicted in Fig. 4. Such an inverter circuit is the basic logic component for CMOS ICs. The parasitic SCR within it, however, is the origin of latchup. Once latchup is triggered on, large current will conduct through a low-impedance path from V_{DD} (source of HV PMOS) to GND (source of HV NMOS). Thus, HV CMOS ICs will fail to function correctly and even be burned out due to latchup-generated high power.

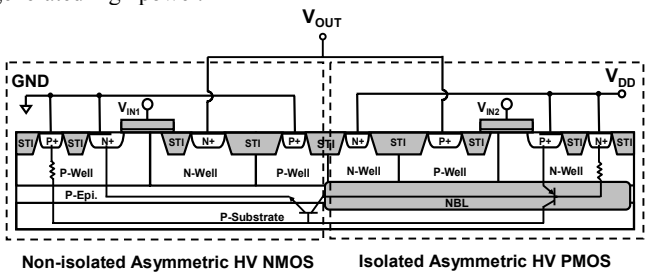
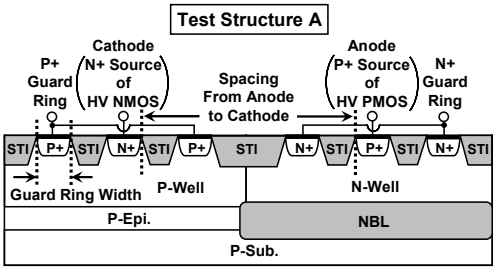
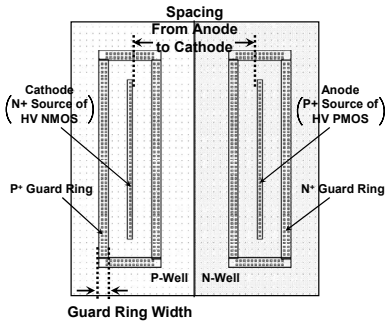


FIGURE 4. THE CROSS-SECTIONAL VIEW OF AN INVERTER LOGIC CIRCUIT CONSISTING OF NON-ISOLATED ASYMMETRIC HV NMOS AND ISOLATED ASYMMETRIC HV PMOS.

In order to investigate each possible case of the parasitic SCR in HV CMOS circuits due to different device structures, three different test structures (test structures A, B, and C) are used to investigate the dependence of device structures and layout parameters on latchup immunity in HV CMOS circuits. The device cross-sectional views and their layout top views of the test structures A, B, and C are depicted in Figs. 5, 6, and 7, respectively. Test structure A (B) is employed to simulate the parasitic SCR resulting from non-isolated asymmetric (symmetric) HV NMOS and isolated asymmetric (symmetric) HV PMOS. Test structure C is used to simulate the parasitic SCR resulting from isolated asymmetric HV NMOS and HV PMOS. Table I summarizes the device structures of HV MOSFETs in each latchup test structure. Those test structures have been fabricated in a 0.25-μm 40-V CMOS process.

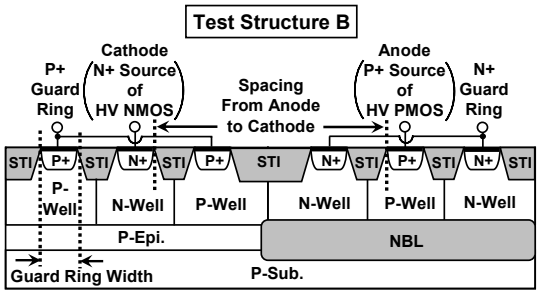


(a)

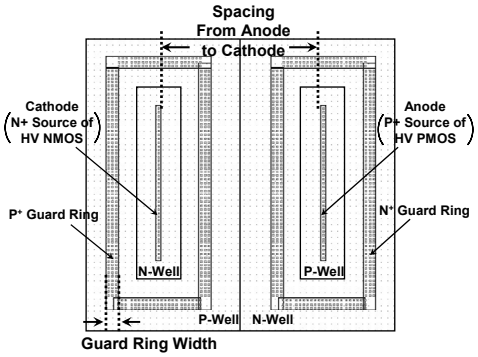


(b)

FIGURE 5. (A) DEVICE CROSS-SECTIONAL VIEW, AND (B) LAYOUT TOP VIEW, OF THE TEST STRUCTURE A. TEST STRUCTURE A IS USED TO SIMULATE THE PARASITIC SCR RESULTING FROM NON-ISOLATED ASYMMETRIC HV NMOS AND ISOLATED ASYMMETRIC HV PMOS.

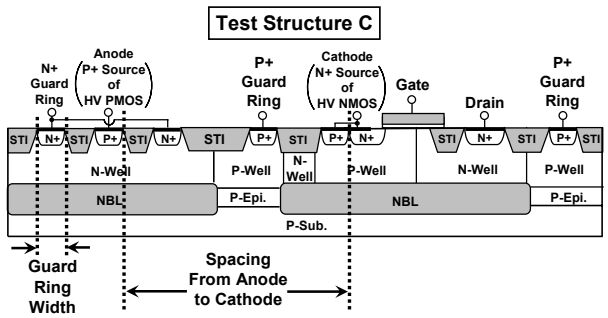


(a)

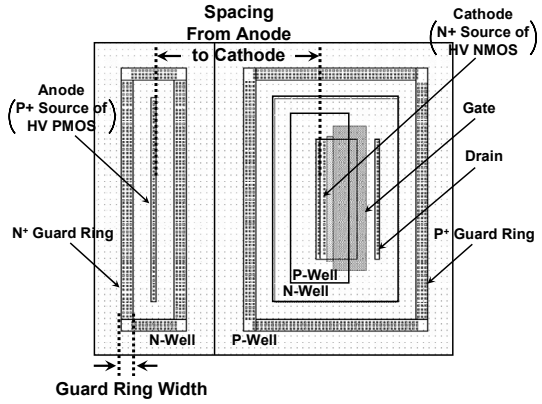


(b)

FIGURE 6. (A) DEVICE CROSS-SECTIONAL VIEW, AND (B) LAYOUT TOP VIEW, OF THE TEST STRUCTURE B. TEST STRUCTURE B IS USED TO SIMULATE THE PARASITIC SCR RESULTING FROM NON-ISOLATED SYMMETRIC HV NMOS AND ISOLATED SYMMETRIC HV PMOS.



(a)



(b)

FIGURE 7. (A) DEVICE CROSS-SECTIONAL VIEW, AND (B) LAYOUT TOP VIEW, OF THE TEST STRUCTURE C. TEST STRUCTURE C IS USED TO SIMULATE THE PARASITIC SCR RESULTING FROM ISOLATED ASYMMETRIC HV NMOS AND HV PMOS.

TABLE I. SUMMARY OF THE DEVICE STRUCTURES OF HV MOSFETS IN EACH LATCHUP TEST STRUCTURE.

	NMOS Type	PMOS Type
Latchup Test Structure A (Fig. 5)	Non-Isolated Asymmetric	Isolated Asymmetric
Latchup Test Structure B (Fig. 6)	Non-Isolated Symmetric	Isolated Symmetric
Latchup Test Structure C (Fig. 7)	Isolated Asymmetric	Isolated Asymmetric

EXPERIMENTAL RESULTS

To investigate the latchup characteristics in HV CMOS process, the transmission line pulsing (TLP) generator [8] with pulse width (rise time) of 100ns (~10ns) is used to measure latchup I-V curves of three different test structures with various layout parameters. In these test structures, anode and N+ guard rings are connected to V_{DD}, whereas cathode and P+ guard rings are connected to GND. Latchup parameters such as trigger voltage and holding voltage can be extracted from these TLP-measured latchup I-V curves. Thus, the dependence of device structures and layout parameters on latchup immunity in HV CMOS process can be well evaluated. All the latchup measurements are performed at the room temperature of 25°C.

When the continuous-type curve tracer (such as *Tektronix 370A*) is used to measure the latchup I-V curves of HV test structures, these HV devices are usually damaged due to latchup-generated high power before the latchup I-V curves are observed or extracted. In order to avoid the HV devices being damaged so easily by the high-power curve tracer for latchup characterization, TLP generator [8] with pulse width (rise time) of 100ns (~10ns) is used instead in this work to measure latchup I-V curves of three different test structures with various layout parameters. Compared to the general high-power curve tracer whose pulse width (i.e. stress time) approximates to ~ms range, the TLP generator has much shorter pulse width of 100ns and limited energy. Thus, by using TLP generator, the HV devices will not be damaged so easily under a latchup state, and the latchup trigger voltage and holding voltage can be certainly extracted. Such TLP generator with pulse width of 100ns is commonly used for electrostatic discharge (ESD) characterization. To well clarify the TLP-measured latchup characteristics in practical field applications, JEDEC latchup test [9] should be further performed to verify the dependence of device structures and layout parameters on latchup immunity in HV CMOS process.

A. Relationships between Latchup Trigger (Holding) Voltage and Spacing from Anode to Cathode

The relationships between latchup trigger (holding) voltage and spacing from anode to cathode for test structures A, B, and C are shown in Fig. 8. Obviously, test structure C (considering the parasitic SCR resulting from isolated asymmetric HV NMOS and HV PMOS) has the most prominent latchup immunity due to its highest latchup trigger and holding voltage. For example, latchup holding voltage can be as high as 48V (>40V to satisfy latchup-free purpose) for test structure C, even though the spacing from anode to cathode is only as short as 27.5μm, as its TLP-measured latchup I-V curve shown in Fig. 9. However, latchup holding voltage can be only enhanced up to 36V (37V) for test structure A (B), even though the spacing from anode to cathode is as long as 31.6μm, as its TLP-measured latchup I-V curve shown in Fig. 10 (Fig. 11).

B. Relationships between Latchup Trigger (Holding) Voltage and Guard Ring Width

Fig. 12 shows the relationships between latchup trigger (holding) voltage and guard ring width for test structures A, B, and C with spacing (X) from anode to cathode of 19.6μm, 25.6μm, and 27.5μm,

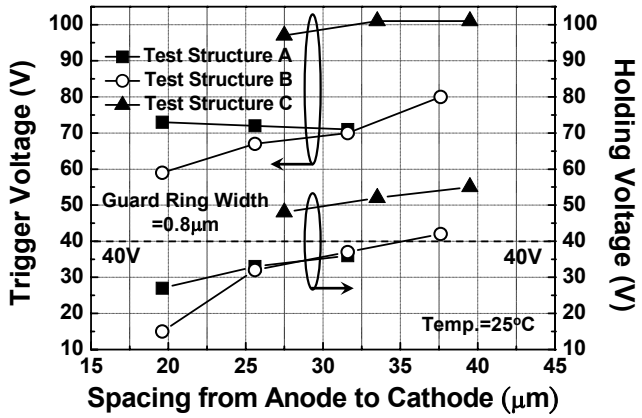


FIGURE 8. THE RELATIONSHIPS BETWEEN TLP-MEASURED LATCHUP TRIGGER (HOLDING) VOLTAGE AND SPACING FROM ANODE TO CATHODE FOR TEST STRUCTURES A, B, AND C.

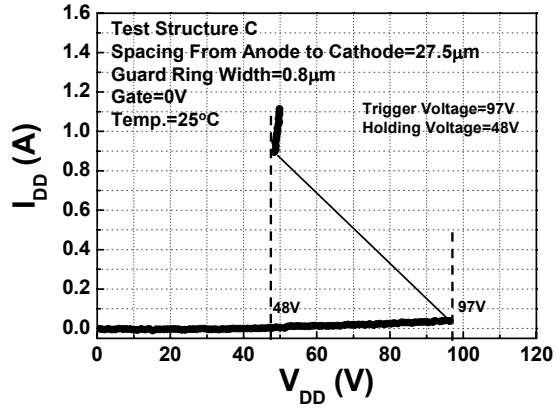


FIGURE 9. TLP-MEASURED LATCHUP I-V CHARACTERISTICS OF TEST STRUCTURE C WITH SPACING FROM ANODE TO CATHODE OF 27.5μm.

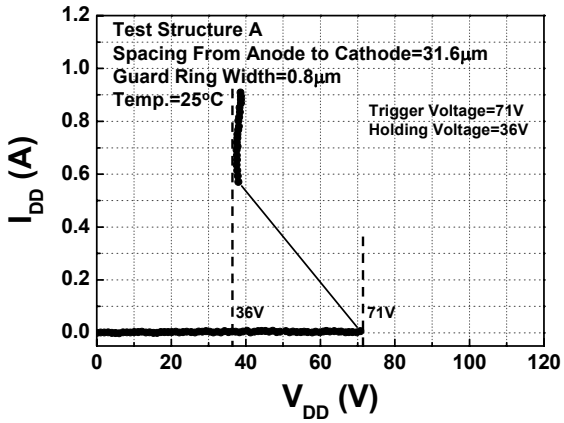


FIGURE 10. TLP-MEASURED LATCHUP I-V CHARACTERISTICS OF TEST STRUCTURE A WITH SPACING FROM ANODE TO CATHODE OF 31.6μm.

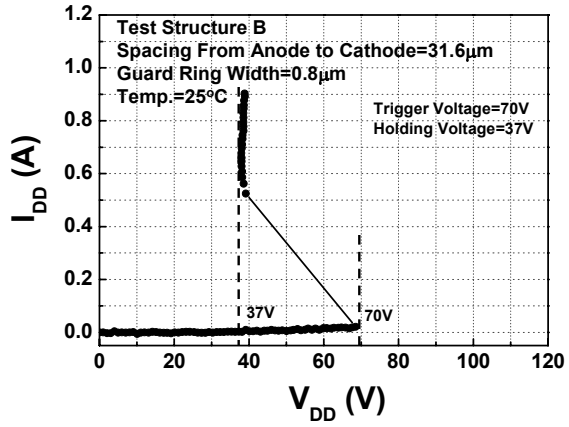


FIGURE 11. TLP-MEASURED LATCHUP I-V CHARACTERISTICS OF TEST STRUCTURE B WITH SPACING FROM ANODE TO CATHODE OF 31.6μm.

respectively. Increasing guard ring width can improve the latchup immunity of test structures A and B. For example, for test structure A (B) with guard ring width of 3μm, latchup trigger voltage and holding voltage can be enhanced up to 83V and 34V (74V and 35V), respectively. However, increasing guard ring width only has little improvement on latchup immunity of test structure C, because the dominant factor to improve latchup immunity is the isolation region of isolated HV NMOS in Fig. 1(a), but not the guard ring structure.

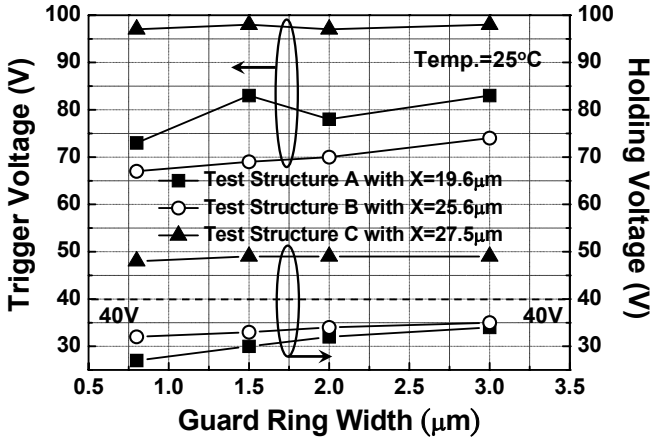


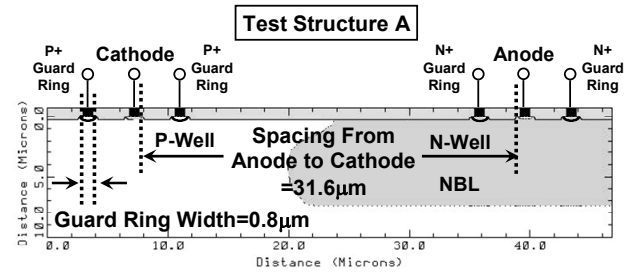
FIGURE 12. THE RELATIONSHIPS BETWEEN TLP-MEASURED LATCHUP TRIGGER (HOLDING) VOLTAGE AND GUARD RING WIDTH FOR TEST STRUCTURES A, B, AND C WITH THE PARAMETER "X" (SPACING FROM ANODE TO CATHODE) OF 19.6μm, 25.6μm, AND 27.5μm, RESPECTIVELY.

From the experimental results in Figs. 8 and 12, the isolation region in isolated HV NMOS is the dominant factor to enhance the latchup immunity in HV CMOS process. However, the symmetry of HV device structures has no great impact to improve the latchup immunity. Thus, SCR with isolated HV NMOS (test structure C) has better latchup immunity than that without isolated HV NMOS (test structures A and B). Increasing spacing from anode to cathode can improve the latchup immunity. However, it cannot help the test structure A (B), which considers the parasitic SCR resulting from non-isolated asymmetric (symmetric) HV NMOS and isolated asymmetric (symmetric) HV PMOS, to achieve the latchup-free purpose, even for a large spacing of 31.6μm from anode to cathode. Additionally, increasing guard ring width is a more efficient way to improve latchup immunity in the test structures A and B than that in test structure C.

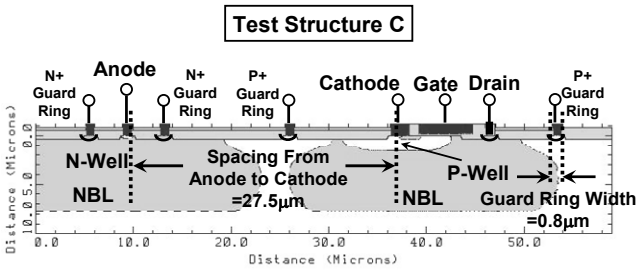
DEVICE SIMULATION

The experimental measured latchup characteristics of different HV test structures can be verified with 2-D device simulation. The device structure used in 2-D device simulation for test structure A (test structure C) with spacing from anode to cathode of 31.6μm (27.5μm) and with guard ring width of 0.8μm is shown in Fig. 13(a) (13(b)). To accurately verify the experimental results, these device structures for device simulation in Figs. 13(a) and 13(b) have the same layout parameters in the silicon test chips.

The simulated latchup I-V characteristics are shown in Fig. 14. Anode and N+ guard rings are connected to V_{DD}, whereas cathode and P+ guard rings are connected to GND. The simulation results in Fig. 14 are consistent with the measured results in Figs. 9 and 10 where test structure C has better latchup immunity (higher latchup trigger and holding voltage), even though there is a smaller (27.5μm) spacing from anode to cathode in test structure C. To further clarify this, the simulated 2-D current flow lines under latchup condition for test structures A and C are shown in Fig. 15(a) and 15(b), respectively. Compared with the test structure A which has the traditional p-n-p-n latchup path, the test structure C needs to overcome an additional NBL/P-well junction barrier to initiate latchup event. Such unique characteristics will lead to a higher latchup trigger or holding voltage, i.e. better latchup immunity, in the test structure C.



(a)



(b)

FIGURE 13. THE DEVICE STRUCTURES USED IN 2-D DEVICE SIMULATION FOR (A) TEST STRUCTURE A, AND (B) TEST STRUCTURE C. THE DEVICE STRUCTURES IN FIGS. 13(A) AND 13(B) HAVE THE SAME LAYOUT PARAMETERS IN THE SILICON TEST CHIPS.

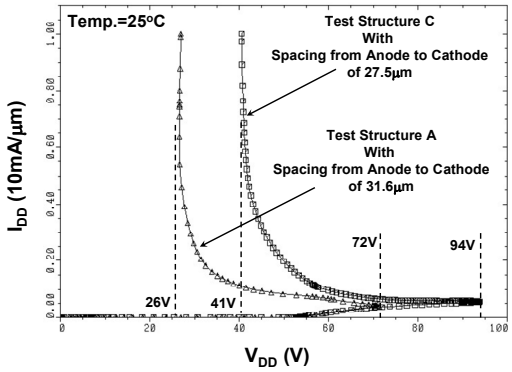
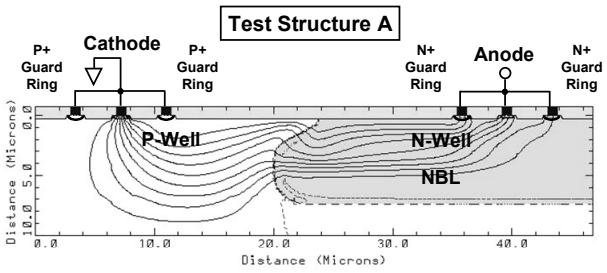


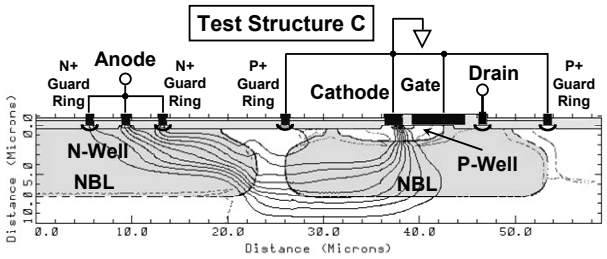
FIGURE 14. THE SIMULATED LATCHUP I-V CHARACTERISTICS FOR BOTH TEST STRUCTURES A AND C.

CONCLUSION

Latchup immunity in 0.25-μm 40-V CMOS process has been investigated with three different test structures under various layout parameters. In order to avoid HV test structures being damaged due to latchup-generated high power, the TLP generator with pulse width of 100ns and limited energy is used in this work to measure latchup I-V curves of different HV test structures. The isolation region in isolated HV NMOS is the dominant factor to enhance the latchup immunity in HV CMOS process. However, the symmetry of HV device structures has no great impact to improve the latchup immunity. The experimental measured latchup characteristics for different test structures in HV CMOS process have also been qualitatively and quantitatively verified with device simulation. The test structures and simulation methodology proposed in this work can be applied to extract safe and compact design rule for latchup prevention in HV CMOS ICs.



(a)



(b)

FIGURE 15. THE SIMULATED 2-D CURRENT FLOW LINES UNDER LATCHUP CONDITION FOR (A) TEST STRUCTURE A, AND (B) TEST STRUCTURE C.

REFERENCES

[1] H. Ballan and M. Declercq, *High Voltage Devices and Circuits in Standard CMOS Technologies*, Kluwer Academic, 1998.

[2] M.-D. Ker and K.-H. Lin, "The impact of low-holding-voltage issue in high-voltage CMOS technology and the design of latchup-free power-rail ESD clamp circuit for LCD driver ICs," *IEEE J. Solid-State Circuits*, vol. 40, pp. 1751–1759, Aug. 2005.

[3] M.-D. Ker and K.-H. Lin, "Double snapback characteristics in high-voltage nMOFETs and the impact to on-chip ESD protection design," *IEEE Electron Device Lett.*, vol. 25, no. 9, pp. 640–642, Sep. 2004.

[4] I.-C. Lin, C.-Y. Huang, C.-J. Chao, M.-D. Ker, S.-Y. Chuan, L.-Y. Leu, F.-C. Chiu, and J.-C. Tseng, "Anomalous latchup failure induced by on-chip ESD protection circuit in a high-voltage CMOS IC product," in *Proc. IPFA*, 2002, pp. 75–79.

[5] S. Gupta, J. Beckman, and S. Kosier, "Improved latch-up immunity in junction-isolated smart power ICs with unbiased guard ring," *IEEE Electron Device Lett.*, vol. 22, no. 12, pp. 600–602, Dec. 2001.

[6] Q. Huang, G. Amaratunga, E. Narayanan, and W. Milne, "Static CMOS latch-up considerations in HVIC design," *IEEE J. Solid-State Circuits*, vol. 25, pp. 613–616, Apr. 1990.

[7] J. C. Mitros, C.-Y. Tsai, H. Shichijo, K. Kunz, A. Morton, D. Goodpaster, D. Mosher, and T. R. Efland, "High-voltage drain extended MOS transistors for 0.18-μm logic CMOS process," *IEEE Trans. Electron Devices*, vol. 48, pp. 1751–1755, Aug. 2001.

[8] T. J. Maloney and N. Khurana, "Transmission line pulsing techniques for circuit modeling of ESD phenomena," in *Proc. EOS/ESD Symp.*, 1985, pp. 49–54.

[9] *IC Latch-up Test*, EIA/JEDEC Std. no. 78, 1997.