DEPENDENCE OF LAYOUT PARAMETERS ON CDE (CABLE DISCHARGE EVENT) ROBUSTNESS OF CMOS DEVICES IN A 0.25-μM SALICIDED CMOS PROCESS

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ABSTRACT

In this paper, the long-pulse transmission line pulsing (LP-TLP) system is proposed to simulate the influence of Cable Discharge Event (CDE) on integrated circuits. The layout dependence on CDE robustness of gate-grounded NMOS (GGNMOS) and gate-VDD PMOS (GDPMOS) devices has been experimentally investigated in detail. All CMOS devices with different device dimensions, layout spacings, and clearances have been drawn and fabricated in a 0.25-μm salicided CMOS process to find optimum layout rules for CDE protection. From the measured results, the CDE robustness of CMOS devices is much worse than their HBM ESD robustness.

INTRODUCTION

Cable discharge event (CDE) is a crucial reliability challenge in Ethernet integrated circuits because the high-energy discharge of CDE phenomenon could damage the connectors, the electronic equipments, and the Ethernet interfaces. Several universal organizations and corporations have commenced to discuss such CDE issues [1]-[3]. Most CMOS IC products are routinely tested by following the EIA/JEDEC Standard No.78 to evaluate latchup robustness. However, the CDE-induced latchup is a more serious condition [3]. Presently, there is still no established component-level standard for CDE tests [1]. Therefore, the long-pulse transmission line (LP-TLP) system is proposed in the paper as the effective measurement setup to investigate and analyze the CDE reliability of IC products.

Furthermore, to design area-efficient CDE protection circuits, the CDE robustness of protection devices is considered as strong as possible in per unit layout area. To optimize the layout area, the layout spacings are the major considerations [4] for designing strong CDE robustness devices. The main layout factors to affect the CDE level of CMOS devices are the channel width (W), the channel length (L), the finger width (Wf) of each finger, and the SAB width (note: the SAB layer is the silicide-blocking layer to block the silicided diffusion on the drain regions). In order to clearly compare the difference between the CDE level and the HBM ESD level, the proposed 500-ns/1000-ns long-pulse (LP) TLP and the conventional 100-ns TLP systems are used to find the dependence on layout parameters.

CABLE DISCHARGE TEST

In 2001, Telecommunication Industry Association (TIA) has reported the equipment to measure discharge waveforms of unshielded twisted pair (UTP) cables [2]. A human-body-model (HBM) ESD gun, following the IEC 61000-4-2 Standard, was used to inject an 8kV contact-discharge pulse into a conductor pair of an assortment of category 5, category 5e, or category 6 UTP cables with a length of 56m. After the UTP cables are charged, their pulse widths of discharge current waveforms have been mesaured approximately ~475ns [2]. This pulse width provides us a way to find the efficient component-level measurement method for investigating CDE robustness of I/O devices in IC products.

LONG-PULSE TLP MEASUREMENT SETUP

The transmission line pulsing (TLP) system was proposed to measure the secondary breakdown current (It2) of CMOS devices in 1985 [5]. By utilizing the characteristic of TLP system, the long-pulse TLP system is proposed to examine the robustness of the DUT under CDE stress. Fig. 1 sketches the measurement setup for the proposed LP-TLP test. The principle of LP-TLP operation is described as following. In the initial state, the switch SW1 is short-circuit and the switch SW2 is open-circuit. Through high-voltage resistance R_H, the high-voltage DC supply provides the long-pulse transmission line with a fixed voltage. The switch SW1 is open-circuit and the switch SW2 is short-circuit in the next state. The stored energy on the long-pulse transmission line transfers to the DUT by the electromagnetic wave, and then the current and voltage pulses on the DUT are measured by oscilloscope to obtain the first group data of the LP-TLP measured I-V curve. The foregoing procedures with increase of voltage charged in the transmission line are continuously duplicated until all I-V characteristics are measured. With the aid of LP-TLP system, the secondary breakdown point of semiconductor devices under CDE stress can be measured.

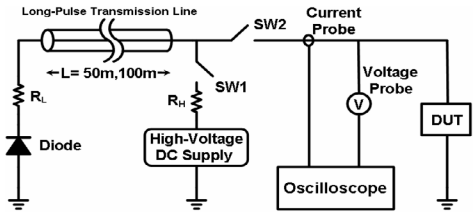

FIG. 1. THE MEASUREMENT SETUP FOR THE PROPOSED LONG-PULSE TLP (LP-TLP) TEST.

A 50-Ω resistor is used as the DUT to verify that the LP-TLP system can generate a long current pulse similar to cable discharge waveform. The measured 500-ns LP-TLP current waveforms are shown in Fig. 2. When the long-pulse transmission line is charged 450V, 640V, and 880V by the high-voltage DC supply, it can generate the corresponding LP-TLP currents of 6A, 9A, and 12A into the 50-Ω resistor at DUT, respectively. Furthermore, the pulse width of these three current waveforms is 500ns when the length of transmission line is 50m, so the proposed LP-TLP system with a long current pulse width has been proven. If the length of transmission line in the LP-TLP setup is 100m, the generated TLP waveform has a pulse width of 1000ns.

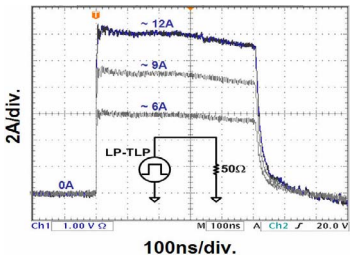

FIG. 2. THE LP-TLP CURRENT WAVEFORMS ON THE 50-Ω RESISTOR AT DUT UNDER DIFFERENT CHARGED VOLTAGES.

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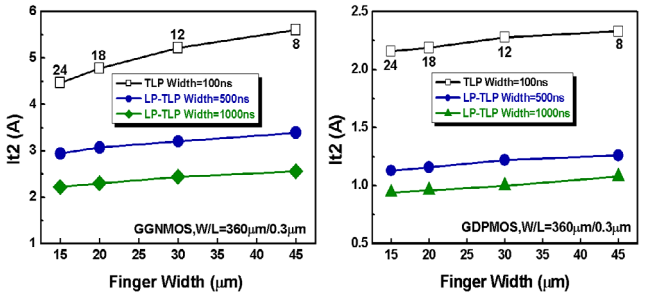
LAYOUT DEPENDENCE

A. FINGER WIDTH DEPENDENCE

In the I/O cell layout of CMOS ICs, a large-dimension device is traditionally drawn with multiple fingers in a parallel connection. If the finger width (Wf) of every finger is shorter, more fingers are used to form the large-dimension device. The large-dimension devices with different number of fingers and finger widths could cause different ESD and CDE performances, even though the devices have the same dimensions of channel width (W) and channel length (L). The more multiple fingers of a large-dimension device are hard to be uniformly turned on during ESD or CDE stresses, hence it may result in different ESD and CDE levels. To verify this issue, both GGNMOS and GDPMOS devices with the fixed channel width (W)/channel length (L) of 360μm/0.3μm but different finger widths are investigated under traditional 100-ns TLP test and 500-ns/1000-ns LP-TLP tests. The tested results are shown in Figs. 3(a) and 3(b).

From the experimental results, the It2 current of GGNMOS of W=360μm under traditional 100-ns TLP stress is decreased from 5.61A to 4.46A as the GGNMOS device is drawn with the finger number from 8 to 24. When the GGNMOS device is drawn with the finger number from 24 to 8, the It2 currents of the GGNMOS devices of W=360μm under the proposed 500-ns (1000-ns) LP-TLP stress are increased from 2.94A to 3.39A (2.22A to 2.56A). Similarly, the more finger number in the GDPMOS device leads to slightly lower ESD and CDE robustness. Moreover, the CDE robustness of GGNMOS and GDPMOS devices is much worse than their HBM ESD robustness under the same layout condition.



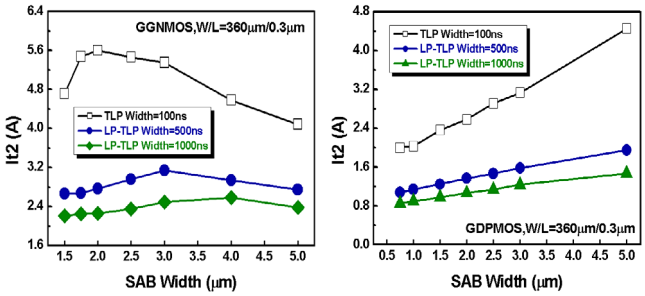
(a) (b)

FIG. 3. THE DENPENDENCE OF THE IT2 CURRENTS OF (a) GGNMOS AND (b) GDPMOS DEVICES ON FINGER WIDTH UNDER TRADITIONAL 100-NS TLP TEST AND THE PROPOSED 500-NS/1000-NS LP-TLP TESTS.

B. SAB WIDTH DEPENDENCE

The dependence of It2 currents of GGNMOS and GDPMOS devices on SAB width is shown in Figs. 4(a) and 4(b), respectively. The layout styles and clearances are all kept the same (W=360μm, L=0.3μm, Wf=30μm), but only the SAB width is different in this investigation. In Fig. 4(a), the It2 current of GGNMOS device under traditional 100-ns TLP stress is increased as the SAB width is increased from 1.5μm to 2μm. Because the silicide blocking on the drain region introduces ballast resistance, it could limit ESD currents to flow through the channel surface of MOSFET. On the contrary, while the SAB width is increased from 2μm to 5μm, the It2 current of GGNMOS devices under traditional 100-ns TLP test is decreased from 5.6A to 4.08A. Due to large increase of the SAB width (i.e. add too much silicide blocking), the power consumption along the ESD current path increases, resulting in a higher thermal stress and consequently a significantly lower It2 current. From the 100-ns TLP measured results, the maximum It2 current of GGNMOS is with the SAB width of 2μm. Under the proposed 500-ns/1000-ns LP-TLP tests, the It2 currents of GGNMOS are similar to the case under traditional 100-ns TLP test but with much lower current levels. However, the maximum It2 currents of GGNMOS under the 500-ns and 1000-ns LP-TLP tests are with the SAB width of 3μm and 4μm, respectively, as shown in Fig. 4(a).

In Fig. 4(b), the It2 currents of GDPMOS under traditional 100-ns TLP and the proposed 500-ns/1000-ns LP-TLP tests are all increased while the SAB width is increased from 0.75μm to 5μm. The phenomenon resulted from the existence of ballast resistance, which causes higher HBM ESD and CDE robustness. From the experimental investigations, it is evident that the GGNMOS and GDPMOS protection devices are very weak to withstand such CDE-induced high energy.



(a) (b)

FIG. 4. THE DENPENDENCE OF THE IT2 CURRENTS OF (a) GGNMOS AND (b) GDPMOS DEVICES ON SAB WIDTH UNDER TRADITIONAL 100-NS TLP TEST AND THE PROPOSED 500-NS/1000-NS LP-TLP TESTS.

CONCLUSION

A LP-TLP system with long pulse widths of 500ns and 1000ns is proposed to investigate the reliability of CDE on IC products. The It2 current of CMOS devices can be measured by the proposed LP-TLP system. Furthermore, the dependence of layout spacings on the CDE levels of CMOS devices in a salicided CMOS process has been experimentally investigated in more details. From the measured results, they can provide us with one set of optimized design rules for chip layout in IC products to sustain CDE stress in a given CMOS process.

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