Dummy-Gate Structure to Improve ESD Robustness in a Fully-Salicided 130-nm CMOS Technology without Using Extra Salicide-Blocking Mask

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Abstract

NMOS with dummy-gate structure is proposed to significantly improve electrostatic discharge (ESD) robustness in a fully-salicided CMOS technology. By using this structure, ESD current is discharged far away from the salicided surface channel of NMOS, therefore the NMOS can sustain a much higher ESD level. The HBM (MM) ESD robustness of the NMOS with dummy-gate structure (W/L = 480 μm/0.18 μm) has been successfully improved from 0.5 kV (125 V) to 1.5 kV (325 V) in a 130-nm fully-salicided CMOS process. Under the same layout area of the gate-grounded NMOS (ggNMOS), HBM (MM) ESD level can be improved over 300% (260%) by the proposed dummy-gate structure. The proposed dummy-gate structure is fully process compatible to general salicided CMOS processes without additional mask, which is very cost-efficient for application in the IC products.

1. Introduction

In deep-sub-micron salicided CMOS technology, the MOSFET is fabricated with salicidation process to improve circuit performance. Salicidation process reduces the sheet resistance of drain/source of MOSFET, but its ESD robustness is dramatically degraded.

Owing to insufficient ballast resistance of MOSFET with salicided process, the ESD discharging current is crowding within the salicided layer to cause non-uniform turn-on issue in ESD protection devices [1], [2]. Several experimental results have proven and suggested to enlarge the clearance from drain contact to poly-gate edge (SDG) of MOSFET for better ESD robustness [2], [3]. To improve ESD robustness, some CMOS processes provide the extra salicide blocking mask to modify the ESD protection NMOS of I/O circuits without the salicided structure. However, the salicide blocking method needs an extra mask and process procedures which will increase fabrication cost. In the prior art, dummy-gate structure with N-well resistors had been reported to improve ESD robustness without extra mask in 0.25-μm and 0.18-μm CMOS processes [4], [5]. However, the effectiveness of this method should be further investigated in the nano-scale CMOS process, such as sub-130 nm CMOS process.

Component-level ESD stresses on IC products had been classified as three models [6]: the human-body model (HBM) [7], [8], the machine model (MM) [9], [10], and the charged device model (CDM) [11]. The ESD voltage ratio between the HBM and MM ESD robustness of CMOS IC products were around ~10 in the submicron (1.0 ~ 0.5 μm) CMOS processes [12], [13]. Typically, a CMOS IC product, which has a HBM ESD robustness of 2 kV, can sustain a MM ESD robustness of 200 V. However, this ratio has been approached to about 15 ~ 20 in the deep-sub-micron fully-salicided CMOS processes [14]. The CMOS IC fabricated in the sub-130 nm CMOS processes can be designed to still have a high HBM ESD robustness, but it becomes more difficult to have a high enough MM ESD level. How to effectively improve MM ESD robustness of IC products has become a challenge in the sub-130 nm CMOS processes.

2. HBM and MM ESD current waveforms

The real ESD discharging current waveforms of HBM and MM ESD stresses through the gate-grounded NMOS (ggNMOS) are measured to compare the difference. The experimental setup to measure the current waveforms during ESD test is illustrated in Fig. 1, where the digital oscilloscope with current probe is used to measure the ESD transient currents in time domain. The actual ESD current waveforms flowing through the ggNMOS with a device dimension of W/L = 300 μm/0.5 μm under 4-kV HBM and 400-V MM ESD stresses are measured and shown in Figs. 2 and 3, respectively.

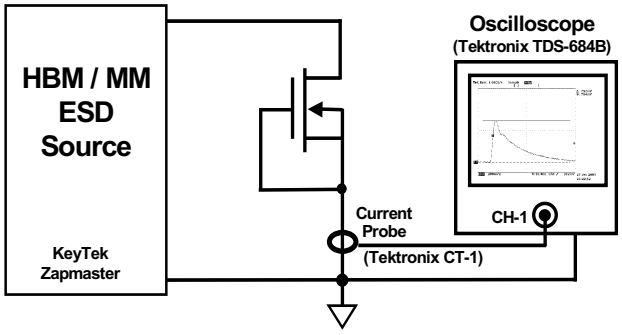

Figure 1. The experimental setup to measure the ESD transient current waveforms during ESD test.

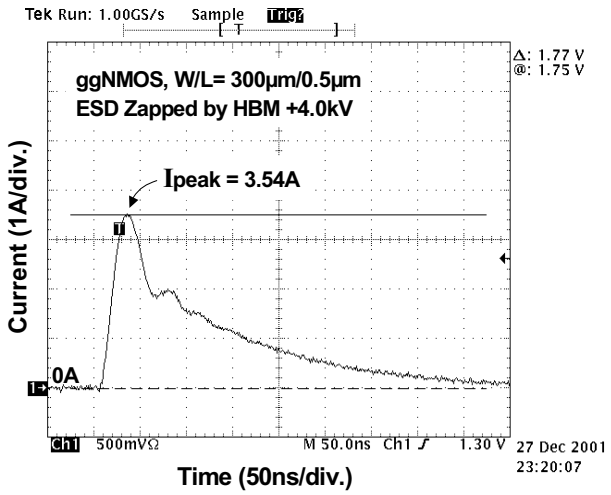

Figure 2. The measured ESD discharging current waveform through the ggNMOS, which is zapped by 4-kV HBM ESD voltage.

The current peak of 4-kV HBM ESD stress in Fig. 2 is 3.54 A, whereas that of 400-V MM ESD stress in Fig. 3 is as high as 4.94 A. As comparing these two ESD current waveforms, the MM ESD stress has a much higher ESD current peak within a shorter current pulse width. This implies that the MM ESD events generate more heat in a shorter time period to burn out the device, and therefore cause a much lower ESD robustness. MM ESD protection has become more difficult than HBM in sub-130 nm fully-salicided CMOS processes. How to effectively improve MM ESD robustness of IC products has become a challenge in the nano-scale fully-salicided CMOS processes. In this work, NMOS with dummy-gate structure is proposed to significantly improve machine-model (MM) electrostatic discharge (ESD) robustness in 130-nm fully-salicided CMOS technology without additional salicide blocking mask [15].

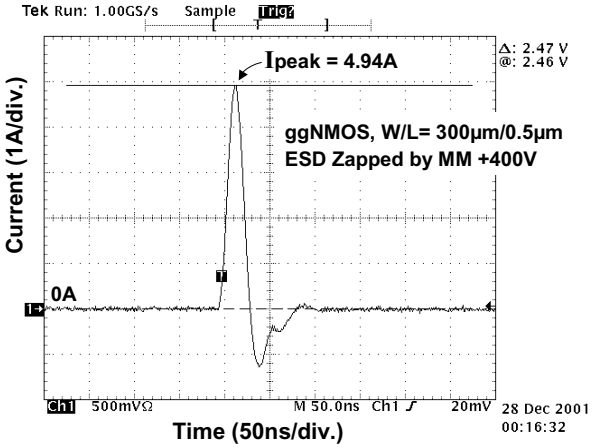

Figure 3. The measured ESD discharging current waveform through the ggNMOS, which is zapped by 400-V MM ESD voltage.

3. ESD device structure

In deep-sub-micron CMOS technology, the NMOS is fabricated with salicidation process to improve circuit performance as shown in Fig. 4. However, due to current crowding issue, salicidation process degrades ESD robustness of ggNMOS dramatically.

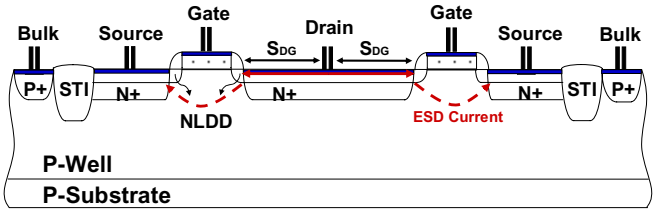

Figure 4. Cross-sectional view of the traditional fully-salicided NMOS transistor.

To significantly improve ESD robustness of ESD protection NMOS of I/O circuits without extra mask and processes, NMOS with dummy-gate structure is proposed in Fig. 5. In Fig. 5, the dummy-gate structure blocks the salicidation region in the drain side of NMOS transistor, and an N-well covers the drain side to increase the ballast resistance.

When a positive ESD voltage is applied to the pad with the VSS relatively grounded. The salicided drain region of NMOS is blocked by the dummy-gate structure, therefore the ESD current is discharged far away from the weakest salicidation layer of NMOS. On the other hand, the drain region of NMOS, which is covered by the N-well structure, has a lager drain ballast resistance. Therefore, the multiple fingers of NMOS can be uniformly triggered on. So, the ESD robustness of NMOS can be effectively improved.

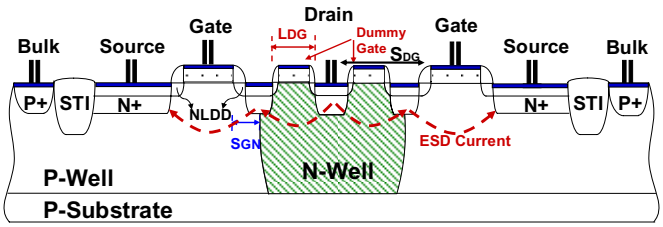

Figure 5. Cross-sectional view of the proposed NMOS with dummy-gate structure.

4. Experimental results

The second breakdown current (It2), human-body-model (HBM) ESD level, and machine-model (MM) ESD level are measured to investigate ESD robustness of the fabricated MOSFET devices. The I-V curves and second breakdown current (It2) of the fabricated MOSFET devices are measured by the transmission line pulse (TLP) generator with a pulse width of 100ns to verify ESD robustness of devices. The ESD failure criterion of devices is defined, as the leakage current is greater than 1μA under the VDD bias of 1.2V for 1.2-V MOSFET devices. The HBM and MM ESD levels are measured by a *ZapMaster* ESD tester to compare ESD robustness of those test devices.

4.1 TLP I-V characteristics

Fully-salicided NMOS and the proposed NMOS with dummy-gate structure were drawn with the same device dimension (W/L = 480 μm/0.18 μm) in a 130-nm fully-salicided CMOS process. To simplify compare the ESD robustness of fully-salicided NMOS and dummy-gate NMOS, the layout spacing from the drain contact to poly gate (S_{DG}, which is indicated in Figs. 4 and 5) is fixed at 2.15 μm in the experimental test chips. The design parameters of dummy-gate NMOS, S_{GN} (spacing between gate and Nwell) is 0.2 μm, and L_{DG} (dummy gate length) is 1.25 μm. The It2 of the fully-salicided NMOS is below 0.1 A, but that of the NMOS with dummy-gate structure can be significantly improved up to 1.08 A, as shown in Fig. 6.

4.2 ESD test results

These two kinds of ggNMOS devices are also verified by the ESD tester under both HBM and MM ESD stresses. The ESD failure threshold (ESD level) is defined at the minimum voltage level of ESD stress that causes I-V curve of the device having 30 % voltage shift at 1 μA. The It2, HBM, and MM ESD levels of these two kinds of ggNMOS are compared in Table I. The HBM ESD robustness of fully-salicided NMOS is below 0.5 kV, but that of NMOS with dummy-gate is improved to 1.5 kV. MM ESD level of fully-salicided ggNMOS is only 125 V. However, MM ESD level of the NMOS with dummy-gate structure is improved to 325 V. Under the same layout area of the ggNMOS, the HBM (MM) ESD level can be improved over 300% (260%) by the proposed dummy-gate structure. HBM/MM ESD ratio of the dummy-gate NMOS is kept at 4.6, which is smaller than the typical value of ~10.

From the experimental results, TLP-measured It2 is consistent with that verified by ESD tester. The ESD robustness of NMOS device has been significantly improved by the proposed dummy-gate structure in a 130-nm fully-salicided CMOS process.

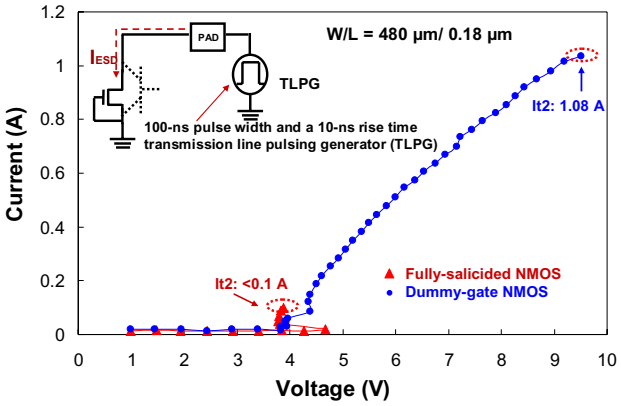

Figure 6. TLP-measured I-V curves of ggNMOS with the fully-salicided and dummy-gate structure.

Table 1.
HBM, MM ESD levels, and It2 of two kinds of ggNMOS transistors

ggNMOS	HBM (kV)	MM (V)	It2 (A)
Fully-salicided NMOS	<0.5	125	<0.1
NMOS with Dummy-Gate structure	1.5	325	1.08

4.3. Failure analysis

In order to clarify the failure locations in these NMOS devices, some failures on these zapped devices has been observed by the optical microscopy (OM). The test chips after ESD stress are decapitated. The top layers including BPSG, metal, poly, and oxidation layer are all removed to substrate layer by chemical processes.

Comparing optical microscopy (OM) pictures of

fully-salicided NMOS and NMOS with dummy-gate structure under MM ESD stress are shown in Figs. 7 and 8, respectively. The failure regions of fully-salicided NMOS after 125-V MM ESD stress are only located within a few gate regions, which is due to current crowding within the weak salicided surface channel. However, the failure regions of NMOS with dummy-gate structure after 325-V MM ESD stress are uniformly located among all the contact regions of drain side. Therefore, MM ESD robustness of transistor with the proposed dummy-gate structure is better than that of fully-salicided structure.

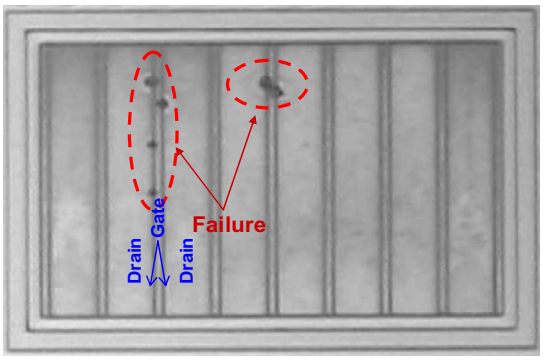

Figure 7. Failure analysis picture of fully-salicided NMOS transistor after 125-V MM ESD stress.

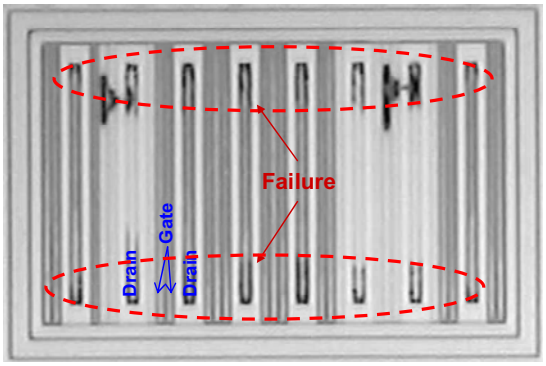

Figure 8. Failure analysis picture of NMOS with dummy-gate structure after 325-V MM ESD stress.

5. Conclusion

NMOS with dummy-gate structure used to significantly improve ESD robustness has been practically verified in a 130-nm CMOS process. Moreover, HBM/MM ESD ratio of ggNMOS is successfully kept at 4.6 by dummy-gate structure. The dummy-gate structure, which is process compatible to general fully-salicided CMOS processes without any additional mask, is very cost-efficient for application in the IC products to improve their ESD robustness.

6. References

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