ASIC with Interpolator for Incremental Optical Encoders

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Abstract

Optical encoders are commonly used in modern positioning systems. The accuracy and resolution of the optical encoder is always restricted by generated sinusoidal signals and the assembly technique. The interpolation circuit and conditional circuit in the optical sensor are preferably integrated into the integrated circuit (IC) to maximize the signal-to-noise-ratio (SNR). Nowadays, system-on-a-chip (SOC) is popular device to minimize the circuit and the cost to the manufacturer of making it. This study presents an ASIC including a conditional circuit for optical signal and a 10-fold interpolation circuit for improving the resolution of optical encoder. Furthermore, an electrical method of reducing the assembly difficulties is proposed. The ASIC is fabricated in a 0.5 μm 2P2M CMOS process.

1. Introduction

The incremental optical encoders usually serve as feedback apparatus in typical positioning systems. Figure 1 shows the structure of a typical linear incremental optical encoder [1]. The light source, index scale and photo-detectors are mounted together on movable reading head. The light source passes through main scale and the index scale, and illuminates the photo detectors. The interaction between the main and the index gratings enables the four detectors to generate two pairs of phase-shifted sinusoidal currents, which are arranged to improve common mode rejection ratio (CMRR). The current signals are always conditioned to two sinusoidal signals with 90 degrees phase shift by trans-impedance amplifier [2]. However if the main scale, index scale and photo detectors are misaligned in the assembly process, then the sinusoidal signals are not exactly orthogonal. The accuracy of the encoder is deteriorated, and the orthogonal error can be compensated for in many ways [3], [4].

Typically, the two sinusoidal signals are digitized as two trains of square signals phase-shifted 90 degrees. The square signals divide the sinusoidal signals into four equal-phase-distances. The encoder is improved by a factor of four. However, the 4-fold improved resolution is still poor in most positioning systems. The interpolation circuit is used to improve the resolution of the encoder. Many ways to interpolate the scaling signals exist, and the resistor string phase shift method is commonly used [5]-[7].

This paper proposed an ASIC with 10-fold interpolator for an incremental optical encoder. The resistor string phase shift method was applied to design a 10-fold interpolator and a conditional circuit that allows phase difference adjustment were also integrated. The ASIC was fabricated in a 0.5 μm 2P2M CMOS process. Four key components, conditional circuit, resistor strings, comparators and logic circuit, were verified individually. In addition, the entire chip verification proceeded by feeding quadrature signals with variable frequencies. Finally, the practical test of an optical encoder with interpolation ASIC was performed.

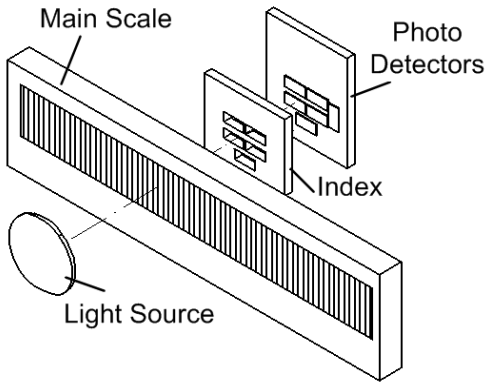


Fig. 1: Structure of a typical linear incremental optical encoder.

2. Conditional Circuit

Figure 2 presents a functional block diagram of the proposed ASIC. The two pairs of differentially scaling sinusoidal currents, I_0-I_{180} and I_{90}-I_{270} are generated from an optical encoder. The subscripts indicate the current phase. Consequently, the conditional circuit with phase-adjusting circuit transfers two pairs of differentially scaling sinusoidal currents into two position-dependent sinusoidal signals, sinθ and cosθ. Finally, the two sinusoidal signals are digitized as two trains of square signals, A and B, phase-shifted by 90 degrees using a 10-fold interpolator.

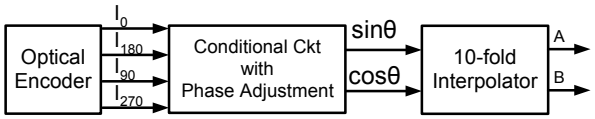


Fig. 2: Functional block diagram of the proposed ASIC.

Figure 3 shows the conditional circuit consisting of trans-impedance and differential amplifiers.

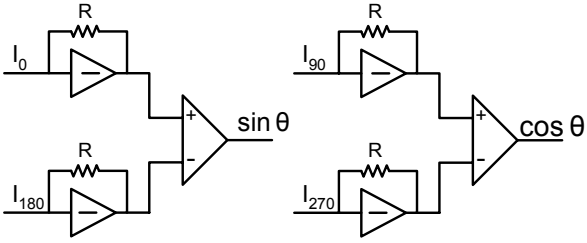


Fig. 3: Conditional circuit for incremental optical encoder.

The phase of the sinusoidal signals is proportional to the position in a grating period on the main scale, so, the conditional circuit should be designed with a wider bandwidth to avoid delays of the sinusoidal signals.

Additional, the slew rate of the conditional circuit should be high enough, else the quadrature signals will be shaped and cause the performance of the interpolator to decay. For a sinusoidal signal $A\sin\theta$, the maximum slew rate is given by,

$$SR_{\max} = 2\pi C f_{\max} \tag{1}$$

where C is the amplitude of the input sinusoidal signal and $f_{\max}$ is the maximum frequency of the sinusoidal signal.

A two-stage CMOS operational amplifier was designed for the conditional circuit to yield a wide bandwidth and high slew rate. The first stage is a p-channel differential input pair with an n-channel current-mirror active load. The second stage is a push-pull output stage for driving resistive loading in 10-fold interpolator.

3. Phase Adjustment

A high-quality orthogonal signal is required for high-fold interpolation. Unfortunately, the phase shift between the scaling sinusoidal signals always deviates from 90 degrees, because of the inconsistency of the properties of the photo detectors and the assembly errors. A method of adjusting the phase is proposed. Assuming that the input non-orthogonal sinusoidal signals are sinθ and cos(θ±φ), φ is the leading or lagging phase error. For the cos(θ±φ) signal, it is represented as,

$$\cos(\theta \pm \varphi) = \cos\theta\cos\varphi \mp \sin\theta\sin\varphi \tag{2}$$

Then

$$\cos\varphi\cos\theta = \cos(\theta \pm \varphi) \pm \sin\varphi\sin\theta \tag{3}$$

From Eq. (3), an amplitude-reduced orthogonal signal cosφcosθ is obtained by adding the original signal cos(θ±φ) to an amplitude-reduced signal sinφsinθ. Figure 4 shows the circuit. The relationship between output and input is

$$\begin{aligned} &\cos\varphi\cos\theta \\ &= \frac{R_7}{R_3}\cos(\theta \pm \varphi) + \left(\frac{R_7}{R_2} - \frac{R_7}{R_1}\right)\sin\theta \\ &= \cos(\theta \pm \varphi) \pm \sin\varphi\sin\theta \end{aligned} \tag{4}$$

If R_2=R_3=R_7 then

$$R_1 = \frac{R_7}{1 \mp \sin\varphi} \tag{5}$$

Only a resistor is required to adjust the phase difference between the input sinusoidal signals, and the constant phase error is thus corrected. The phase adjustment method is also integrated into the conditional circuit and an off-chip adjustable resistor is designed for manual phase adjustment.

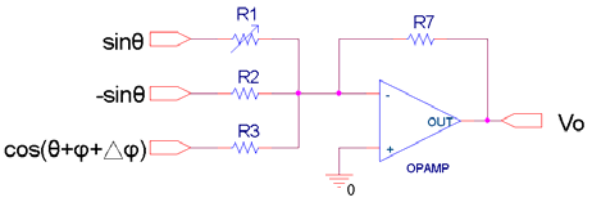


Fig. 4: Circuit for realizing the phase adjustment of sinusoidal signals.

4. Resistor String

Figure 5 shows the functional block of a 10-fold interpolator using the resistor string phase shift method. The resistor strings are a set of non-linear ratio resistors, which shift the input sinusoidal signals into several phase-shifted sinusoidal signals. The zero crossings of the sinusoidal signals divide the input signals into equal phase-distances. The second stage is a set of regenerative comparators, which digitize the sinusoidal signals with equal phase-distance. Then, the digitized signals are decoded by logic circuitry into two trains of square signals, A and B, with high resolution to a positioning system.

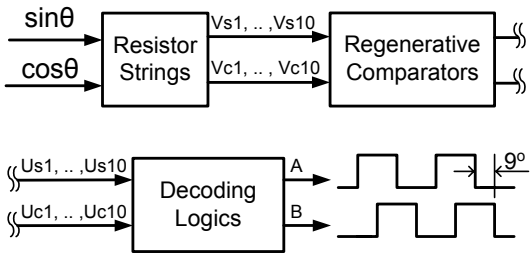


Fig. 5: Functional block of 10-fold interpolator.

For the designed 10-fold interpolator, two sets of 9° phase difference sinusoidal signals, V_{s1}~V_{s10} andV_{c1}~V_{c10}, should be employed. As shown in Fig. 6, two sets of serial resistor are used in the 10-fold interpolator, they have the following relationship,

$$R_{s,k} = \frac{R_s}{1 + \cos\varphi_k / \sin\varphi_k} \qquad k = 1 \sim 9 \qquad (6)$$

$$R_{c,k} = \frac{R_c}{1 + \cos\varphi_k / \sin\varphi_k} \qquad k = 1 \sim 9 \qquad (7)$$

The terminal voltages of the resistor string , V_{sk} and V_{ck}, are written as,

$$\begin{aligned} V_{sk} &= \frac{(R_s - R_{s,k})}{R_s} \times \sin\theta + \frac{R_{s,k}}{R_s} \times \cos\theta \\ &= A_{sk} \sin(\theta + \varphi_k) \qquad k = 1 \sim 9 \end{aligned} \qquad (8)$$

$$\begin{aligned} V_{ck} &= \frac{(R_c - R_{c,k})}{R_c} \times \cos\theta - \frac{R_{c,k}}{R_c} \times \sin\theta \\ &= A_{ck} \cos(\theta + \varphi_k) \qquad k = 1 \sim 9 \end{aligned} \qquad (9)$$

where $R_s = R_{s1} + \ldots + R_{s10}$, $R_c = R_{c1} + \ldots + R_{c10}$, $R_{s,k} = R_{s1} + \ldots + R_{sk}$, $R_{c,k} = R_{c1} + \ldots + R_{ck}$. A_{sk} and A_{ck} are the reduced amplitudes of the phase shifted sinusoidal signals and φ_k is the shifted phase, which divides the input sinusoidal signals into equal phase-distances, i.e. 9 degrees in 10-fold interpolator.

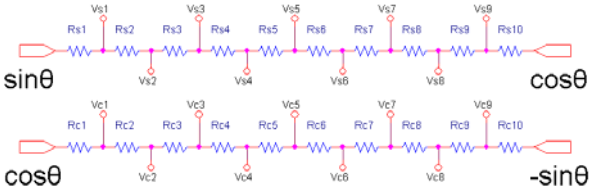


Fig. 6: Non-linear resistor strings of 10-fold interpolator.

The ratios of resistor strings R_{sk} and R_{ck} are identical. Table 1 shows the resistance ratios of 10-fold interpolator. R_k represnts R_{sk} and R_{ck}.

Table 1. Resistance ratios for 10-fold interpolator.

R1	R2	R3	R4	R5
1.7265	1.3702	1.1656	1.0515	1
R6	R7	R8	R9	R10
1	1.0515	1.1656	1.3702	1.7265

In the CMOS process, the matching behavior of the resistors is affected by several parameters, including the spread sheet resistance, lithographical errors, etching errors, bend effects, contact resistance and alignment errors [8]. The layout of resistor strings is proposed and measured. The poly resistor is used in the resistor strings to yield good resistor ratio.

A layout in which no contacts are used in the current path, although the end of the resistor string is fabricated and measured, is employed to reduce the contact resistance [9]. As shown in Fig. 7, a long poly resistor string is used and the distance between the contacts is directly proportion to the ratio R_1~ R_{10}. The contacts V_{s1} ~ V_{s9} are not in the current path; therefore, the error due to variations in the contact resistance is eliminated. Moreover, each terminal that is interconnected by two symmetrical contact arrays reduces the interconnect resistance and the time constant.

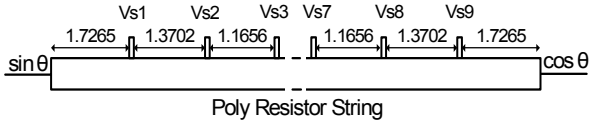


Fig. 7: Layout of resistor string of 10-fold interpolator.

5. Regenerative Comparator

Comparators are usually used to convert input signals into an output signal with abrupt edges. If the response time of the comparator is much faster than the input signal near the threshold level in a noisy environment, then, the comparator output chatters between two stable levels. Quadrature signals from optical encoders are usually slow and noisy, thus, positive feedback in the comparator is usually applied to eliminate the chattering effects. As shown in Fig. 8, the hysteresis voltage of the regenerative comparator is defined as,

$$V_H = V_{t+} - V_{t-} \qquad (10)$$

where V_{t+} and V_{t-} are the positive and negative threshold voltages of the regenerative comparator, respectively. The larger hysteresis voltage corresponds to better anti-noise capability. A phase delay appears when the regenerative comparator is applied. For a hysteresis voltage V_H, the phase delay

can be derived as,

$$phase\ delay = \sin^{-1}\left(V_H / 2C\right) \qquad (11)$$

In designing the regenerative comparator, the compromise between the anti-noise ability and the phase delay should considered.

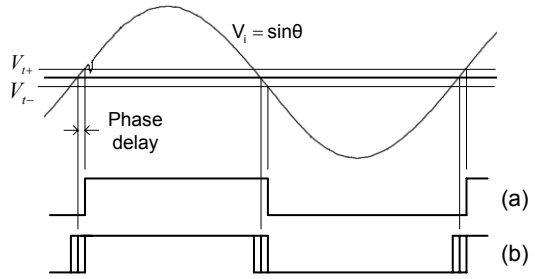


Fig. 8: Response of a fast comparator to a slow signal in a noisy environment: (a) with hysteresis; (b) without hysteresis.

6. Experimental Results and Discussion

Figure 9 shows the photograph of the proposed ASIC with a 10-fold interpolator.

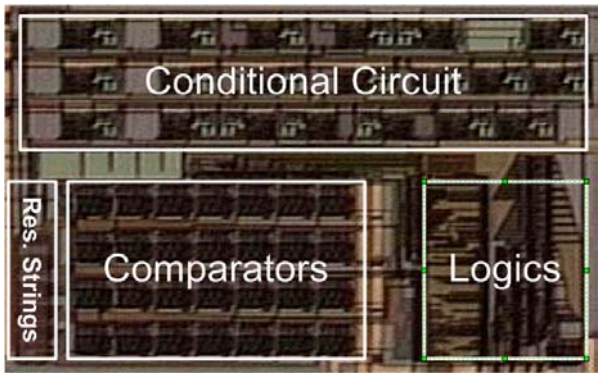


Fig. 9: Photograph of the proposed ASIC with a 10-fold interpolator.

6.1 Amplifier in conditional circuit In a modern positioning system, both the 300 kHz maximum frequency response and a 2V/μs slew rate are required. Figure 10 shows the circuit for testing on the amplifier. The test signal, VIN, was fed into the circuit, and the response, VOUT, was measured. Figure 11 shows the phase delay between the input and output of the differential amplifier, which is maintained below 2.1 degrees when the frequency is lower than 300 kHz. The slew rate of the two-stage amplifier is measured by applying a step input from 5V to 0V. The measured slew rate, plotted in Fig. 12, is 43V/μs. Both the bandwidth and the slew rate meet the requirements of a conditional circuit.

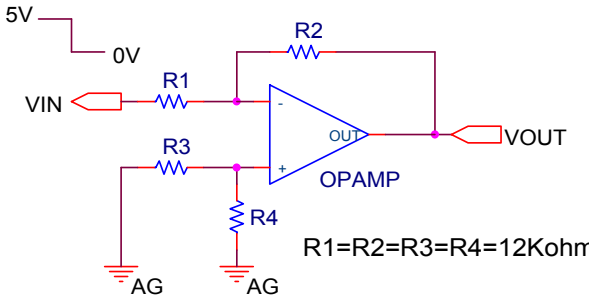


Fig. 10: Circuit for testing a two-stage amplifier used in a conditional circuit.

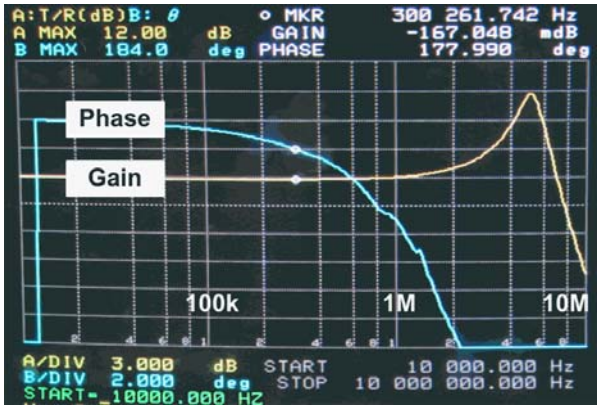


Fig. 11: Frequency response of the two-stage amplifier.

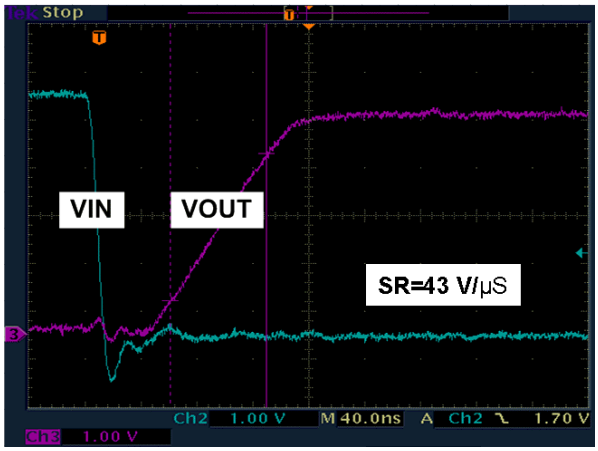
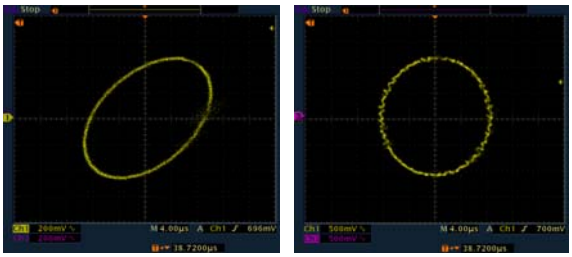


Fig. 12: Measured slew rate of the two-stage amplifier.

6.2 Phase Adjustment Circuit The phase adjustment circuit is used to adjust the phase difference between the input quadrature signals from optical encoder, and thereby improve the accuracy of the encoder. Figures 13(a) and 13(b) show the Lissajous pattern of the quadrature signals before and after the phase adjustment circuit respectively. The pattern becomes a circle after the adjustments are mode; that is the quadrature signals are shifted to obtain a 90 degrees phase difference.



(a) (b)

Fig. 13: Lissajous pattern of the (a) input non-orthogonal quadrature signals. (b) adjusted input quadrature signals after adjustment of phase.

6.3 Resistor Strings A set of resistor strings for a 10-fold interpolator is fabricated in a poly resistor with the layout discussed previously. Equation (12) defines the integral nonlinearity (*INL*) of an interpolator, and the definitions of both V_{ck} and V_{sk} are the same.

$$INL \quad of\, V_{sk} = P_{mk} - P_{ik} \tag{12}$$

where P_{mk} and P_{ik} are the measured and ideal shifted phases of signal V_{sk} respectively. The ideal phase distance after 10-fold interpolation is 9 degrees. Figure 14 plots the *INL* and *DNL* of the resistor string, respectively. The *INL* is under one degree, i.e. the error on one ideal phase distance is only 11%.

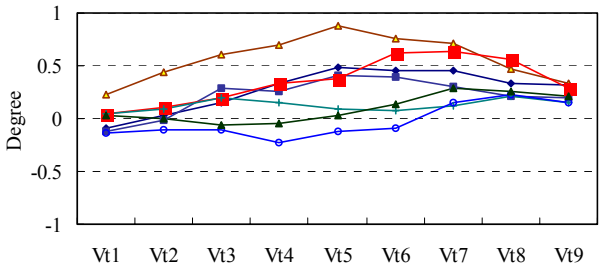


Fig. 14: *INL of* the resistor string.

6.4 Regenerative Comparator Figure 15 plots the measured typical hysteresis input-output curve, where V_i , V_o, V_H and V_{off} are the input voltage difference, output voltage, hysteresis voltage and input offset voltage of the regenerative comparator, respectively. The values of V_H and V_{off} on the five chips are measured and shown in Table 2. In this test, the deviation of V_i is less than 6 mV. The table also shows the corresponding induced phase delays calculated from Eq. (11) when C=1V. The largest phase delay is only 1.7 degrees.

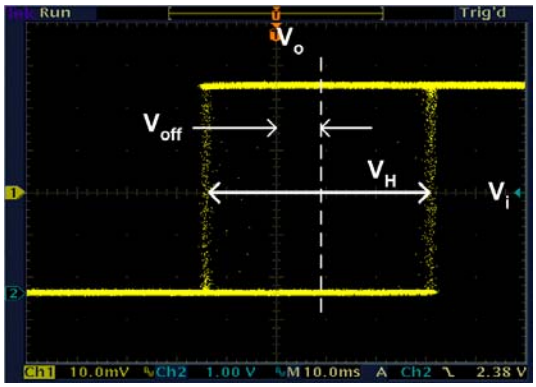
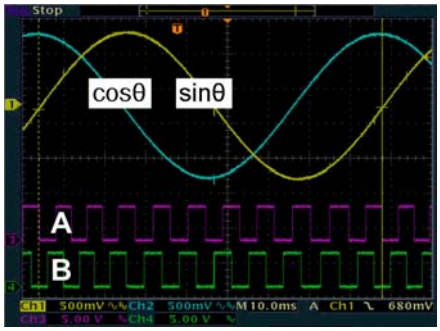


Fig. 15: Designed CMOS comparator with hysteresis.

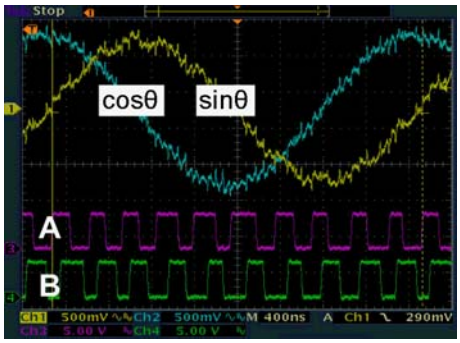
Table 2. Measured V_H and V_{off} for five chips.

Chip	#1	#2	#3	#4	#5
Voff (mV)	-0.2	3.6	4.1	-5.8	-4
V_H (mV)	53.2	51.2	59.4	54	56
Phase delay (degree)	1.52	1.47	1.70	1.55	1.60

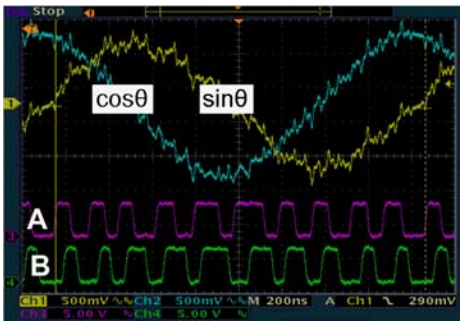
6.5 Whole chip test given ideal quadrature signal input As shown in Fig. 16, the interpolated square signals of whole chip were measured at 12Hz, 290 kHz and 584 kHz ideal quadrature signal inputs. The two trains of square signals, A and B, are still available given a 584kHz signal input.



(a) 12 Hz



(b) 290 kHz



(c) 584 kHz

Fig. 16: Input and output waveforms of tested ASIC given (a) 12 Hz (b) 280 kHz and (c) 584 kHz ideal quadrature input signals.

6.6 Whole chip test using optical encoder A test is conducted by adapting the ASIC on an incremental optical encoder. Figure 17 plots the input and output waveforms of tested ASIC given 85 Hz quadrature signals input from a practical incremental encoder. Two trains of square signals, A and B, are clear and easily distinguishable.

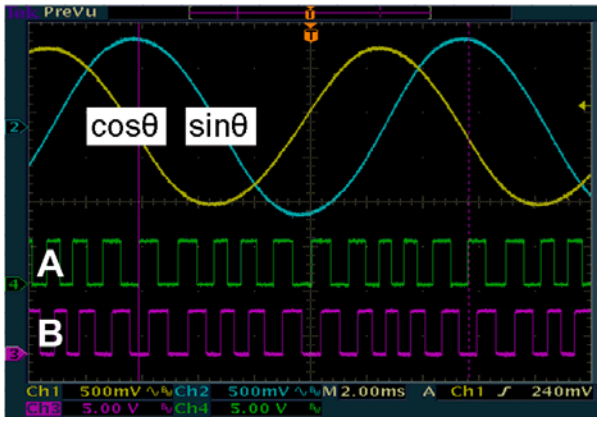


Fig. 17: Input and output waveforms of tested ASIC using 85 Hz quadrature signals, input from a practical incremental encoder

7. Conclusion

A complete ASIC integrated the 10-fold interpolator and a phase-adjusting circuit was designed and fabricated in a 0.5 μm double-poly / double-metal CMOS process. The amplifiers in the conditional circuit were tested, and the 300 kHz maximum frequency response and the 43V/μs slew rate were measured. The *INL* of resistor strings is less than one degree; that is, the error of one ideal phase distance is only 11%.

When the entire chip was tested at an ideal quadrature signal input, two trains of square signals were still available using a 584kHz signal input. Finally, the entire chip was tested using quadrature signals input from an incremental encoder. Two trains of square signals are clear and easily distinguishable.

8. Acknowledgment

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