Design on LVDS Receiver with New Delay-Selecting Technique for UXGA Flat Panel Display Applications

Ming-Dou Ker and Chien-Hua Wu
Nanoelectronics and Gigascale Systems Laboratory, National Chiao-Tung University, Hsin-Chu, Taiwan, mdker@ieee.org

***Abstract*—A LVDS receiver with new data recovery design for flat-panel-display (FPD) link is presented. The new delay-selecting technique is used in LVDS receiver to reduce the circuit complexity and to save chip power for cost-efficient applications. The proposed LVDS receiver with an operation data rate of 1.25 Gb/s has been successfully verified in a 0.13-μm CMOS process, which can fully support the operation of FPD link with UXGA resolution.**

I. Introduction

As the process technologies are continually scaled down, the on-chip data rate moves faster than the off-chip data rate. As the result, the interface between chips becomes a significant bottleneck in high-speed data communication. Thus, how to speed up the data transmission over several inches or even meters becomes more and more important.

Figure 1 shows a typical flat-panel-display (FPD) link application with LVDS interface. The FPD link chipset is a family of interface devices specifically configured to support data transmission from graphics controller to LCD panels. The employed technology, LVDS (low-voltage differential signaling), [1], is one of I/O interfaces usually used in high-speed data communication. LVDS interface can not only speed up the data rate but also reduce the power consumption. To decrease the number of data channels in FPD link, the transmitters have been specified to translate 28 bits wide TTL data into 4 bits wide and 7 bits deep LVDS data. As the result, each data channel would transmit 7 serial bits in each clock period. In this case, as shown in Fig. 1, four data channels are used to transmit LVDS data signals and one clock channel is used to transmit clock.

To recover these serial data streams, the receiver must generate seven different sampling clock phases to sample serial data stream and convert it into parallel data. However, because of the channel effect, incorrectly data recovering might be induced by the skew between data channels and clock channel. As data rate is increased, the skew effect becomes more serious. As the result, how the receiver generates suitable sampling clock phases against the skew effect becomes more and more important.

In this work, a LVDS receiver with new data recovery design for FPD link is presented. This LVDS receiver can automatically adjust the sampling clock phases at the stable region of each serial bit against the skew effect.

II. Circuit Operation

Three-times-oversampling is the popular way used to recover data [2]-[4]. In FPD link, because the input data rate is the seven times input clock frequency, it needs 21 different sampling phases to implement three-times-oversampling. Implemented with fully differential circuit structure, a PLL providing 28 different sampling clock phases can be implemented with 14 VCO cells, as shown in Fig.2. But a PLL providing 21 sampling clock phases must be implemented with 21 VCO cells. To reduce the VCO cells, a PLL providing 28 different sampling clock phases is used to design receiver in this work. By selecting 21 suitable sampling clock phases from these 28 sampling clock phases to oversample 7 bits serial data stream, the receiver can recover serial data stream correctly. However, the motion of selecting suitable sampling clock phases needs a lot of MUXs to implement it. To save these MUXs and to reduce the circuit complexity, a new delay-selecting technique is adopted to implement the receiver in this work.

In the new proposed delay-selecting technique, the receiver will delay input data stream for quarter data step, half data step, and three-quarters data step, respectively. One suitable delayed data stream of these three delayed data streams will be selected to cancel the skew between input data stream and input clock.

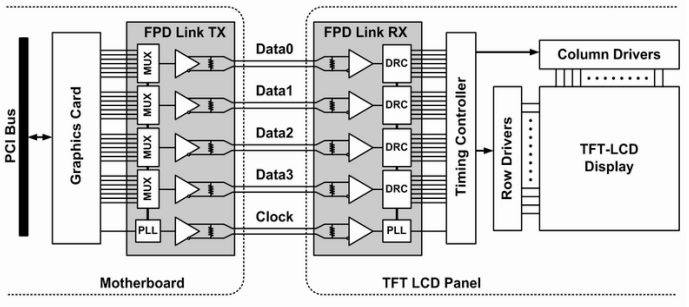


Figure 1. Typical flat-panel-display (FPD) link application with LVDS interface.

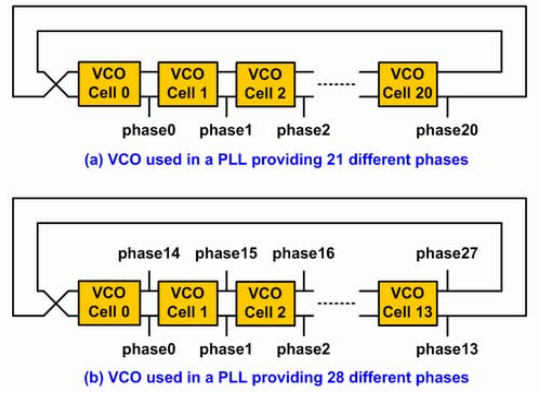


Figure 2. The VCOs in PLL for providing (a) 21 phases and (b) 28 phases.

Figure 3 shows the operation timing of the new proposed delay-selecting technique. The selected data stream will be delayed again for quarter, half, and three-quarters data step by the detection window. These delayed data streams will be sampled with seven different sampling clock phases provided by the PLL. By analyzing these sampled results, the LVDS receiver can detect whether data transition edges happen near the sampling points or not, and shift the delay time up or down in the next clock period by selecting different delayed data stream in delay selector. The LVDS receiver will keep adjusting the delay time until these sampling points locate in the data stable region. In FPD link, because the first recovered bit in each clock period must be the serial bit which is most close to the rising edge of the input clock [5], the delay time used to cancel the skew between data stream and clock is limited in +/– half data step.

Figure 3. Operation timing of the new proposed delay-selecting technique.

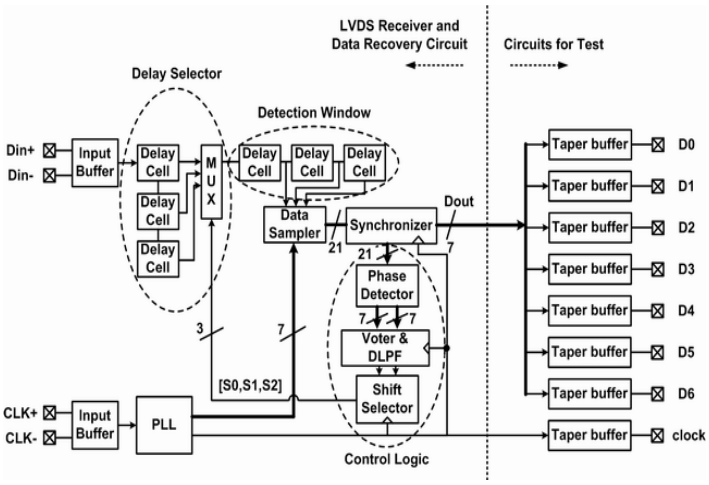


Figure 4. The architecture of the LVDS receiver designed with the new proposed delay-selectiong technique.

III. Circuit Implementation

Figure 4 shows the architecture of the LVDS receiver designed with the new proposed delay-selecting technique.

The input buffers are used to convert input signals, input data stream or input clock, from the 3.3V-domain LVDS signals to 1.2V full-swing signals. After the input buffer, all signals are processed in the 1.2-V power domain. The full-swing 1.2V clock will be sent into PLL. The PLL will lock the input clock and provide seven different sampling clock phases. The full-swing 1.2V input data stream will be sent into delay selector and detection window. The delay time of each delay cell is quarter data step time. Each delayed serial bit will be oversampled three times in the data sampler. The synchronizer is used to synchronize these oversampling results.

Phase detector is used to detect whether a data transition happens in each oversampling range and sends out seven adjusting requirements in each clock period. However, wrong adjusting requirements might be induced by the jitter effect. Against such wrong adjustment, a voter and a DLPF (digital low pass filter) are used [2]. The voter is used to make sure that the adjusting requirements "up" or "down" are two more than opposite adjusting requirements "down" or "up" in each clock period. The DLPF is used to make sure that the adjusting requirement keeps in the same direction "up" or "down" over three clock periods. After the voter and the DLPF, the adjusting requirement will be accepted and sent into the shift selector. According to the adjusting requirement, the shift selector will send new selecting signal into the delay selector to shift delay time up or down quarter data step time in the next clock period.

A. Input Buffer

Input buffers used in this work are modified from the circuit reported in [6]. Because the designed LVDS is fabricated in a 0.13-μm 1.2V/3.3V CMOS process, the input buffer is designed to covert 3.3V-domain LVDS signal into 1.2V-domain full-swing signal. Figure 5 shows the modified input buffer. Because the Vdd at the terminal of R1 and R2 is 1.2V, the differential input signal at the second stage buffer, n1 and n2, will be kept under 1.2V. As the result, the first stage buffer can convert 3.3V-domain LVDS input signal into a differential signal under 1.2V. Because the operation voltage of each node in the second stage buffer is under 1.2V, the second stage buffer can be implemented with 1.2V devices. The second stage buffer will convert the differential signals into 1.2V full-swing signals at its output nodes.

B. PLL

Although only seven sampling phases are needed in the designed LVDS receiver, the PLL is implemented with 14 VCO cells as shown in Fig. 2(b). Because the PLL is implemented with 14 VCO cells, the delay time of each VCO cell is quarter data step time when the PLL locks the input clock. By using the same VCO cells as the delay cells, the delay time of each delay

cells can be locked at quarter data step time. Figure 6 shows the circuit diagram of the VCO cell [7].

IV. Measurement Results

The designed LVDS receiver has been fabricated in a 0.13-μm 1.2V/3.3V CMOS process. Figure 7 shows the layout and die-on-board photo of the fabricated LVDS receiver. Figure 8 shows the measurement setup to verify this LVDS receiver. The pattern generator sends 7 bits serial LVDS data stream and clock into the test chip, and the test chip will recover these serial data into 7 bits parallel recovered data. These recovered parallel data and locked clock will be sent out by taper buffers, which are shown in the right-half side of Fig. 4.

Figure 9 shows the input data stream and the expected recovered data at the output nodes. The pattern generator sets the first serial bit as cyclic "0101", and both the second and the seventh serial bits are set as cyclic "0011". If the test chip can recover data correctly, the first recovered bit, D0, will be a cyclic "0101" data stream, and the second recovered bit, D1, and the seventh recovered bit, D6, will be a cyclic "0011" data stream. Figure 10 shows the measurement result when the data rate is 1.25 Gb/s. D0, D1, and D6 are all recovered correctly.

Figure 11 shows the measurement results, when setting the delay time (as skew) between data stream and clock as 100 ps and 150 ps at 1.25 Gb/s operation data rate (data step time is 800 ps). When the delay time is 100 ps, these recovered data can be still recovered correctly in Fig. 11(a). But, when the delay time is increased to 150 ps, the recovered D0 becomes cyclic "0011" and the recovered D1 becomes cyclic "0101" in Fig. 11(b).

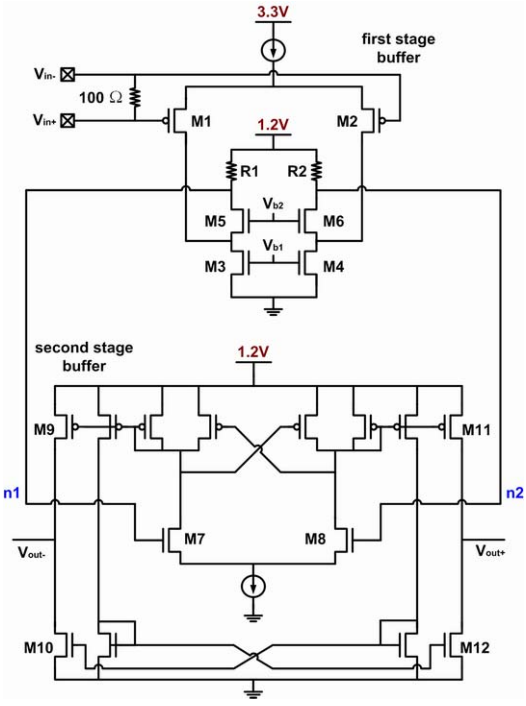


Figure 5. Schematic diagram of input buffer.

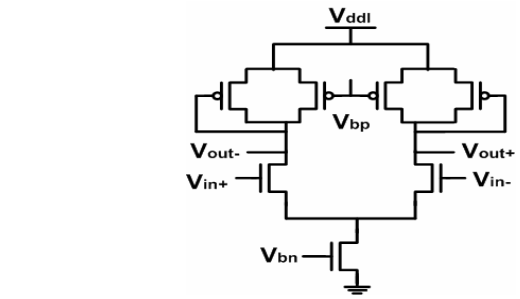


Figure 6. Circuit diagram of VCO cell.

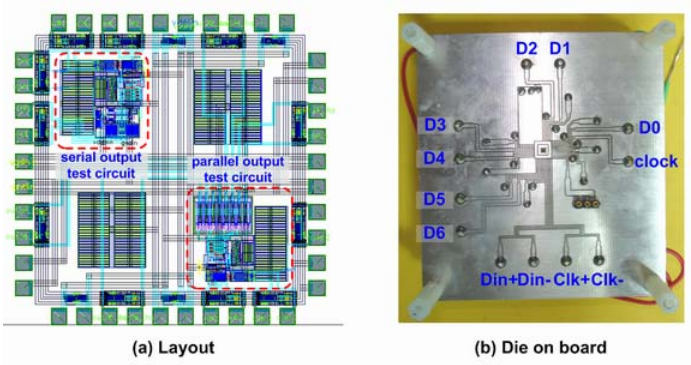


Figure 7. (a) Layout and (b) die-on-board photo of the fabricated LVDS receiver.

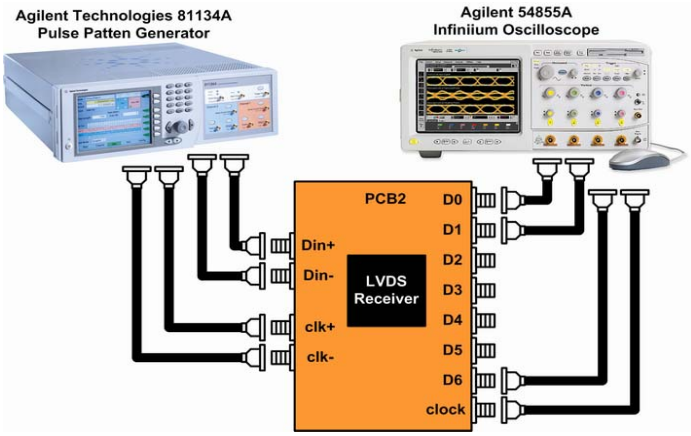


Figure 8. Measurement setup.

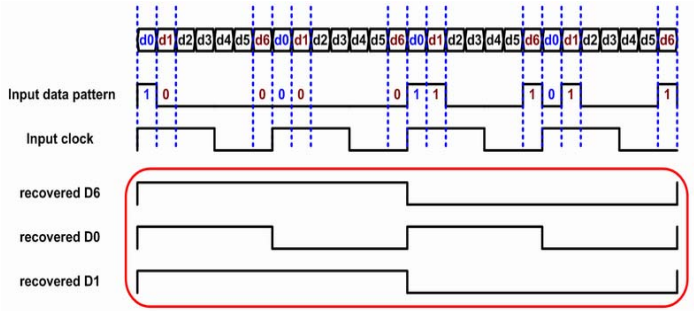
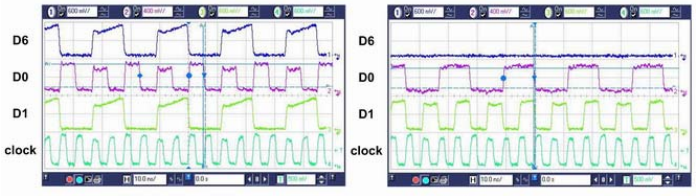


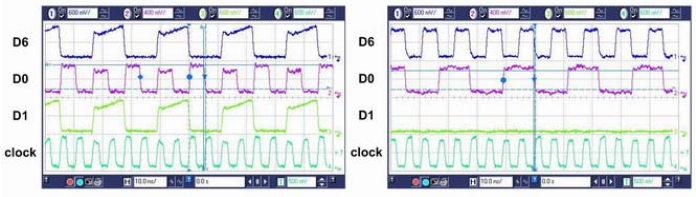
Figure 9. Test input pattern and the corresponding correct recovered data outputs.

Figure 10. Measured results when the data rate is 1.25Gb/s.



(a) (b)

Figure 11. Measured results when the delay time is (a) 100 ps and (b) 150 ps.



(a) (b)

Figure 12. Measured results when the delay time is (a) –600 ps and (b) –650 ps.

Figure 12 shows the measurement results, when setting the delay time between data stream and clock as –600 ps and –650 ps at 1.25 Gb/s operation data rate. When the delay time is –600 ps, these recovered data can be still recovered correctly in Fig. 12(a). But, when the delay time is –650 ps, the recovered D0 becomes cyclic "0011" and the recovered D6 becomes cyclic "0101" in Fig. 12(b). As the result, the skew tolerance of the fabricated LVDS receiver is from –600 ps to 100 ps. However, the skew region should be a symmetrical region. Thus, a 250 ps skew may exist in the measurement setup (including the test PCB and the metal trace from the pad to the internal circuits of the chip) when the delay time is set at 0 ps, as shown in Fig. 13. As the result, the skew tolerance of the fabricated LVDS receiver should be +/– 350 ps.

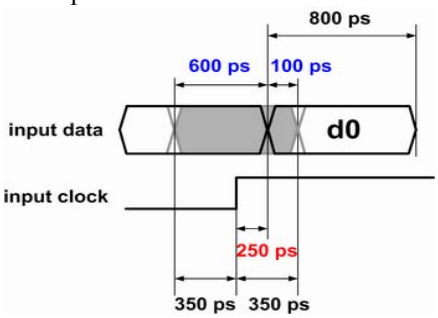


Figure 13. Skew tolerance of the fabricated LVDS receiver in the measurement.

TABLE I. MEASUREMENT SUMMARY

Symbol	Parameters	Conditions	Min	Max	Units
V_{cm}	Input common mode voltage	V_d = 400 mV	0	1270	mV
V_d	Input differential voltage	V_{cm} = 1 V	150	—	mV
f_{clk}	Input clock frequency	V_{cm} = 1 V and V_d = 400 mV	165	250	MHz
DR	Input data rate	V_{cm} = 1 V and V_d = 400 mV	1.11	1.8	Gb/s
t_{skew}	Skew tolerance between input signals	DR = 1.25 Gb/s	–350	350	ps
P	Power consumption	DR = 1.25 Gb/s	—	39.7	mW

Table I is the measurement summary of the fabricated LVDS receiver. The LVDS receiver can receive a LVDS signal with common-mode voltage of 0 ~ 1.27 V and minimum differential voltage of 150 mV. The operation data rate of the LVDS receiver is in the range of 1.11 Gb/s ~ 1.8 Gb/s.

V. CONCLUSION

A LVDS receiver with new data recovery design for FPD link has been presented. This proposed LVDS receiver design has been implemented in a 0.13-µm CMOS technology, and the function of LVDS receiver has been successfully verified. The fabricated LVDS receiver can correctly recover data signals at the data rate from 1.11 Gb/s to 1.8 Gb/s, which can fully support the operation of FDP link with UXGA resolution. Comparing with a conventional design, the new proposed LVDS receiver architecture can reduce the circuit complexity, layout area, and power consumption for flat-panel-display applications.

REFERENCES

[1] IEEE standard for low-voltage differential signaling (LVDS) for scalable coherent interface (SCI), 1596.3 SCI-LVDS standard, IEEE Std. 1596.3-1996, 1994.

[2] S. Kim *et al*., "An 800 Mbps multi-channel CMOS serial link with 3X oversampling," in *Proc. of IEEE Custom Intergrated Circuits Conference*, 1995, pp. 451-454.

[3] S.-H. Lee *et al*., "A 5-Gb/s 0.25-µm CMOS jitter-tolerant variable-interval oversampling clock/data recovery circuit," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1822-1830, 2002.

[4] Y. Miki *et al*., "A 50-mW/ch 2.5-Gb/s/ch data recovery circuit for the SFI-5 interface with digital eye-tracking," *IEEE J. Solid-State Circuits*, vol. 39, pp. 613-621, 2004.

[5] LVDS 24-Bit Color Flat Panel Display Link, DS90CF581/ DS90CF582 National Semiconductor Corp., 1997.

[6] A. Boni, A. Pierazzi, and D. Vecchi, "LVDS I/O interface for Gb/s-per-pin operation in 0.35-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, pp. 706-711, 2004.

[7] J. G. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1723-1732, 1996.