ESD Protection Design for Giga-Hz RF CMOS LNA with Novel Impedance-Isolation Technique

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Abstract — A novel ESD protection design with impedance-isolation technique is proposed and successfully verified in a 0.25-μm CMOS process with top thick metal. Its purpose is to reduce the detrimental effect of the on-chip ESD protection circuit on the power gain and noise figure of an RF LNA circuit. With the resonance of LC-tank, the impedance generated from the ESD protection devices can be isolated from the input node of RF LNA at the operation frequency, so the power gain loss and noise figure of RF LNA can be successfully co-designed with the desired ESD robustness. The proposed ESD protection circuit with novel impedance-isolation technique will be one of the most effective ESD protection solutions for RF circuits in higher frequency band (>10GHz).

I. INTRODUCTION

The parasitic effects of on-chip ESD clamp devices on the I/O pad often degrade the power gain and increase the noise figure in RF circuit, especially in the LNA input stage. There are some requests on ESD clamp devices in giga-Hz RF circuits: low parasitic capacitance, constant input capacitance, insensitive to substrate coupling noise, and good ESD performance [1], [2]. The traditional input ESD clamp device is the gate-grounded NMOS (GGNMOS), which was often drawn with a large device dimension and wider drain-contact-to-poly-gate layout spacing to sustain an acceptable ESD level [3], [4]. To further improve ESD level of NMOS, the gate-coupled circuit technique [5], [6] or the substrate-triggering circuit technique [7]-[9] had been designed to uniformly trigger on the multiple fingers of ESD protection NMOS. But, the GGNMOS with a larger device dimension and a wider drain diffusion junction contributes a larger parasitic drain capacitance to the input pad. The overlapped gate-to-drain capacitance also contributes to the input pad. Such GGNMOS is not suitable for RF ESD application, especially in the higher frequency band.

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The SCR device [10] with the anode of P+ diffusion in an N-well, which has a lower parasitic capacitance to ground, as compared to GGNMOS with N+ diffusion on the P-substrate, could be a good choice for RF ESD protection. But, the higher trigger-on voltage and the slower turn-on speed must be enhanced [11] to effectively protect the much thinner gate oxide of input devices in RF CMOS process.

A typical request on the maximum loading capacitance for RF ESD protection device was specified as ~200fF [12]. In order to fulfill such a tight specification, diodes are commonly used for ESD protection in RF LNA [13]-[15]. Moreover, by adding a turn-on efficient ESD clamp circuit across the power rails of ESD protection circuit formed by double diodes, the overall ESD level of RF input pin had been significantly improved [16]. Recently, a cancellation technique has been reported to reduce the parasitic effect from the ESD protection device for GHz RF input [17].

In this paper, a novel on-chip ESD protection design with LC-tank to tune out the parasitic effects from ESD clamp devices for giga-Hz RF applications is proposed. The LC-tank is designed to resonate at the operation center frequency of the RF circuits. So, the RF input port will see very large impedance from the ESD clamp devices with the LC-tank, which resonate at the RF operation frequency. The proposed LC-tank ESD protection circuits with different

combinations of L and C values have been designed and verified in a 0.25-μm CMOS process. The RF circuit performance metrics, including the noise figure and power gain, on the fabricated LC-tank ESD protection circuits has been investigated by two-port GSG measurement. ESD robustness of the fabricated LC-tank ESD protection circuits has been verified by ESD simulator in both human-body-model (HBM) and machine-model (MM) ESD stresses.

II. Impact of ESD Devices on RF Performance

For an input pin, there are four ESD-stress modes [6], in which the positive or negative ESD pulse is applied to an input pin with the VDD or VSS pins relatively grounded. To provide comprehensive protection against such four-modes ESD stress, the typical ESD protection design for RF circuits is shown in Fig. 1, which had been successfully verified in a 900-MHz RF receiver with HBM ESD level of greater than 8kV [16]. The power-rail ESD clamp circuit was designed to help the ESD protection diodes for discharging ESD current in forward-biased condition during the four-modes ESD stresses.

Diodes operating in the forward-biased condition can sustain much high ESD level, so the ESD protection diodes can be drawn with a small device dimension to minimize the parasitic effect to RF circuits. However, when the operating frequency of RF circuits is further increased, such parasitic effect from the small-dimension ESD protection diodes can still degrade RF performance.

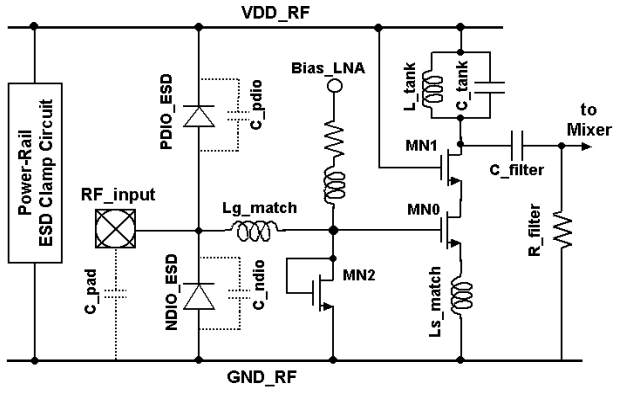


Fig. 1. The typical ESD protection design with double diodes and active power-rail ESD clamp circuits for LNA RF input pin [16].

To further reduce the parasitic capacitance effect from the ESD protection diodes on the RF input pin, the diodes can be realized in the polysilicon layer in CMOS process and stacked in series [1], [2]. The typical design with stacked polysilicon diodes to protect RF input pin is shown in Fig. 2, which had been successfully verified in a 2.4-GHz RF LNA with ESD robustness of 2kV [2].

To find the impact of such ESD protection diodes on the circuit performance of giga-Hz RF LNA, the power gain of a RF LNA with on-chip ESD protection device has been generally calculated from its small-signal equivalent circuit, as that shown in Fig. 3.

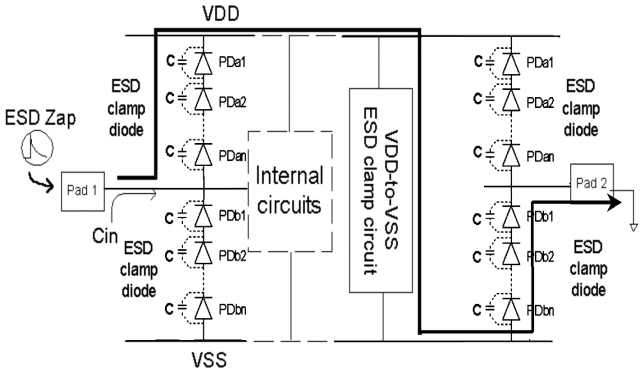


Fig. 2. Typical ESD protection design with stacked poly-silicon diodes to reduce parasitic capacitance effect from ESD protection devi ces for LNA RF input pin [2].

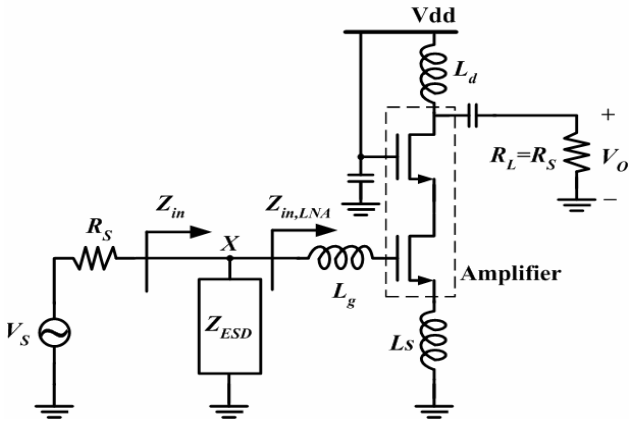


Fig. 3. The equivalent small-signal circuit of a RF LNA with on-chip ESD protection device for calculating the overall power gain.

A simple expression for the input impedance at resonance of the inductively degenerated LNA is [18]

$$Z_{in,LNA} = s(L_s + L_g) + \frac{1}{sC_{gs}} + (\frac{gm}{C_{gs}})L_s \approx w_T L_s = R_s \,. \quad (1)$$

The overall input impedance of the RF LNA with ESD protection device (Z_{ESD}) is

$$Z_{in} = Z_{ESD} \parallel Z_{in,LNA} \approx Z_{ESD} \parallel R_s . \quad (2)$$

So, the overall transconductance (G_m) of this LNA stage is

$$G_m = \frac{Z_{ESD}}{Z_{ESD}+R_s}\frac{w_T}{s(R_s+Z_{in})} = \frac{w_T}{sR_s}\frac{Z_{ESD}}{R_s+2Z_{ESD}} = \frac{w_T}{sR_s}\frac{1}{2+\frac{R_s}{Z_{ESD}}}. \quad (3)$$

To analyze the overall power gain of the LNA, we neglect the feedback capacitor C_{gd} of the MOS device first and assume that the input and output are conjugately matched to get a simpler expression of the power gain. The transducer power gain G_T (corresponding to S21) is

$$G_T = \frac{P_L}{P_{avs}} = \frac{\frac{1}{8}|V_s G_m|^2 (R_o \parallel R_s)}{\frac{1}{8}|V_s|^2 / R_s} = |G_m|^2 R_s (R_o \parallel R_s) = \left(\frac{w_T}{w_0}\right)^2 \frac{(R_o \parallel R_s)}{R_s}\left|\frac{1}{2+\frac{R_s}{Z_{ESD}}}\right|^2 . \quad (4)$$

In (4), P_L is the power delivered to the load, P_{avs} is the power available from the source, and R_o is the output impedance of the amplifier. w_T and w_0 are the unity gain frequency of MOS device and the operating frequency of input RF signal, respectively.

Ideally, if the impedance of the ESD protection device (Z_{ESD}) can be approaching to infinite, the power gain (G_T) and noise figure (NF) of the RF LNA with ESD protection device can be converged to those of a pure RF LNA without the ESD protection device. However, even though the ESD protection diodes are operated in the forward-biased condition to discharge ESD current with the help of active power-rail ESD clamp circuit, such ESD protection diodes still have to be drawn with some finite device size for sustaining the desired ESD level. The parasitic capacitance and resistance from the ESD protection diodes, even with limited device size, still generate the Z_{ESD} into above equations.

To practically investigate the negative impact from the ESD protection diode to RF performance, a shallow-trench-isolation (STI) diode with different device dimensions had been fabricated in a 0.25-μm salicided CMOS process [19]. The schematic cross-sectional view of STI diode is shown in Fig. 4(a), where it is an n+/p-well diode. The N+ diffusion (cathode) and P+ diffusion (anode) are separated by shallow trench isolation (STI). The practical layout of a unit cell of the STI diode and its symbol are drawn in Fig. 4(b). The device cross-sectional view along the line A--B of Fig. 4(b) is corresponding to that drawn in Fig. 4(a). In Fig. 4(b), X is the length of the N+ diffusion. S is the minimum spacing of STI. W is the width of the N+ diffusion. The parameter of width (W) was changed in the testchip to investigate its impact on the power gain (S21) and noise figure of RF performance. In ESD condition, the ESD current path along the diode is shown by the dashed line in Fig. 4(a). The ESD current would flow from P+ diffusion to N+ diffusion under the STI layer with the help of active power-rail ESD clamp circuit.

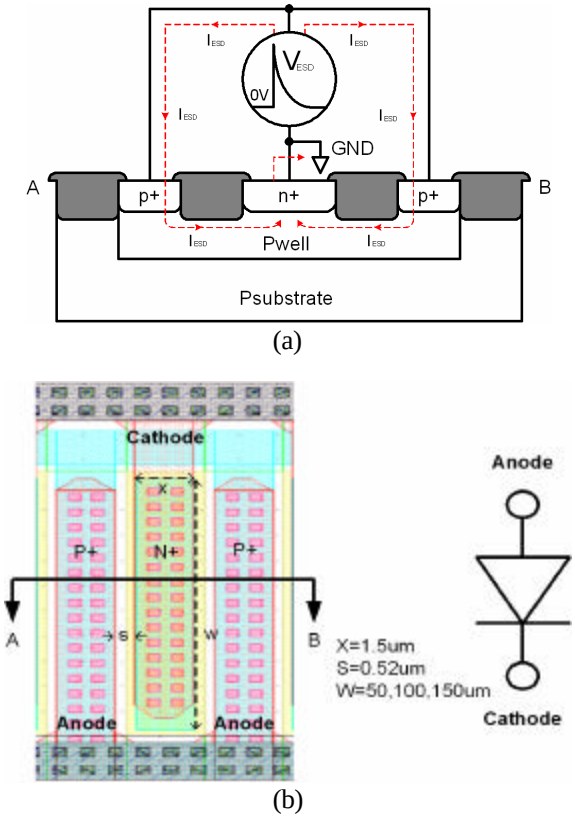
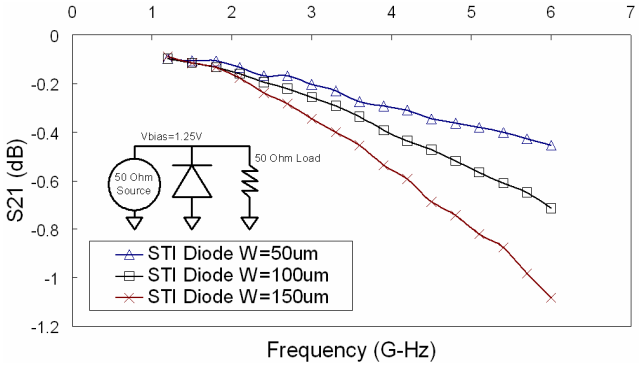


Fig. 4. (a) The schematic cross-sectional view of the STI diode. (b) The practical layout of a unit cell of the STI diode and its symbol.

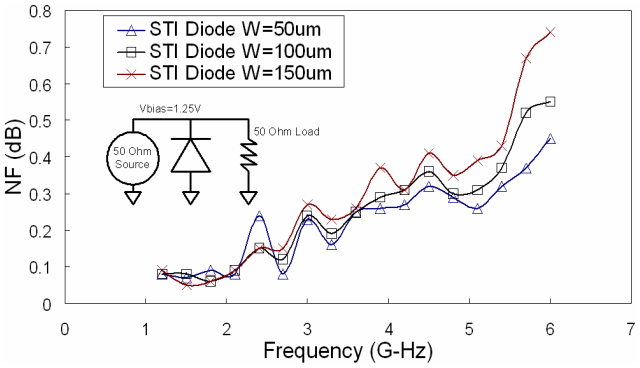
An S-parameter measurement system is used to measure the power gain (S21) and noise figure of the fabricated STI diodes under different device dimensions. Every ESD diode has its own two-port

GSG pads. The power gain S21 and noise figure is measured from 1.2GHz to 6GHz with a step of 300MHz. The ESD diode is connected between signal line and ground. The dc bias voltage on the signal line is 1.25V. The input port is with 50-ohm source and the output port is with 50-ohm load.

The dependences of S21 and noise figure on the operating frequency of STI diodes under different device dimensions are compared in Figs. 5(a) and 5(b), respectively. The power gain S21 is decreased by STI diode under the same device dimension when the operating frequency increases. The power gain S21 decreases drastically by STI diode with a larger device dimension at a higher operating frequency. The difference of power gain S21 loss of the STI diodes between different device dimensions becomes larger at the higher frequency. The larger parasitic capacitance of STI diode wastes more RF signal to ground and causes the power gain loss.



(a)



(b)

Fig. 5. The measured (a) S21, and (b) noise figure, of STI diodes on the operating frequency under different device dimensions.

Obviously, the noise figure increases by STI diode under the same device dimension when the operating frequency increases, as shown in Fig. 5(b). The power gain loss is proportional to the increase of the noise figure. The noise figure increases drastically by STI diode with a larger device dimension under the higher operating frequency. This has confirmed the negative impact from the ESD protection diodes to RF circuit performance.

If the RF circuit is operating at a very high frequency (>10GHz), the equivalent impedance of ESD protection devices seen from the RF input port to ground will be reduced. As Z_{ESD} decreases, gain decreases and this will increase noise figure. So, the impedance Z_{ESD} will not approach infinity in the actual RF LNA with any ESD protection circuit. This implies that the on-chip ESD protection circuit will seriously degrade circuit performance of RF LNA, especially in much higher frequency. Therefore, how to design effective on-chip ESD protection circuit for RF circuits operating in higher frequency is a challenge, which must be solved for safe mass production of the RF chips.

III. ESD Protection Design with Impedance-Isolation Technique

The RF power gain loss and noise figure contributed by ESD devices are strongly dependent on the parasitic capacitance and parasitic resistance of ESD devices in the input port. If the parasitic effect of input ESD devices can be blocked from the RF circuit operation, the RF power gain would not be degraded anymore. To provide nearly infinite impedance from the on-chip ESD protection devices, a novel impedance-isolation ESD protection design with LC-tank to tune out the parasitic effects from the ESD devices for giga-Hz RF applications is shown in Fig. 6, where the LC tank is inserted between the RF input pad and the ESD protection diodes (called as the **LCD** structure).

To avoid ESD diodes operating in breakdown condition during PS-mode (positive-to-VSS) and ND-mode (negative-to-VDD) ESD stresses to cause a much lower ESD level, a turn-on efficient RC-based ESD clamp circuit between the power-rails is constructed into the ESD protection circuit. Because the ESD current is discharged through forward-biased Dp1 (Dn1), thick metal inductor, and the large-dimension MNESD between power rails under the PS-mode (ND-mode) ESD stress, ESD level can be still maintained high enough to protect the internal RF circuits.

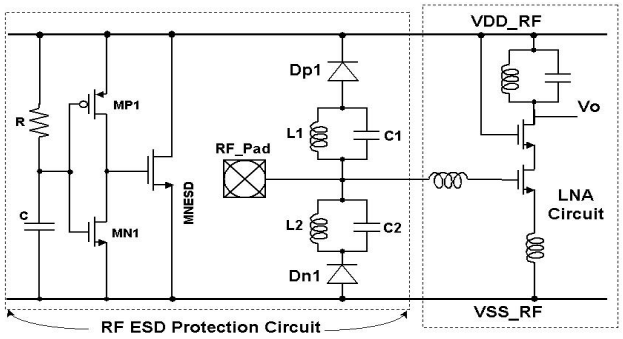


Fig. 6. The proposed impedance-isolation ESD protection design with LC-tank for RF LNA circuit (called as the **LCD** structure).

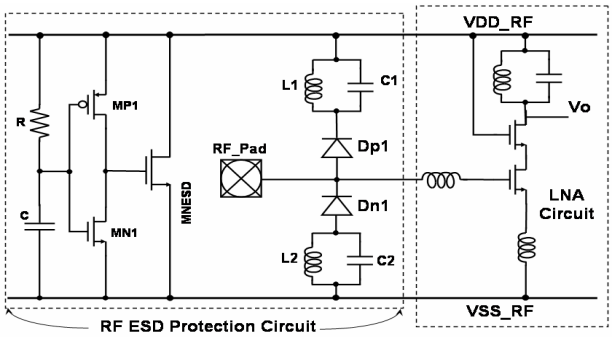


Fig. 7. Alternative impedance-isolation ESD protection design with LC-tank for RF LNA circuit (called as the **DLC** structure).

The LC-tank is designed to resonate at the operation center frequency of the RF circuit. So, the RF input port will ideally see infinite impedance from ESD clamp devices with the LC-tank, which resonate at RF operation frequency. The inductance and capacitance in the LC-tank can be decided from the resonating frequency of

$$\omega_0 = \frac{1}{\sqrt{LC}}. \qquad (5)$$

With consideration on the parasitic effect of inductor and capacitor realized in the real silicon chip, the values of inductance and capacitance of LC-tank under the same resonating frequency (demonstrated at 2.7 GHz in this work) are modified in a pair to investigate the overall circuit performance. The LC-tanks with the same resonating frequency at 2.7GHz, but realized by different inductance and capacitance are listed in Table I, which have been designed and fabricated in a 0.25-μm CMOS process with thick top-layer metal to realize inductors.

With consideration on the Q (quality) factor of on-chip inductor in RF CMSO process, the LC tank may have some impedance mismatching on the operating frequency. To verify the efficiency of impedance isolation in the ESD protection circuit, an alternative design is shown in Fig. 7, where the LC tank is inserted between the ESD protection diodes and the VDD/VSS power rails (called as the **DLC** structure). In order to stack the LC-tank and the N+ diode, a deep N-well is used to isolate the P-well of the N+ diode from the common P-type substrate.

A lot of test chips with the proposed impedance-isolation technique have been designed and fabricated with different diode dimensions (for Dn1 and Dp1), or with different LC values (but with the same resonant frequency of 2.7 GHz).

TABLE I
DIMENSIONS OF INDUCTOR AND CAPACITOR IN LC TANK.

fo=2.7GHz	1	2	3	4	5
Inductance (top thick metal)	12.12nH (6.5 Circles)	8.64nH (5.5 Circles)	5.88nH (4.5 Circles)	3.74nH (3.5 Circles)	2.17nH (2.5 Circles)
Capacitance (MIM)	219fF (14.8umx14.9um)	361fF (19umx19um)	596fF (24.4umx24.4um)	999fF (31.6umx31.6um)	1731fF (41.6umx41.6um)

TABLE II
LAYOUT DIMENSIONS OF ESD PROTECTION DIODES.

Total Capacitance	*200f*			*600f*			*1200f*		
Dimension	W(μm)	X(μm)	Finger Number	W(μm)	X(μm)	Finger Number	W(μm)	X(μm)	Finger Number
Dn1	21.38	3.2	1	21.38	3.2	3	21.38	3.2	6
Dp1	22	3.2	1	22	3.2	3	22	3.2	6

IV. EXPERIMENTAL RESULTS

The proposed impedance-isolation ESD protection circuits with different combinations of LC-tanks have been designed and verified in a 0.25-μm CMOS process for both LCD and DLC structures. The partial layout diagram for impedance-isolation RF ESD protection circuits in a testchip for two-port GSG measurement is shown in Fig. 8. The ESD protection diodes (Dn1 and Dp1) are drawn in different device dimensions with the capacitance of 100fF, 300fF, and 600fF for each diode. The layout dimensions for the Dp1 and Dn1 diodes under different capacitances, which are directly calculated from SPICE parameters, are shown in Table II.

The RF circuit performance of noise figure and power gain on the fabricated LC-tank ESD protection circuits have been investigated by two-port GSG measurement with the S-parameter measurement system HP 85122A. The experimental setup to measure power gain and noise figure is shown in

Fig. 9. ESD robustness of the fabricated impedance-isolation ESD protection circuits has been verified by ESD Zapmaster in both human-body-model (HBM) and machine-model (MM) ESD stresses.

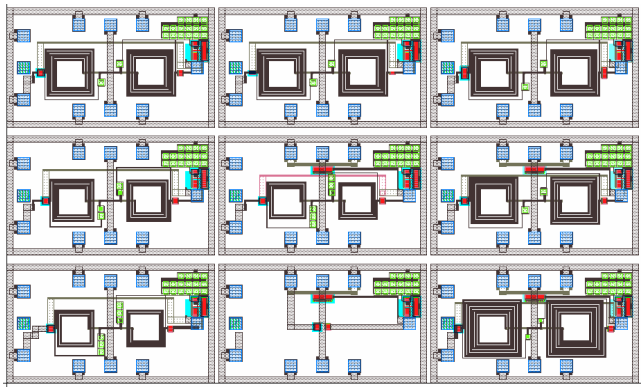


Fig. 8. Part of the layout diagram for impedance-isolation RF ESD protection circuits in a testchip for two-port GSG measurement.

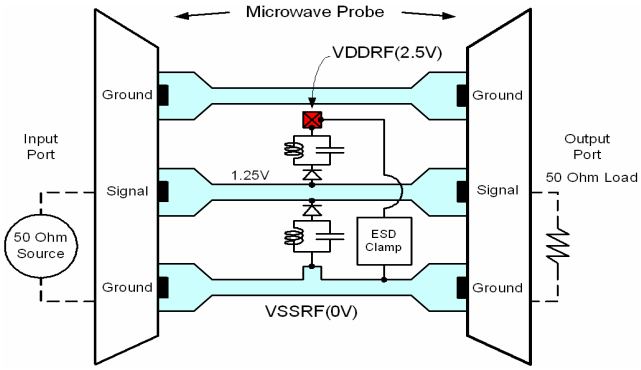
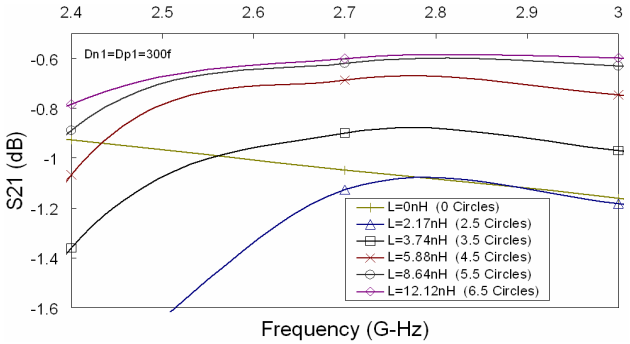


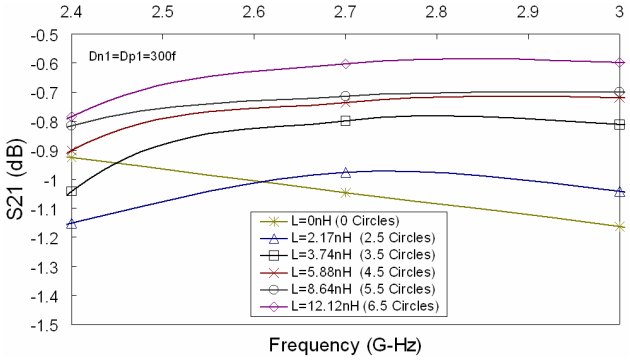
Fig. 9. The experimental setup to measure the power gain and noise figure of the fabricated RF ESD protection circuit with LC-tank.

A. Power Gain

The power gain S21 vs. frequency of the impedance-isolation RF ESD protection circuit with LCD or DLC structure under different inductance is shown in Figs. 10(a) and 10(b) during the frequency range of 2.4 ~3 GHz. The line shown with L=0 nH (0 circle) means that the ESD protection diodes were not blocked with the LC-tank, which is the traditional ESD protection design of Fig. 1 for comparison reference. The diodes (Dn1 and Dp1) in Fig. 10 have a parasitic capacitance of 300 fF for each diode. In Fig. 10(a), the measured results show that the power gain loss become smaller when the inductance is larger. At 2.7 GHz, the RF power gain S21 is increased from –1.05 dB (without LC tank) to –0.6 dB (with LC tank, L=12.12 nH).



(a)



(b)

Fig. 10. The measured power gain loss of the impedance-isolation RF ESD protection circuit from 2.4 to 3 GHz with different inductances under the (a) LCD structure, and (b) DLC structure.

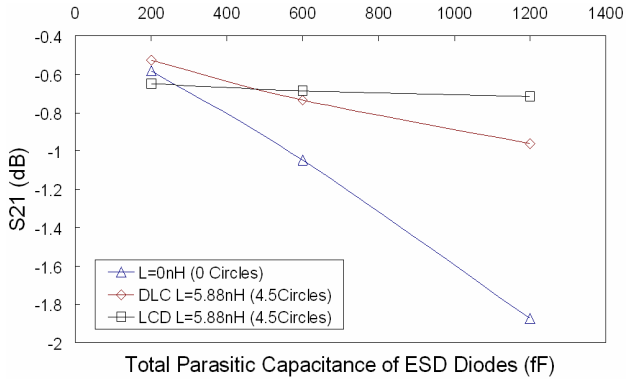


Fig. 11. Comparisons on the power gain loss between the impedance-isolation RF ESD protection circuit with LCD and DLC structures and the prior-art design without LC tank at 2.7 GHz.

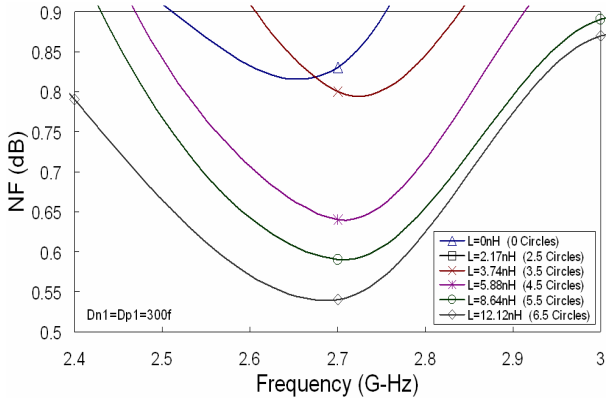
When ESD diodes are drawn with larger device sizes, comparisons on the power gain loss (at 2.7 GHz) between the proposed RF ESD protection design (LCD structure) and the prior-art ESD protection

design marked with L=0nH (in Fig. 1 without LC tank) are shown in Fig. 11. The S21 is seriously degraded in Fig. 11, when the total parasitic capacitance of the ESD protection diodes is increased (the ESD protection diode dimension is increased). However, the degradation on S21 in Fig. 11 can be rescued when the LC tanks are added into the ESD protection circuits. Especially, the LCD structure shows a better S21 when the ESD protection diode dimension is increased. This has proven that the LC-tank technique can successfully block the most parasitic effect from ESD diodes to RF circuits, especially when the ESD diodes are drawn with larger device dimensions.

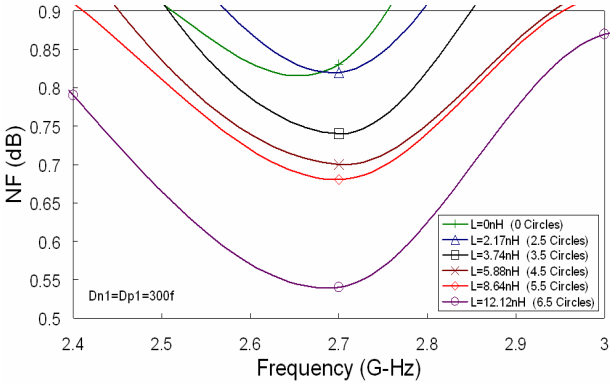
B. Noise Figure

The noise figures in the frequency range, between 2.4 GHz to 3 GHz, among the fabricated RF ESD protection circuits with different inductances in the LC-tank are compared in Fig. 12(a) and 12(b) with the LCD and DLC structures, respectively. The line shown with L=0 nH (0 circle) is the prior-art ESD protection design of Fig. 1 as a reference. The noise figure (NF) of the proposed RF ESD circuit with LC-tank is smaller than that of the traditional ESD protection circuits without LC-tank. All the ESD diodes (Dn1 and Dp1) are drawn with the same device dimensions in ESD protection circuits, which are all with a parasitic capacitance of 300 fF. At 2.7 GHz, the overall noise figure of RF ESD protection circuit is decreased from 0.83 dB (without LC-tank) to 0.54 dB (with LCD structure, L=12.12 nH).

The comparisons on the increase of noise figure (at 2.7 GHz) between the proposed RF ESD protection design with LC tank and the prior-art ESD design without LC tank are shown in Fig. 13, under different device dimensions of the ESD diodes. The noise figure in dB scale is obviously increased in Fig. 13, when the total parasitic capacitance of the ESD protection diodes is increased. With a larger ESD protection diode dimension (also larger parasitic capacitance), the ESD robustness of RF input pin can be increased. But, it also causes a serious increase on the noise figure of the RF performance. However, the increase on noise figure in Fig. 13 can be rescued when the LC tanks are added into the ESD protection circuits. Especially, the LCD structure shows a smaller noise figure when the ESD protection diode dimension is increased. The LCD structure performs a lower noise figure in higher frequency that that of DLC structure, because the DLC structure has the diodes connected to the RF input. The extra parasitic capacitance from the deep N-well in the N+ diode structure, or from the normal N-well in the P+ diode structure, slightly increases the noise figure of DLC structure.



(a)



(b)

Fig. 12. The measured noise figure of the impedance-isolation RF ESD protection circuit from 2.4 to 3 GHz with different inductances under the (a) LCD structure, and (b) DLC structure.

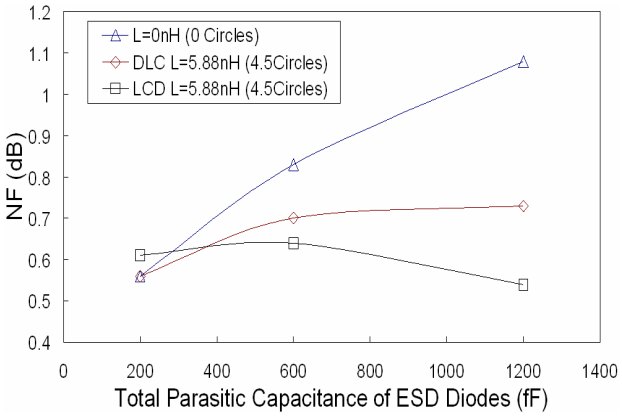


Fig. 13. Comparisons on the increase of noise figure between the impedance-isolation RF ESD protection circuit with LCD and DLC structures and the prior-art design without LC tank at 2.7 GHz.

C. ESD Robustness

The positive-to-VDD (PD-mode), negative-to-VDD (ND-mode), positive-to-VSS (PS-mode), and negative-to-VSS (NS-mode) HBM and MM ESD test results on the fabricated impedance-isolation RF ESD protection circuits with LCD structure under different inductor circles are summarized in Table III. All the LC-tanks have the same resonating frequency at 2.7 GHz. The total parasitic capacitance (Cdiodes) generated from the ESD diodes (Dn1 and Dp1) is also varied as 200, 600, and 1200 fF, to verify the corresponding ESD robustness. The actual layout dimensions for such diodes in a 0.25-μm CMOS process have been shown in Table II. The I-V curves of RF input pin with LCD RF ESD protection circuit before and after positive-to-VSS ESD stress are compared in Fig. 14, where the leakage currents are measured with VDD and VSS pins grounded together.

From the measured results in Table III, the more inductor circles in the LCD RF ESD protection circuits lead to the lower HBM and MM ESD levels, under the same device size (600 fF) of ESD diodes. When the inductor in LC-tank is kept as 4.5 circles in layout, the HBM and MM ESD levels of the proposed RF ESD protection circuit can be increased by the increase of the device size of ESD diodes, which are indicated as the Cdiodes in Table III.

As comparing the ESD levels of ESD protection diodes with different device dimensions, the diode of 1200fF did not sustain 2-times higher ESD level than that of the diode of 600 fF under the same LC tank design. To find the failure location, the PS-mode ESD-zapped RF input pin is observed under the bias of VDD at 2.5V and the input pin at 0V. The photon emission microscope (EMMI) is used to find the location of hot spots. The observed EMMI picture on the LCD RF ESD protection circuit after PS-mode ESD stress is shown in Fig. 15, where the hot spot is located on the Dp1 diode, not on the Dn1 diode. The failure is due to the contact spiking from the P+ diffusion of the Dp1 diode to the N-well. This implies that the ESD current is conducted from the RF input pin to the VDD power line through the LC tank and Dp1 diode, and then discharged from the VDD power line to the grounded VSS pin through the active power-rail ESD clamp circuit, under the positive-to-VSS ESD zapping condition. To reduce the parasitic capacitance generated from the diodes (Dp1 and Dn1), the layout clearance from the contact of P+ diffusion in N-well for Dp1 (N+ diffusion in P-well for Dn1) to the edge of P/N junction is drawn with a small spacing. This small clearance in Dp1 under the ESD zapping condition causes the contact spiking, as that shown in Fig. 15.

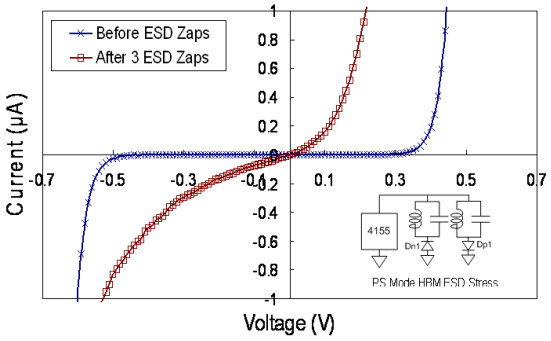


Fig. 14. The I-V curves of the RF input pin with LCD RF ESD protection circuit before and after positive-to-VSS (PS-mode) ESD stress.

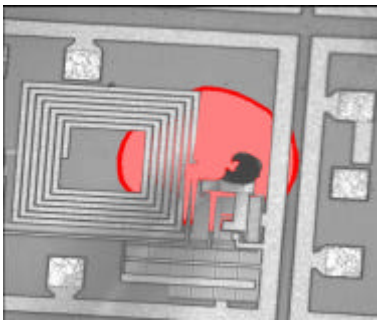


Fig. 15. The EMMI picture on the LCD RF ESD protection circuit after PS-mode ESD stress. The hot spot is located on the Dp1 diode.

V. CONCLUSION

A novel on-chip ESD protection design with impedance-isolation to tune out the parasitic effects from the ESD devices for giga-Hz RF applications has been successfully verified in a 0.25-μm CMOS process. The impedance-isolation concept realized by the LC-tank is designed to resonate at the operation center frequency of RF circuits, and to generate infinite impedance from ESD clamp devices with the LC-tank. To meet the requests of 2-kV HBM and 200-V MM ESD protection, ESD diodes (drawn with capacitance of Dn1=Dp1=300 fF) and LC-tank (L=5.88 nH drawn in 4.5 circles) in the proposed impedance-isolation RF ESD protection circuit can be optimized to have the best RF performance of power gain loss of only –0.69 dB and noise figure increase of only 0.63 dB, under 2.7 GHz operating frequency.

TABLE III
ESD LEVELS OF THE FABRICATED ESD PROTECTION CIRCUITS WITH LCD STRUCTURE.

LCD RF ESD Protection circuit			PD-mode		NS-mode		PS-mode		ND-mode	
Cdiodes	L	C	HBM(V)	MM(V)	HBM(V)	MM(V)	HBM(V)	MM(V)	HBM(V)	MM(V)
600fF	2.5 Circles	1731fF	5700	425	7100	775	3200	275	7200	400
600fF	3.5 Circles	999fF	4000	400	6800	700	2500	225	6000	350
600fF	4.5 Circles	596fF	3400	375	6600	650	2000	200	5200	275
600fF	5.5 Circles	361fF	3200	300	6400	650	1600	175	4600	225
600fF	6.5 Circles	219fF	2800	300	6000	625	1400	150	3900	200
200fF	4.5 Circles	596fF	3000	300	4300	500	1600	125	3000	200
1200fF	4.5 Circles	596fF	3800	325	8000	775	2700	200	6300	325

REFERENCES

[1] M.-D. Ker, T.-Y. Chen, and C.-Y. Chang, "ESD protection design for CMOS RF integrated circuits," in *Proc. of EOS/ESD Symp.*, 2001, pp. 346-354.

[2] M.-D. Ker and C.-Y. Chang, "ESD protection design for CMOS RF integrated circuits using polysilicon diodes," *Microelectronics Reliability*, vol. 42, pp. 863-872, 2002.

[3] S. Daniel and G. Krieger, "Process and design optimization for advanced CMOS I/O ESD protection devices," in *Proc. of EOS/ESD Symp.*, 1990, pp. 206-213.

[4] S. G. Deebe, "Methodology for layout design and optimization of ESD protection transistors," in *Proc. of EOS/ESD Symp.*, 1996, pp. 265-275.

[5] C. Duvvury and C. Diaz, "Dynamic gate coupling of nMOS for efficient output ESD protection," in *Proc. IRPS*, 1992, pp. 141-150.

[6] M.-D. Ker, C.-Y. Wu, T. Cheng, and H.-H. Chang, "Capacitor-couple ESD protection circuit for deep-submicron low-voltage CMOS ASIC," *IEEE Trans. VLSI Systems.*, vol. 4, pp. 307-321, Sept. 1996.

[7] M.-D. Ker, T.-Y. Chen, C.-Y. Wu, H. Tang, K.-C. Su, and S.-W. Sun, "Novel input ESD protection circuit with substrate-triggering technique in a 0.25-um shallow-trench- isolation CMOS technology," in *Proc. IEEE Int. Symp. Circuits and Systems*, 1998, pp. 212-215.

[8] C. Duvvury, S. Ramaswamy, A. Amerasekera, R. A. Cline, B. H. Andresen, and V. Gupta, "Substrate pump NMOS for ESD protection applications," in *Proc. of EOS/ESD Symp.*, 2000, pp. 7-17.

[9] M.-D. Ker and T.-Y. Chen, "Substrate-triggered technique for on-chip ESD protection design in a 0.18-μm salicided CMOS process," *IEEE Trans. on Electron Devices, in press*, 2003.

[10] M.-D. Ker, "Electrostatic discharge protection circuits in CMOS IC's using the lateral SCR devices: an overview," in *Proc. of IEEE Int. Conf. on Electronics, Circuits and Systems*, 1998, pp. 325-328.

[11] M.-D. Ker and K.-C. Hsu, "Substrate-triggered SCR device for on-chip ESD protection in fully silicided sub-quarter-micron CMOS process," *IEEE Trans. on Electron Devices*, vol. 50, no.2, pp. 397-405, Feb. 2003.

[12] C. Richier, P. Salome, G. Mabboux, I. Zaza, A. Juge, and P. Mortini, "Investigation on different ESD protection strategies devoted to 3.3V RF applications (2 Ghz) in a 0.18μm CMOS process," in *Proc. of EOS/ESD Symp.*, 2000, pp. 251-259.

[13] R. Velghe, P. Vreede, and P. Woerlee, "Diode network used as ESD protection in RF applications," in *Proc. of EOS/ESD Symp.*, 2001, pp. 337-345.

[14] G. Gramegna, M. Paparo, P.G. Erratico, and P. De Vita, "A sub-1-dB NF 2.3-kV ESD-protected 900-MHz CMOS LNA," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1010-1017, July 2001.

[15] P. Leroux, J. Janssens, and M. Steyaert, "A 0.8 dB NF ESD-protected 9mW CMOS LNA," *Tech. Dig. of ISSCC*, 2001, pp. 410-411.

[16] M.-D. Ker, W.-Y. Lo, C.-M. Lee, C.-P. Chen, and H.-S. Kao, "ESD protection design for 900-

MHz RF receiver with 8-kV HBM ESD robustness," in *Dig. of IEEE RFIC Symp.*, 2002, pp. 427-430.

[17] S. Hyvonen, S. Joshi, and E. Rosenbaum, "Cancellation technique to provide ESD protection for multi-GHz RF inputs," *Electronics Letters*, vol. 39, pp. 284-286, Feb. 2003.

[18] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE Journal of Solid-State Circuits*, vol.32, no.1, pp.745-759, 1997.]

[19] C.-M. Lee and M.-D. Ker, "Investigation on RF performance of diodes for ESD protection in giga-Hz RF circuits," in *Proc. of Taiwan ESD Conf.*, 2002, pp. 45-50.