

# Evaluation on Board-Level Noise Filter Networks to Suppress Transient-Induced Latchup under System-Level ESD Test

Ming-Dou Ker and Sheng-Fu Hsu

Nanoelectronics and Gigascale Systems Laboratory  
Institute of Electronics, National Chiao-Tung University, Taiwan

**Abstract** – Different types of board-level noise filter networks are evaluated for their effectiveness to improve the immunity of CMOS ICs against transient-induced latchup (TLU) under system-level electrostatic discharge (ESD) test. By choosing proper components in each noise filter network, the TLU immunity of CMOS ICs can be greatly improved. All the experimental evaluations have been verified with the SCR test structures and the ring oscillator fabricated in a 0.25- $\mu\text{m}$  CMOS technology. Some of such board-level solutions can be further integrated into the chip design to effectively improve TLU immunity of CMOS IC products.

## I. Introduction

Recently, transient-induced latchup (TLU) has attracted much more reliability attentions than before in CMOS technology [1]-[8]. This tendency results from not only the progress of the more integrated functionality into a single chip, but also the strict requirements of reliability test standards such as system-level electrostatic discharge (ESD) test [9] for electromagnetic compatibility (EMC) regulation. Fig. 1 shows the measurement setup of the system-level ESD test with indirect contact-discharge test mode [9]. When the ESD gun zaps to the horizontal coupling plane (HCP), all CMOS ICs inside the equipment under test (EUT) will be disturbed due to the high ESD-coupled energy. Fig. 2 shows the measured  $V_{DD}$  transient waveform on one of the CMOS ICs inside the EUT with ESD voltage of -1000V. Clearly, the power lines (pins) of the CMOS IC no longer maintain their normal voltage levels (+2.5V), but acts as an underdamped sinusoidal voltage instead (with transient negative peak voltage of -10V). Such underdamped sinusoidal voltage on power or ground lines (pins) of CMOS ICs can easily trigger on TLU [10], even though such TLU-sensitive CMOS ICs have already met the requirements of the quasi-static latchup test standard [11].

In order to improve the TLU immunity of CMOS ICs,

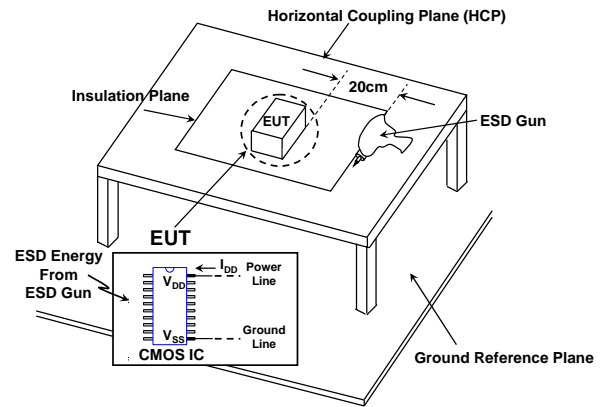


Fig. 1. The measurement setup of the system-level ESD test with indirect contact-discharge test mode [9].

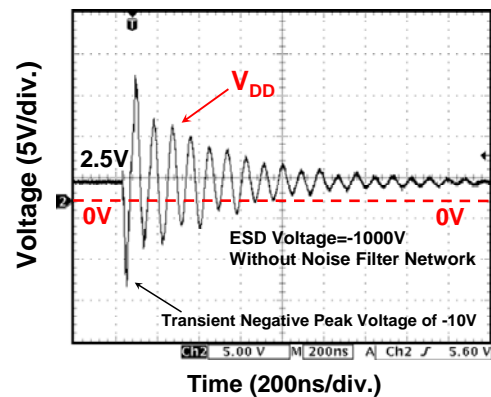


Fig. 2. The measured  $V_{DD}$  transient waveform on one of the CMOS ICs inside the EUT with ESD voltage of -1000V zapping on the HCP.

an intuitional solution is the usage of the board-level noise filter network between the noise sources and CMOS ICs to decouple, bypass, or absorb noise voltage (energy) which may initiate TLU. With ESD voltage of -1000V, Fig. 3 shows the measured  $V_{DD}$  transient waveform when a decoupling capacitance of  $0.1\mu\text{F}$  is added between  $V_{DD}$  and  $V_{SS}$  (ground) of the CMOS IC. Compared with the measured  $V_{DD}$  transient waveform in Fig. 2, the ESD-generated underdamped sinusoidal voltage noises on power lines can be immediately and greatly reduced (decoupled) by the decoupling capacitor, so the TLU immunity of the CMOS ICs can be improved.

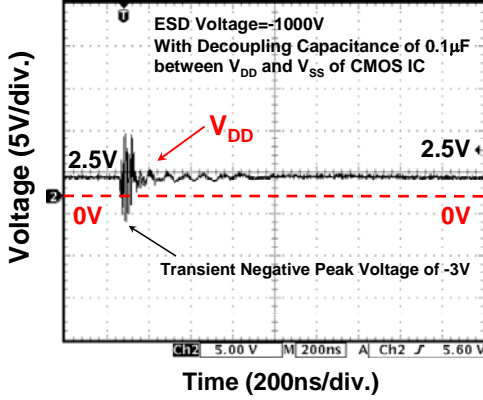


Fig. 3. With ESD voltage of -1000V, the measured  $V_{DD}$  transient waveform on the CMOS IC with decoupling capacitance of  $0.1\mu\text{F}$  between  $V_{DD}$  and  $V_{SS}$  (ground).

The purpose of this work is to develop a high efficiency board-level noise filter network for TLU prevention. Different types of noise filter networks are evaluated for their improvements on TLU immunity, including capacitor filter, ferrite bead, transient voltage suppressor (TVS), and several high-order noise filters such as LC-like (2nd-order) and  $\pi$ -section (3rd-order) filters. All the experimental results have been verified with the SCR test structures and the ring oscillator fabricated in a  $0.25\text{-}\mu\text{m}$  CMOS technology.

## II. Test Structure

SCR structure is used as the basic test structure for TLU measurements because the occurrence of latchup results from the inherent SCR of two cross-coupled BJTs, parasitic vertical PNP and lateral NPN BJTs, in bulk CMOS ICs [12]. The device cross-sectional view and layout top view of the SCR structure are sketched in Figs. 4(a) and 4(b), respectively. The geometrical parameters such as  $D$ ,  $S$ , and  $W$  represent the distances between well-edge and well (substrate) contact, anode and cathode, and the adjacent contacts,

respectively. All the SCR structures are fabricated by  $0.25\text{-}\mu\text{m}$  salicided CMOS technology.

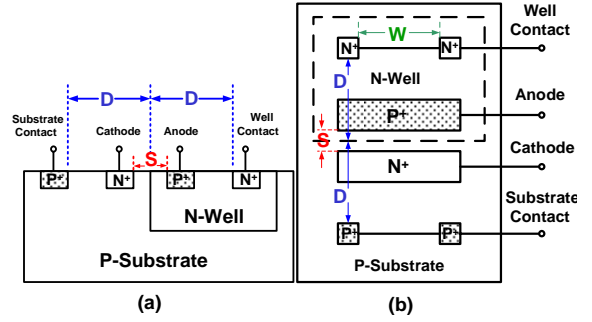


Fig. 4. (a) Device cross-sectional view, and (b) layout top view, of the SCR structure for TLU measurements.

## III. TLU Measurement Setup

During the system-level ESD test, we can only judge whether the EUT passes the required criterion through the abnormal function of EUT (e.g. EUT shuts down). Nevertheless, it is hard to directly evaluate the TLU immunity of single IC inside the EUT. To solve this issue, a component-level TLU measurement setup with bi-polar trigger waveform is used [13], as shown in Fig. 5. It has the advantage of easily evaluating the TLU immunity of single IC by the measured voltage/current waveforms through oscilloscope. More importantly, with the ability of generating an underdamped sinusoidal voltage, it can accurately simulate how a CMOS IC inside the EUT will be disturbed by the ESD-generated noises under the system-level ESD test. In this measurement setup, an ESD simulator is used to generate the underdamped sinusoidal trigger source,  $V_{\text{Charge}}$ . A capacitor with capacitance of  $200\text{pF}$  used in the machine model (MM) ESD test is employed as the charged capacitor. Noise filter network located between TLU-triggering

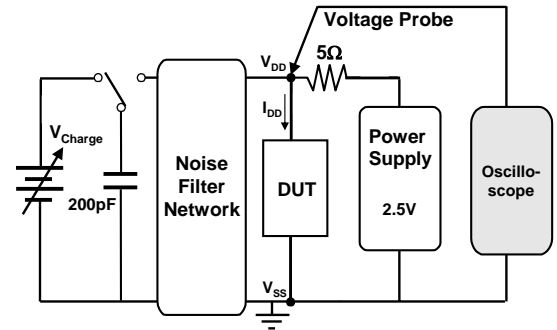


Fig. 5. A component-level TLU measurement setup with bi-polar trigger waveform [13]. It has the advantage of easily evaluating the TLU immunity of single IC.

source and the device under test (DUT) is used to decouple, bypass, or absorb noise voltage (energy) produced by TLU-triggering source. The DUT is the SCR structure shown in Fig. 4. The  $P^+$  anode and the  $N^+$  well contact of SCR are connected together to  $V_{DD}$ , whereas the  $N^+$  cathode and the  $P^+$  substrate contact are connected together to  $V_{SS}$  (ground).  $I_{DD}$  is the current flowing into the  $P^+$  anode and the  $N^+$  well contact of SCR. Furthermore, a small current-limiting resistance of  $5\Omega$  is used to avoid the possible electrical over-stress (EOS) damage under a high-current latchup state [14].

With the component-level TLU measurement setup in Fig. 5, Figs. 6(a) and 6(b) show the measured  $V_{DD}$  and  $I_{DD}$  transient responses with  $V_{Charge}$  of -2V and -7V, respectively. Both cases have no noise filter network between TLU-triggering source and the DUT (i.e. SCR with the specified device layout parameters of D

=16.6 $\mu$ m, S=20 $\mu$ m, and W=22.5 $\mu$ m). With a smaller  $V_{Charge}$  of -2V, TLU doesn't occur because  $I_{DD}$  doesn't significantly increase after applying the underdamped sinusoidal noise on  $V_{DD}$ , as shown in Fig. 6(a). However, with a larger  $V_{Charge}$  of -7V, TLU can be initiated, because  $I_{DD}$  significantly increases (up to 60mA), and  $V_{DD}$  is pulled down to the latchup holding voltage (1.8V), as shown in Fig. 6(b). In Fig. 6(a),  $V_{DD}$  acts as the underdamped sinusoidal voltage just as that under the system-level ESD test in Fig. 2. Thus, this component-level TLU measurement setup can be used to evaluate different types of board-level noise filter networks for their effectiveness to improve the TLU immunity of CMOS ICs under system-level ESD test.

## IV. Experimental Evaluations

Different types of noise filter networks are investigated for their effectiveness to improve the TLU immunity of the SCR structure, including: (1) capacitor filter, (2) LC-like filter, (3)  $\pi$ -section filter, (4) ferrite bead, (5) TVS, and (6) hybrid type filters based on the combinations with TVS and ferrite bead. The SCR structure for all cases has the specified layout parameters of D=16.6 $\mu$ m, S=20 $\mu$ m, and W=22.5 $\mu$ m.

### A. TLU Level of the SCR Structure without Noise Filter Network

Without the noise filter network, the component-level TLU measurement setup in Fig. 5 can be used to evaluate the TLU level of the SCR with various geometrical parameters. The TLU level is defined as the minimum positive (negative)  $V_{Charge}$  which can trigger on TLU. Thus, higher TLU level is better for DUT, because it means that the DUT is less sensitive to TLU under the system-level ESD test. However, the specified SCR structure (with D=16.6 $\mu$ m, S=20 $\mu$ m, and W=22.5 $\mu$ m) used in this work has a very low TLU level (positive (negative) level of +15V (-7V)). Actually, it was found out that all the SCR structures are rather susceptible to TLU (the magnitudes of both positive and negative TLU levels are all smaller than 20V) unless the SCR is latchup-free (i.e. latchup holding voltage is larger than the normal operating voltage of +2.5V). Thus, due to such low immunity to TLU, the noise filter network is indeed necessary to improve the TLU immunity of DUT through bypassing, decoupling, or absorbing noise voltage (energy) between the TLU-triggering source and DUT.

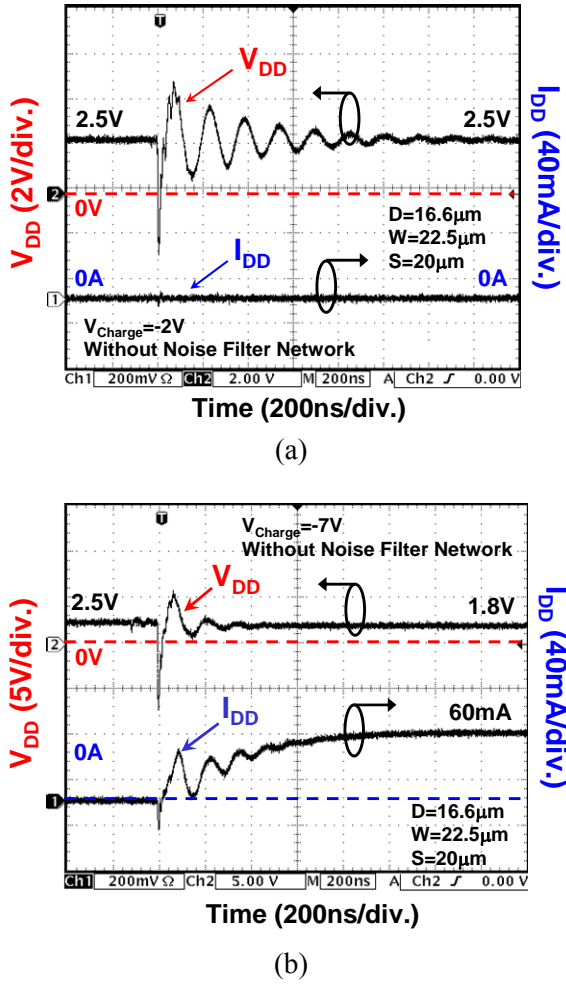


Fig. 6. The measured  $V_{DD}$  and  $I_{DD}$  transient responses of the SCR with  $V_{Charge}$  of (a) -2V, and (b) -7V. Both cases have no noise filter network between TLU-triggering source and the SCR.

## B. TLU Level of the SCR Structure with Noise Filter Network

### 1. Capacitor Filter, LC-Like Filter, and $\pi$ -Section Filter

Three types of noise filter networks: capacitor filter, LC-like filter, and  $\pi$ -section filter are depicted in Figs. 7(a), 7(b), and 7(c), respectively. Fig. 8 shows their improvements on both positive and negative TLU levels of the SCR structure.

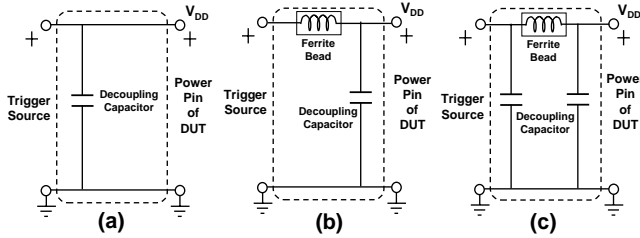


Fig. 7. Three types of noise filter networks are investigated for their improvements on TLU level of SCR: (a) capacitor filter, (b) LC-like filter, and (c)  $\pi$ -section filter.

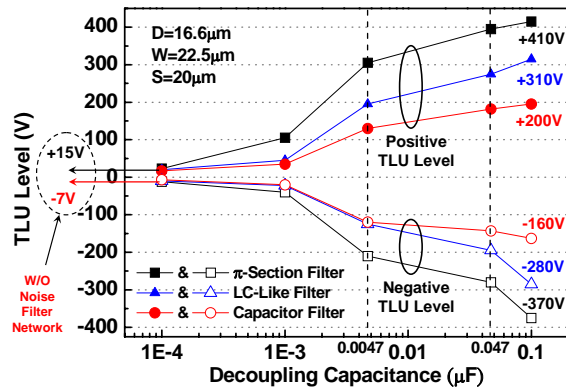


Fig. 8. The relations between the decoupling capacitance and the TLU level of the SCR under three types of noise filter networks: capacitor filter, LC-like filter, and  $\pi$ -section filter.

The ceramic disc capacitor with advantages of high rated working voltage (1kV), good thermal stability, and low loss at wide range of frequency is employed as the decoupling capacitor in the noise filter of Fig. 7(a). Decoupling capacitances widely ranging from 100pF to 0.1μF are used to investigate their improvements on TLU level of the SCR structure. With the aid of the capacitor filter, the positive TLU level can be significantly enhanced from +15V (without decoupling capacitor) to +200V (with decoupling capacitance of 0.1μF), as shown in Fig. 8. Similarly, the negative TLU level can be also significantly enhanced from -7V (without decoupling capacitor) to -160V (with decoupling capacitance of

0.1μF). Thus, by choosing a proper capacitance value, a simple 1st-order decoupling capacitor placed between  $V_{DD}$  and  $V_{SS}$  (ground) of CMOS ICs can be used to improve the TLU immunity of DUT under the system-level ESD test, no matter for the positive or the negative ESD voltage.

The ferrite bead, which is commonly used for absorbing RF energy, substitutes for inductor as a second-order LC-like filter component, as shown in Fig. 7(b). Here, a resistor-type ferrite bead (Part number: RH 3.5x9x0.8 with minimum impedance of 80Ω (120Ω) at 25MHz (100MHz)) is employed. Due to a higher insertion loss (2nd-order filter), such LC-like filter has better TLU level enhancements than that with the capacitor filter (1st-order filter). For example, the positive TLU level can be significantly enhanced from +15V (without decoupling capacitor) to +310V (with decoupling capacitance of 0.1μF), as shown in Fig. 8. Similarly, the negative TLU level can be also significantly enhanced from -7V (without decoupling capacitor) to -280V (with decoupling capacitance of 0.1μF). Thus, in order to achieve a high TLU level, the LC-like filter can be used to avoid an excessively or unreasonably large decoupling capacitance in a simple 1st-order capacitor filter.

A 3rd-order  $\pi$ -section filter is used to further enhance the TLU level of the SCR, as shown in Fig. 7(c). This  $\pi$ -section filter consists of a ferrite bead (the same one in Fig. 7(b)) and two decoupling capacitors with equal decoupling capacitance. With the highest insertion loss among the noise filter networks in Figs. 7(a), 7(b), and 7(c), the TLU level of SCR can be most greatly improved. For example, the positive TLU level can be significantly enhanced up to +410V (with decoupling capacitance of 0.1μF), as shown in Fig. 8. Similarly, the negative TLU level can be also significantly enhanced up to -370V (with decoupling capacitance of 0.1μF).

### 2. Ferrite Bead, TVS, and Hybrid Type Filters

Four other types of noise filter networks: ferrite bead, TVS, hybrid type I, and hybrid type II are depicted in Figs. 9(a), 9(b), 9(c), and 9(d), respectively. Fig. 10 shows their improvements on both positive and negative TLU levels of the SCR structure.

The ferrite bead absorbs RF energy while the noise-induced time-varied current flows through it. The resistor-type ferrite beads with three different minimum impedances at 25MHz are employed in this work: 35Ω, 50Ω, and 80Ω. However, a noise filter network with only ferrite bead alone doesn't perform



well enhancement on TLU level due to a worse energy-absorbing ability at frequency lower than 10MHz [15]. As a result, TLU level of the SCR structure will not be efficiently improved (the magnitudes of both positive and negative TLU levels are all lower than 25V), even though the minimum impedance of the ferrite bead at 25MHz is as high as 80Ω.

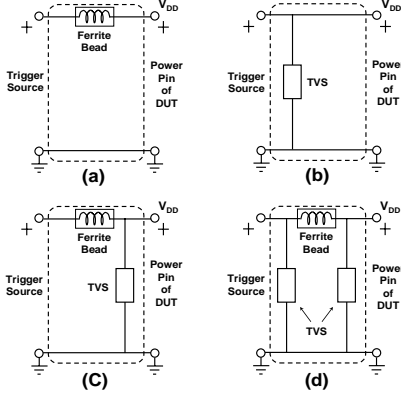


Fig. 9. Four other types of noise filter networks are investigated for their improvements on TLU level of SCR: (a) ferrite bead, (b) TVS, (c) hybrid type I, and (d) hybrid type II.

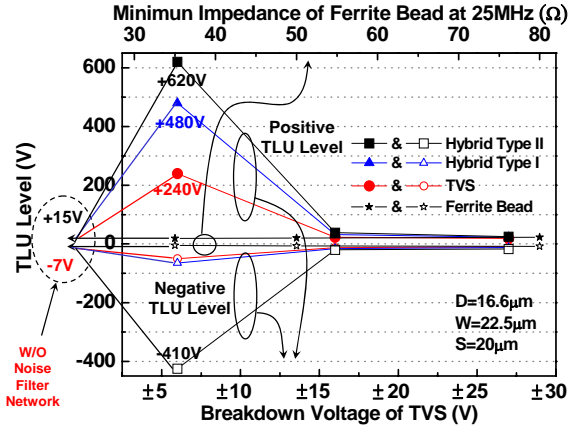


Fig. 10. The relations among the TLU level of SCR, minimum impedance of ferrite bead at 25MHz, and the breakdown voltage of TVS under four types of noise filter networks: ferrite bead, TVS, hybrid type I, and hybrid type II.

TVS, which is commonly used to bypass/decouple the high-frequency noises, is also considered for improving the TLU immunity of the SCR. The bidirectional-type TVS (Part number: P6KE series) with three different breakdown voltages,  $V_{BR}$ , ( $\pm 6.8V$ ,  $\pm 16V$ , and  $\pm 27V$ ) are employed in this work. As shown in Fig. 10, the TVS with breakdown voltage of  $\pm 16V$  or  $\pm 27V$  fail to improve the TLU level of the SCR (the magnitudes of both positive and negative TLU levels are all lower than 25V), because TLU occurs prior to the breakdown of such high- $V_{BR}$  TVS.

That is, the intrinsic (without noise filter network) TLU level of SCR (positive and negative TLU level of  $+15V$  and  $-7V$ ) is smaller than the  $V_{BR}$  of TVS ( $\pm 16V$  and  $\pm 27V$ ). Thus, only the TVS with  $V_{BR}$  lower than the intrinsic TLU level of DUT can effectively enhance the TLU level. For example, the positive (negative) TLU level can be enhanced up to  $+240V$  ( $-50V$ ).

Hybrid type filters consisting of both ferrite bead (minimum impedance of 80Ω at 25MHz) and TVS (with different  $V_{BR}$ ) are also evaluated for their improvements on TLU level of the SCR, as shown in Figs. 9(c) and 9(d). Hybrid types I and II are the counterparts of the LC-like and  $\pi$ -section filters where the TVS substitutes for the decoupling capacitor. As shown in Fig. 10, only the hybrid type filters with a low- $V_{BR}$  ( $\pm 6.8V$ ) TVS can efficiently improve the TLU level. In addition, because such higher-order hybrid type filters provide the higher insertion loss, they can enhance the TLU level of SCR more greatly than ferrite bead or TVS alone. For example, for hybrid type filters with a low- $V_{BR}$  ( $\pm 6.8V$ ) TVS, hybrid type I (II) can greatly enhance the positive TLU level up to  $+480V$  ( $+620V$ ), and enhance the negative TLU levels up to  $-65V$  ( $-410V$ ).

Through investigating different types of noise filter networks for their improvements on TLU levels in Figs. 8 and 10, it can be found out TVS (hybrid type I) doesn't improve the negative TLU level as greatly as the 1st-order capacitor filter (LC-like filter). For example, the negative TLU level can be greatly enhanced up to  $-160V$  ( $-280V$ ) for 1st-order capacitor filter (LC-like filter) with decoupling capacitance of  $0.1\mu F$ , but only up to  $-50V$  ( $-65V$ ) for TVS (hybrid type I) with a low  $V_{BR}$  of  $\pm 6.8V$ . Thus, the decoupling capacitor is better than TVS for being a noise-bypassing component in the noise filter networks, because it not only can enhance negative TLU level more efficiently but also is compatible to CMOS technology for integrating the noise filter into chips.

## V. Verification on Real Circuits

A 100-MHz ring oscillator with 101-stage inverter chain and 7-stage taper buffer fabricated in a  $0.25\text{-}\mu m$  CMOS technology is used as a real circuit to investigate different types of noise filter networks for their enhancements on TLU levels. The schematic diagram and layout top view of the ring oscillator are shown in Figs. 11(a) and 11(b), respectively. The geometrical parameters such as X, Y, and Z represent the distances between well-edge and well (substrate)

contact, source (drain) regions of PMOS and NMOS, and the adjacent well contacts (substrate contacts), respectively. The ring oscillator is treated as the DUT in Fig. 5, where the  $N^+$  well contact and the  $P^+$  source of PMOS are connected together to  $V_{DD1}$ , but the  $P^+$  substrate contact and the  $N^+$  source of NMOS are connected to  $V_{SS}$  (ground). In addition, the layout parameters of all the taper buffers are fixed, and the power line of the taper buffer ( $V_{DD2}$ ) with a +2.5V power supply voltage is separated from the power line of the inverter chain ( $V_{DD1}$ ) to evaluate the TLU level of the inverter chain but not the taper buffer. The parasitic SCR structure within the ring oscillator consists of the  $P^+$  source of PMOS (anode), N-well, P-substrate, and the  $N^+$  source of NMOS (cathode). In real situation under the system-level ESD test, TLU can be triggered on by ESD-generated underdamped sinusoidal noises coupled to  $V_{DD1}$  of the ring oscillator, so that rapid-increasing current ( $I_{DD1}$ ) will be conducted through a low-impedance path between  $V_{DD1}$  and ground, eventually probably burning out the chip due to over heating. Thus, the component-level TLU measurement setup in Fig. 5 can be used to simulate system-level ESD test by applying the underdamped sinusoidal noises on  $V_{DD1}$ , and to further evaluate different types of board-level noise filter networks for their effectiveness on the TLU immunity of the ring oscillator under system-level ESD test.

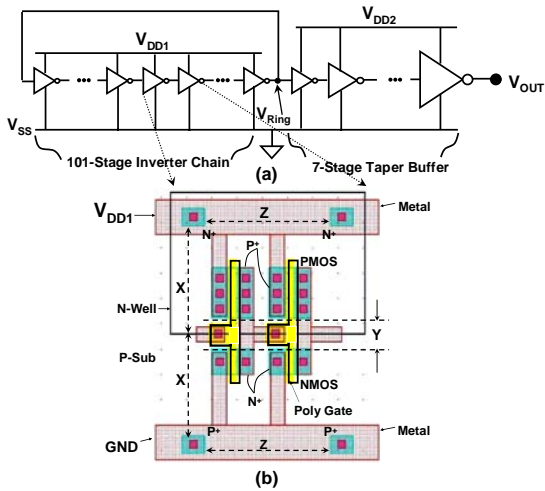


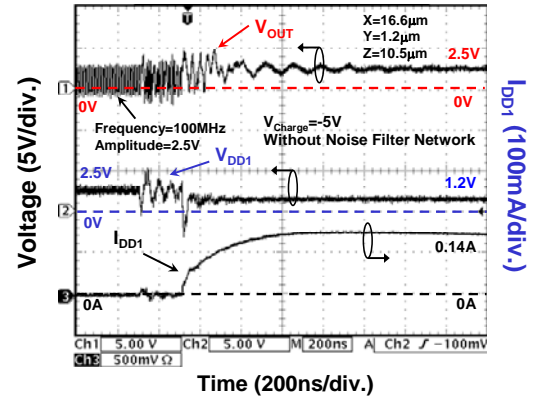
Fig. 11. (a) Schematic diagram, and (b) layout top view, of the ring oscillator fabricated in a 0.25- $\mu m$  CMOS process.

To consider the worst case of evaluating TLU level, the ring oscillator with layout parameters of  $X=16.6\mu m$ ,  $Y=1.2\mu m$ , and  $Z=10.5\mu m$  is used. The anode to cathode spacing ( $Y$ ) of  $1.2\mu m$  is the minimum allowed distance according to the foundry's design rule. In addition, a large  $X$  ( $Z$ ) of  $16.6\mu m$

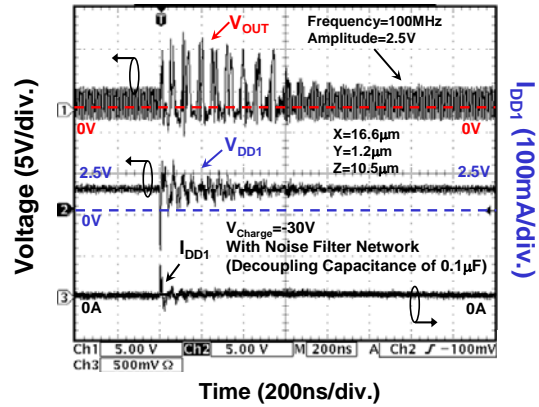
( $10.5\mu m$ ) makes sure a large parasitic well or substrate resistance of the parasitic SCR within ring oscillator, so that this ring oscillator has the minimum latchup triggering current or holding voltage (i.e. most sensitive to latchup).

## A. TLU Transient Waveforms of the Ring Oscillator

Figs. 12(a) and 12(b) show the measured  $V_{DD1}$ ,  $I_{DD1}$ , and  $V_{OUT}$  transient responses for the ring oscillator without or with the noise filter network, respectively. For the ring oscillator without the noise filter network, TLU can be triggered on even if the  $V_{Charge}$  is as low as -5V, as shown in Fig. 12(a). Once TLU is initiated,  $I_{DD1}$  will significantly increase (0.14A) with the pull-down  $V_{DD1}$  (1.2V) due to a low-impedance latching path between  $V_{DD1}$  and ground. Thus, the ring oscillator fails to function correctly, causing the output voltage of the ring oscillator,  $V_{Ring}$ , to be pulled down to ground. So,  $V_{OUT}$  is kept at +2.5V after the 7-stage taper buffer.



(a)



(b)

Fig. 12. The measured  $V_{DD1}$ ,  $I_{DD1}$ , and  $V_{OUT}$  transient responses for the ring oscillator (a) without, and (b) with, the noise filter network.

For the ring oscillator with the noise filter network (capacitor filter with decoupling capacitance of  $0.1\mu\text{F}$ ), TLU doesn't occur even though the  $V_{\text{Charge}}$  is as high as  $-30\text{V}$ , as shown Fig. 12(b). Clearly, with the aid of the decoupling capacitor to decouple TLU-triggering noises to  $V_{\text{DD1}}$ , the ring oscillator still maintains its normal function after the TLU-triggering disturbance.

## B. TLU Level of the Ring Oscillator with Noise Filter Network

Fig. 13 shows the relations between the decoupling capacitance and the TLU level of the ring oscillator under three types of noise filter networks: capacitor filter, LC-like filter, and  $\pi$ -section filter. With the aid of the 1st-order capacitor filter ( $0.1\mu\text{F}$ ), the positive (negative) TLU level can be enhanced from  $+8\text{V}$  ( $-5\text{V}$ ) to  $+70\text{V}$  ( $-60\text{V}$ ). In addition, higher-order noise filter networks such as LC-like filter and  $\pi$ -section filter can be used to achieve higher TLU level. For example, with decoupling capacitance of  $0.1\mu\text{F}$ , the positive (negative) TLU level can be enhanced up to  $+90\text{V}$  ( $-85\text{V}$ ) for LC-like filter, and up to  $+210\text{V}$  ( $-155\text{V}$ ) for  $\pi$ -section filter.

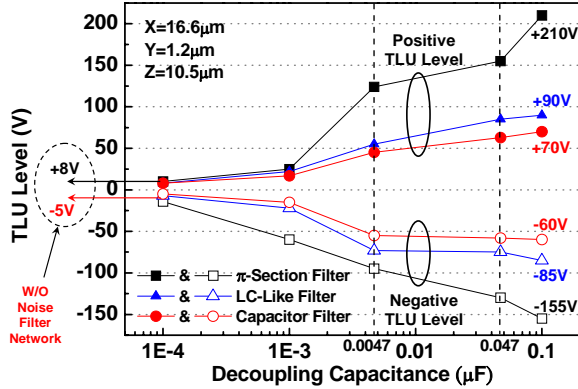


Fig. 13. The relations between the decoupling capacitance and the TLU level of the ring oscillator under three types of noise filter networks: capacitor filter, LC-like filter, and  $\pi$ -section filter.

Fig. 14 shows the relations among the TLU level of the ring oscillator, minimum impedance of ferrite bead at 25MHz, and the breakdown voltage of TVS under four types of noise filter networks: ferrite bead, TVS, hybrid type I, and hybrid type II. Due to a worse energy-absorbing ability of ferrite bead at frequency lower than 10MHz [15], the TLU level will not be efficiently improved by only ferrite bead alone (the magnitudes of both positive and negative TLU levels are all lower than 25V), even though the minimum impedance of the ferrite bead at 25MHz is as high as

$80\Omega$ . In addition, TVS with breakdown voltage of  $\pm 16\text{V}$  or  $\pm 27\text{V}$  fail to improve the TLU level because TLU occurs prior to the breakdown of such high- $V_{\text{BR}}$  TVS. Thus, only the low- $V_{\text{BR}}$  TVS ( $\pm 6.8\text{V}$ ) can efficiently enhance the TLU level. For example, the positive (negative) TLU level can be enhanced up to  $+30\text{V}$  ( $-33\text{V}$ ). If such low- $V_{\text{BR}}$  TVS is further used in hybrid type filters, TLU level can be greatly enhanced. As shown in Fig. 14, the positive (negative) TLU level is only  $+30\text{V}$  ( $-33\text{V}$ ) for TVS alone, but it can be enhanced up to  $+40\text{V}$  ( $-42\text{V}$ ) for hybrid type I, and up to  $+100\text{V}$  ( $-125\text{V}$ ) for hybrid type II.

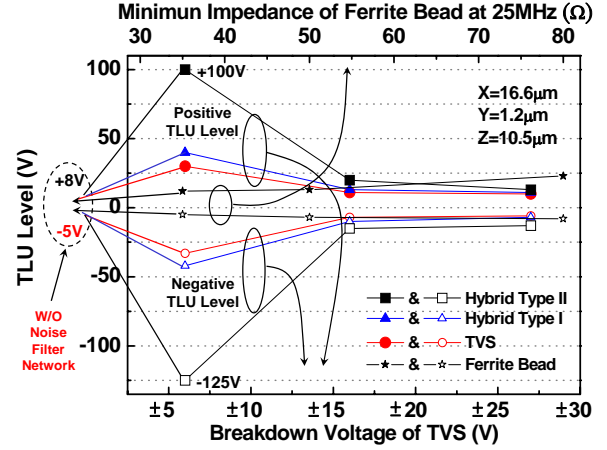


Fig. 14. The relations among the TLU level of the ring oscillator, minimum impedance of ferrite bead at 25MHz, and the breakdown voltage of TVS under four types of noise filter networks: ferrite bead, TVS, hybrid type I, and hybrid type II.

Among Figs. 8, 10, 13, and 14, through investigating the TLU level enhancements by different types of noise filter networks for SCR and for ring oscillator, the TLU levels of the ring oscillator are overall smaller than those of the SCR. The reason is that the ring oscillator has smaller DC latchup trigger current (voltage) due to both the layout geometrical parameters and the larger total p-n junction area (larger junction leakage current). Thus, the TLU level enhancements by different types of noise filter networks strongly depend on the DUT. As a result, the DC latchup characteristics of DUT should be identified in advance when the board-level noise filter networks are designed to improve the TLU immunity of DUT under the system-level ESD test.

## VI. Conclusion

By choosing proper components in each noise filter network, the TLU immunity of CMOS ICs under the system-level ESD stresses can be greatly improved. From the experimental results, the decoupling

capacitor is better than TVS for being a noise-bypassing component in the noise filter networks, because it not only can enhance negative TLU level more efficiently, but also is compatible to CMOS technology for integrating the noise filter into chips. In addition, the TLU level enhancements by different types of noise filter networks strongly depend on the DUT. Thus, the DC latchup characteristics of DUT should be identified in advance when the board-level noise filter networks are designed to improve the TLU immunity of DUT under the system-level ESD test. To improve TLU immunity of electronic products, both board-level solutions and chip-level solutions should be adopted to meet the applications with high system-level ESD specification.

## References

- [1] S. Voldman, "Latch-up – it's back," in *Threshold Newsletter*, ESD Association, Sep./Oct., 2003.
- [2] S. Bargstädt-Franke, W. Stadler, K. Esmark, M. Streibl, K. Domanski, H. Gieser, H. Wolf, and W. Bala, "Transient latch-up: experimental analysis and device simulation," in *Proc. EOS/ESD Symp.*, 2003, pp. 70-78.
- [3] J. T. Mechler, C. Brennan, J. Massucco, R. Rossi, and L. Wissel, "Contention-induced latchup," in *Proc. IRPS*, 2004, pp. 126–129.
- [4] K. Domanski, S. Bargstadt-Franke, W. Stadler, M. Streibl, G. Steckert, and W. Bala, "Transient-LU failure analysis of the ICs, methods of investigation and computer aided simulations," in *Proc. IRPS*, 2004, pp. 370–374.
- [5] K. Chatty, P. Cottrell, R. Gauthier, M. Muhammad, F. Stellari, A. Weger, P. Song, and M. McManus, "Model-based guidelines to suppress cable discharge event (CDE) induced latchup in CMOS ICs," in *Proc. IRPS*, 2004, pp. 130–134.
- [6] K. Domanski, S. Bargstädt-Franke, W. Stadler, U. Glaser, and W. Bala, "Development strategy for TLU-robust products," in *Proc. EOS/ESD Symp.*, 2004, pp. 299-307.
- [7] G. Boselli, V. Reddy, and C. Duvvury, "Latch-up in 65nm CMOS technology: a scaling perspective," in *Proc. IRPS*, 2005, pp. 137–144.
- [8] S. Voldman, "Latchup and the domino effect," in *Proc. IRPS*, 2005, pp. 145–156.
- [9] IEC 61000-4-2 Standard, "EMC – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test," IEC, 2001.
- [10] M.-D. Ker and S.-F. Hsu, "Transient-induced latchup in CMOS technology: physical mechanism and device simulation," in *IEDM Tech. Dig.*, 2004, pp. 937–940.
- [11] EIA/JEDEC Standard No. 78, "IC Latch-up Test," Electronic Industries Association, 1997.
- [12] R. Troutman, *Latchup in CMOS Technology: The Problem and the Cure*, Kluwer Publications, New York, 1986.
- [13] I. Morgan, C. Hatchard, and M. Mahanpour, "Transient latch-up using an improved bi-polar trigger," in *Proc. EOS/ESD Symp.*, 1999, pp. 190–202.
- [14] M.-D. Ker and S.-F. Hsu, "Evaluation on efficient measurement setup for transient-induced latchup with bi-polar trigger," in *Proc. IRPS*, 2005, pp. 121–128.
- [15] M. I. Montrose, *Printed Circuit Board Design Techniques for EMC Compliance*, IEEE Press, 2000.