ESD Protection Design with the Low-Leakage-Current Diode String for RF Circuits in BiCMOS SiGe Process

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Abstract – The Low-Leakage-Current Diode String (LLCDS) in a BiCMOS SiGe process is proposed for on-chip ESD protection design in RF circuits. With an additional bias resistance, a voltage is applied to the n-well of diode string resulting in a significant reduction in the leakage current of the diode string under normal circuit operating conditions. The leakage current of LLCDS can be minimized under some selected bias resistance, which can be calculated from the derived equations. Such LLCDS can be used in the power-rail ESD clamp circuit, in cooperation with the small double diodes in the I/O pads, to achieve whole-chip ESD protection for RF ICs in SiGe process.

I. Introduction

The Silicon-Germanium (SiGe) BiCMOS technology with great RF performance of SiGe HBT has been recognized as one of the best chip solutions for broadband and wireless systems. For RF ESD protection design, in order to protect the internal circuits from ESD damage, the power-rail ESD clamp needs to be designed along with the small input ESD diodes to achieve whole-chip ESD protection [1]-[3]. Fig. 1 shows the typical RF ESD protection scheme in which the input ESD diodes are co-designed with the power-rail ESD clamp circuit. The ESD stress may have positive or negative voltages on an input (or output) pad with respect to the grounded VDD or VSS pins. For a comprehensive ESD verification, the pin-to-pin ESD stress and the VDD-to-VSS ESD stress, have been specified to verify the whole-chip ESD robustness. So, the ESD clamp circuit between the power rails is very helpful for protecting an RF I/O pin and the RF core circuits against ESD damage [3]. The diode string is one solution that has been applied in the power-rail ESD clamp circuits [4], [5]. The diode string is operated in forward-biased condition to discharge ESD current. Thus, it can sustain a very high ESD level in a small silicon area.

However, the main drawback for using the diode string as the power-rail ESD clamp circuit is the leakage current, especially at high temperatures. A parasitic vertical p-n-p bipolar transistor exists in the conventional P+/N-well diode with the common grounded P-type substrate. This parasitic vertical p-n-p bipolar transistor (BJT) causes high leakage current along the diode string [4]-[6], especially at high temperatures. Some modified designs on the diode string to reduce leakage current have been reported in [5], which are referred to as the Cladded diode string, Boosted diode string, and Cantilever diode string. But, those designs, which have been verified in bulk CMOS technology, still have high leakage current (~mA) at the temperature of 125°C [6]. In the SiGe process, the deep trench (DT) has been used to reduce the substrate leakage current of the diode string [7], [8]. With the DT and n+ buried layer in SiGe process, the parasitic vertical p-n-p BJT in the diode string was connected with a base-emitter-short configuration [8], which results in a lower substrate leakage current than that of the conventional P+/N-well diode in CMOS process.

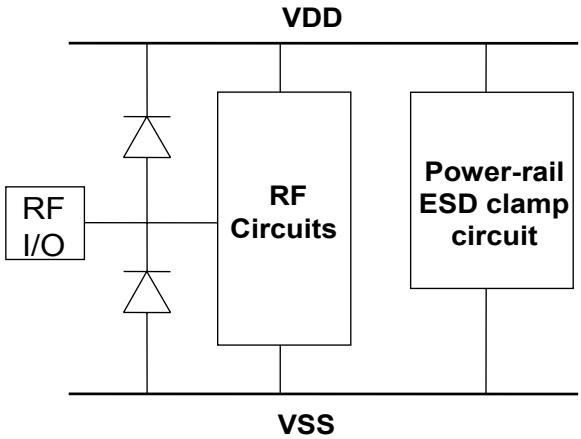

Fig. 1 The typical RF ESD protection scheme with co-designed input ESD diodes and the power-rail ESD clamp circuit. The diode string has been applied in the power-rail ESD clamp circuit.

In this work, two kinds of power-rail ESD clamp circuits for RF ESD protection design in BiCMOS SiGe technology are proposed. One is the Low-Leakage-Current Diode String (LLCDS), and another is the LLCDS-triggered SiGe HBT. In the new proposed LLCDS, an extra bias is applied to the deep N-well of the LLCDS to minimize the leakage current. The characteristics of these two new power-rail ESD clamp circuits are compared with that of the conventional diode string.

II. Review on the Diode Strings

A. Conventional Diode String

The cross-sectional view of the conventional diode string is shown in Fig. 2. Because of the parasitic vertical p-n-p transistor, the diode string causes base-emitter debiasing of succeeding stages due to current being diverted into the substrate via the collectors. If the gain of the parasitic vertical p-n-p transistor is more than one, the increase of stacked diodes in the diode string doesn't linearly increase the total blocking voltage across the diode string. This implies that more diodes would be needed to support the desired blocking voltage. To reduce the leakage current of the conventional diode string, three modified designs had been reported in [4], [5].

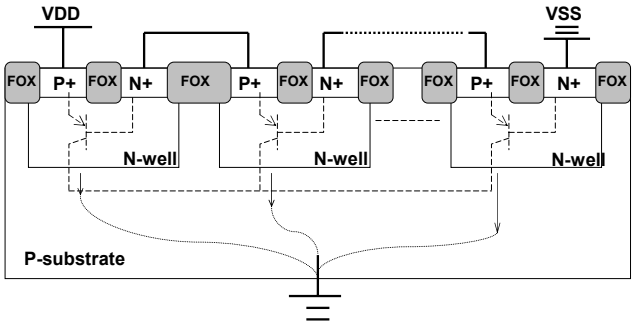

Fig. 2 The cross-sectional view of the conventional diode string.

B. Modified Diode String to Reduce Leakage Current

A modified design to reduce the leakage current by using triple-well technologies had been reported in [7]. Fig. 3 shows the cross-sectional view of the n-stage triple-well diode string with its parasitic base-emitter tied p-n-p bipolar transistors. Operating in the forward-biased condition, diode current will flow through the P-well regions with holes not being injected into the base region of the parasitic vertical p-n-p bipolar transistors because of the base-emitter tied configuration, which suppresses the substrate leakage current. The substrate leakage current can thus be kept very small before the triple-well diode string turns on. It results from the parasitic base-emitter junction being tied p-n-p bipolar transistor.

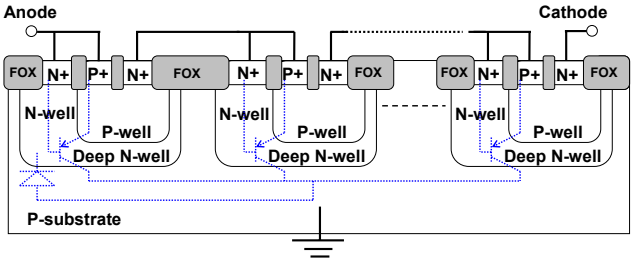

Fig. 3 The cross-sectional view of the n-stage triple-well diode string and its parasitic base-emitter tied p-n-p bipolar transistors.

III. Design on LLCDS

The cross-sectional view of the new proposed of low-leakage-current diode string (LLCDS) in a 0.18-μm BiCMOS SiGe process is shown in Fig. 4. Compared with the conventional P+/N-well diode string, this structure has a deep N-well to isolate the P-well from the common P-substrate. An extra bias through the resistor R is applied to the deep N-well to minimize the leakage current into the substrate. The equivalent circuit of LLCDS with the parasitic n-p-n BJTs is shown in Fig. 5. In this design, the deep N-well of every diode in the LLCDS is connected to VDD through a bias resistance R. The connection of deep N-well to VDD causes the parasitic n-p-n BJTs in the LLCDS to be slightly turned on. The current generated from the slightly turned-on n-p-n BJT in the diode will flow into the next diode of LLCDS, but not to the common P-substrate. So, the leakage current into the substrate is not increased by this new design.

The bias resistance (R) is connected between the bias voltage and the deep N-well to control the total leakage current through LLCDS. The total current flowing into LLCDS should be equal to the total current flowing out the device. The total leakage current of the LLCDS can be derived as

$$I_{total\ leakage} = I_{C1} + I_{C2} + I_{C3} + I_{C4} + I_A\ , \qquad (1)$$

where all currents have been indicated in Fig. 5. Under normal circuit operating conditions, the LLCDS is designed to be kept off with the leakage current as small as possible. So, in this condition, the BJT 1 is in the saturation mode and BJTs 2, 3 and 4 are in the active mode. The emitter and collector currents of each BJT can be expressed in terms of its base-emitter (V_{BE}) and base-collector (V_{BC}) voltages.

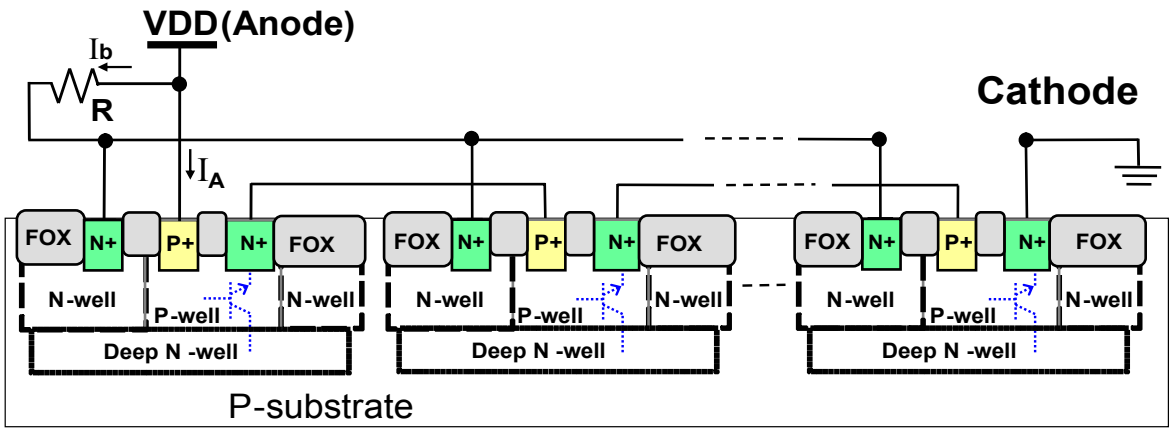

Fig. 4 The cross-sectional view of the proposed LLCDS realized in a 0.18-μm BiCMOS SiGe process.

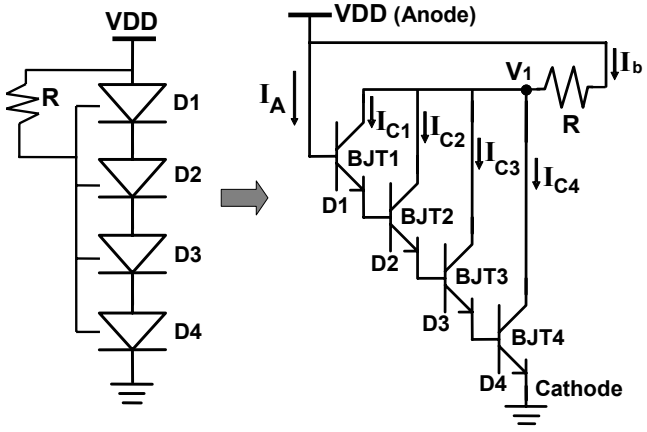

Fig. 5 The equivalent circuit of the LLCDS with 4 stacked diodes in 0.18-μm BiCMOS SiGe process.

The emitter and collector currents of each parasitic n-p-n BJT in the LLCDS and the voltage equations in the equivalent circuit are derived as

$$I_E = a_{11}\left(e^{qV_{BE}/kT}-1\right) - a_{12}\left(e^{qV_{BC}/kT}-1\right) \quad (2)$$

$$I_C = a_{21}\left(e^{qV_{BE}/kT}-1\right) - a_{22}\left(e^{qV_{BC}/kT}-1\right) \quad (3)$$

$$V_{BC1} = R \times I_b \quad (4)$$

$$V_{BEn} = (kT/q)\left[\ln(I_{En}+1)-\ln(I_s)\right], \text{ for } n = 1 \sim 4 \quad (5)$$

$$V_{DD} = \sum_{n=1}^{4}(kT/q)\left[\ln(I_{En}+1)-\ln(I_s)\right] \quad (6)$$

According to above equations (4)-(6), the emitter and collector currents of BJT1 can be derived in the following.

$$I_{E1} = a_{11}\left((I_{E1}+1)/I_s-1\right) - a_{12}\left(e^{qRI_b/kT}-1\right) \quad (7)$$

$$I_{C1} = a_{21}\left((I_{E1}+1)/I_s-1\right) - a_{22}\left(e^{qRI_b/kT}-1\right) \quad (8)$$

where

$$a_{11} = qA\left[D_p n_i^2/N_B W + D_E n_{EO}/L_E\right], \quad (9)$$

$$a_{12} = qAD_p n_i^2/N_B W, \quad (10)$$

$$a_{21} = qAD_p n_i^2/N_B W, \text{ and} \quad (11)$$

$$a_{22} = qA\left[D_p n_i^2/N_B W + D_C n_{CO}/L_C\right]. \quad (12)$$

From the equivalent circuit, the collector current of BJT2 is the β gain relation with the emitter of BJT1.

$$I_{C2} = \beta_2 I_{B2} = \beta_2 I_{E1} \quad (13)$$

The value of β in BJT2 can be determined by its base-emitter voltage.

$$\beta_2 = \frac{qN_B L_p^2}{\varepsilon_s (V_{bi}-V_{BE2})} \quad (14)$$

Similarly, the collector currents of the BJT3 and BJT4 can be derived.

$$I_{C3} = \beta_3 I_{B3} = \beta_2\beta_3 I_{E1}, \quad (15)$$

$$\text{where } \beta_3 = \frac{qN_B L_p^2}{\varepsilon_s (V_{bi}-V_{BE3})}. \quad (16)$$

$$I_{C4} = \beta_4 I_{B4} = \beta_2\beta_3\beta_4 I_{E1}, \quad (17)$$

$$\text{where } \beta_4 = \frac{qN_B L_p^2}{\varepsilon_s (V_{bi}-V_{BE4})}. \quad (18)$$

The value of the current flow through the bias resistance R should be the sum of the four collector currents.

$$I_{C1}+I_{C2}+I_{C3}+I_{C4} = I_{C1} + \left(\beta_2+\beta_2\beta_3+\beta_2\beta_3\beta_4\right) I_{E1} \quad (19)$$

Finally, the total leakage current can be expressed by the following equation as a function of bias resistance R and the current gain (β) of each BJT. A minimum value for the leakage current exists, when the equation differentiated with respect to R equals zero. In this manner, the optimized value of R to achieve the minimized leakage current can be found.

$$I_{Total\ Leakage} = \left(1+\beta_2+\beta_2\beta_3+\beta_2\beta_3\beta_4\right) I_{E1}$$
$$= \left(1+\beta_2+\beta_2\beta_3+\beta_2\beta_3\beta_4\right) \times$$
$$\left[\left(a_{11}/I_s - a_{11}\right) - a_{12}\left(e^{qRI_b/kT}-1\right)\right] / \left(1-a_{11}/I_s\right) = f(R) \quad (20)$$

IV. LLCDS-Triggered HBT

The power-rail ESD clamp circuit realized with diode-triggered HBT in SiGe BiCMOS process had been reported [9], as shown in Fig. 6. However, the leakage (or standby) current of this circuit will be the main concern for low-power applications. To further reduce the total leakage current, the second design of the power-rail ESD clamp circuit with the LLCDS-triggered SiGe HBT is shown in Fig. 7(a). The corresponding equivalent circuit of this LLCDS-triggered SiGe HBT is shown in Fig. 7(b).

The equation of the total leakage current through the LLCDS-triggered SiGe HBT can be derived in the same way. For the SiGe HBT, the base current and the collector current can be expressed as the function of V_{BE}. Considering the LLCDS part in this second power-rail ESD clamp circuit, the parasitic BJT1 will be operated in the saturation region and the parasitic BJT 2, 3 and 4 will be operated in the active region under normal operating conditions. The collector and emitter currents of each BJT and the circuit equations in the equivalent circuit can be derived in the following.

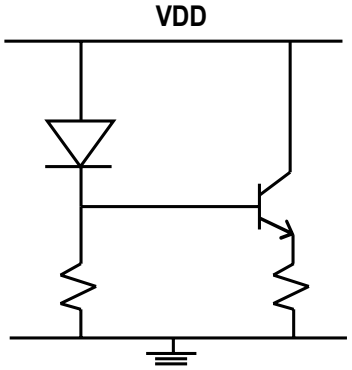

Fig. 6 The power-rail ESD clamp circuit with diode-triggered HBT in SiGe BiCMOS process [9].

$$I_E = a_{11}\left(e^{qV_{BE}/kT}-1\right) - a_{12}\left(e^{qV_{BC}/kT}-1\right) \quad (21)$$

$$I_C = a_{21}\left(e^{qV_{BE}/kT}-1\right) - a_{22}\left(e^{qV_{BC}/kT}-1\right) \quad (22)$$

$$V_{BC1} = R \times I_b \quad (23)$$

$$V_{BEn} = \left(kT/q\right)\left[\ln\left(I_{En}+1\right) - \ln\left(I_s\right)\right], \text{ for } n = 1 \sim 4 \quad (24)$$

$$V_{DD} - \sum_{n=1}^{4}\left(kT/q\right)\left[\ln\left(I_{En}+1\right) - \ln\left(I_s\right)\right] = V_{BE(HBT)} \quad (25)$$

Equation (25) is different to that of the pure LLCDS, because the cathode of LLCDS is not connected to ground in this second design but connected to the base of HBT. With such a circuit connection, all current of LLCDS will flow into the base of HBT and the resistance (Ro).

Finally, the equation of total leakage current along the LLCDS-triggered SiGe HBT can be expressed in the following.

$$I_{total\ leakage} = V_{BE}(R, R_o) / R_o + I_B + I_C \quad (26)$$

where $I_B = \dfrac{qAD_{pe}n_i^2}{W_E N_{de}} e^{qV_{BE}(R,R_o)/kT}$, and (27)

$$I_C = \frac{qAD_{nb}n_i^2}{W_B N_{ab}} e^{qV_{BE}(R,R_o)/kT}. \quad (28)$$

The D_{pe} is the diffusion coefficient of emitter, N_{de} is the emitter doping, D_{nb} is the diffusion coefficient of base, and N_{ab} is the base doping concentration.

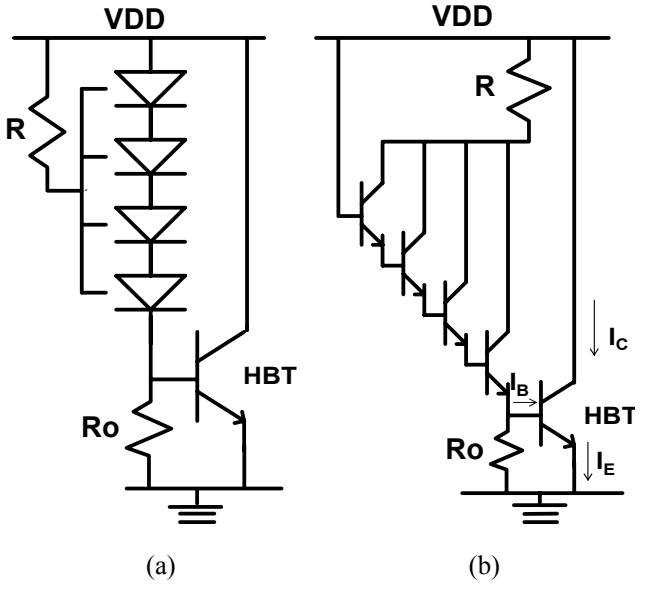

Fig. 7 (a) The second design of power-rail ESD clamp circuit realized with the LLCDS-triggered SiGe HBT and (b) its corresponding equivalent circuit.

The resistance (Ro) between the base node of SiGe HBT and ground will affect the total leakage current. As a result, there are two design parameters, R and Ro, in this circuit for minimizing the leakage current.

V. Experimental Results

These two new designs of power-rail ESD clamp circuits have been fabricated in a 0.18-μm BiCMOS SiGe process. The conventional diode string shown in Fig. 2 is also fabricated in the same process with the same diode layout dimensions for comparison. During the measurement, the cathode of LLCDS and the p-substrate are grounded by two separated channels, so that the cathode current and the substrate current can be monitored separately. The DC characteristics of the conventional diode string and the LLCDS with different numbers (n= 2, 3, and 4) of stacked diodes are compared in Fig. 8 and Fig. 9, respectively.

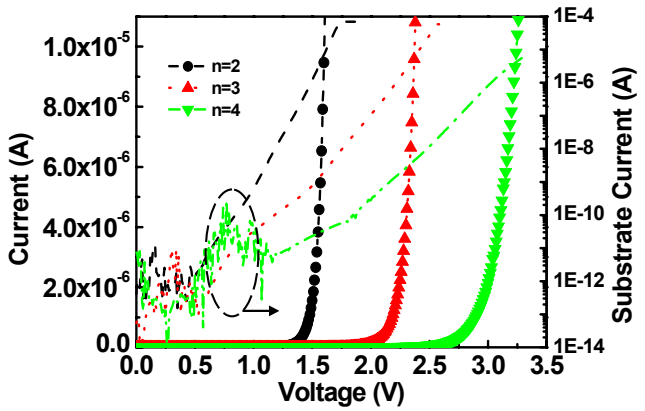

Fig. 8 The DC I-V characteristics of the conventional diode string with different numbers (n= 2, 3, and 4) of stacked diodes under the temperature of 25 °C.

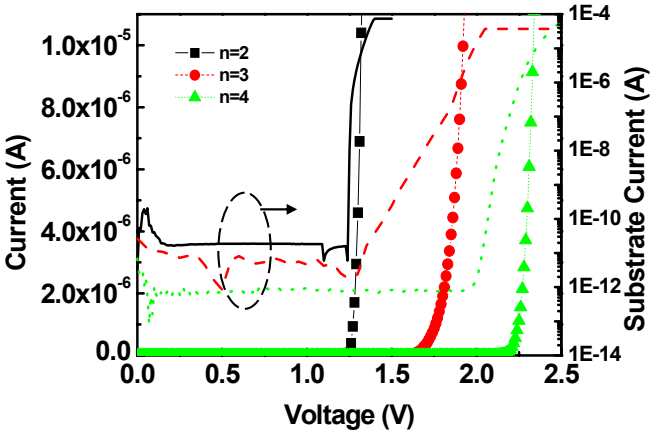

Fig. 9 The DC I-V characteristics of the LLCDS with different numbers (n= 2, 3, and 4) of stacked diodes under the temperature of 25 °C and the bias resistance of 10 kΩ.

The LLCDS has a lower substrate leakage current than that of the conventional diode string, because there is a bias applied trough the resistance R into the deep N-well. For the circuit applications with VDD of 1.8V, the substrate leakage current in LLCDS (Fig. 9) with 4-stacked diodes can be two-order of magnitude smaller than that of the conventional diode string (Fig. 8).

In Fig. 10, the relationship between bias resistance (R) and the total leakage current through the LLCDS with four stacked diodes (n=4) is measured at different temperatures. The total leakage current through the diode string (n=4) is increased when the temperature is increased from 75 °C to 125 °C. However, the total leakage current can be minimized by selecting the suitable bias resistance. From the measured results, the LLCDS (n=4) has a minimized leakage current at 125 °C by using a bias resistance of 10 kΩ.

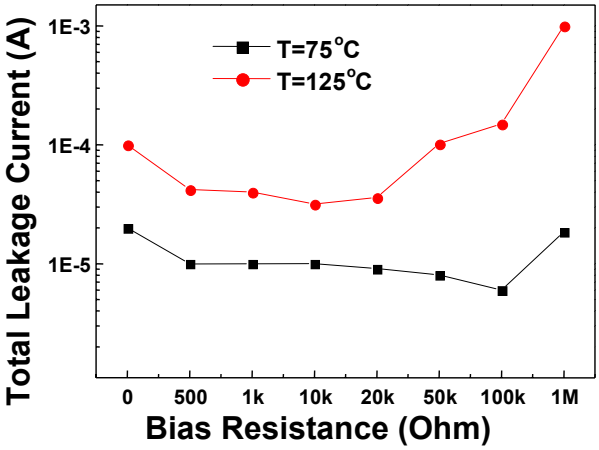

Fig. 10 The relationship between bias resistance (R) and total leakage current of LLCDS with diode number of n=4 and the bias condition of VDD=1.8V, which are measured at the temperatures of 75 °C and 125 °C, respectively.

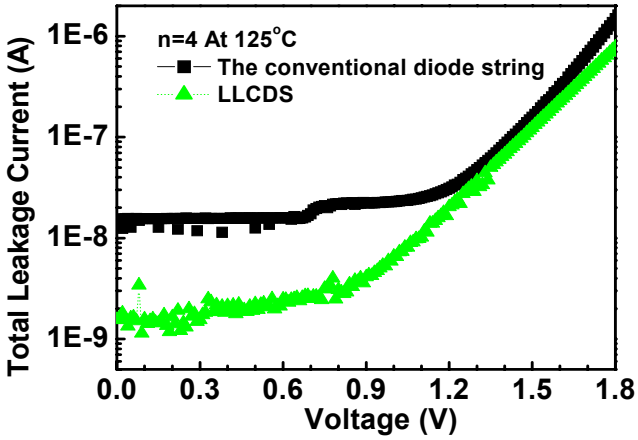

Fig. 11 Comparison on total leakage currents of the conventional diode string and the LLCDS under 125°C, n=4, and R=10 kΩ.

The LLCDS indeed has a lowest leakage current if the value of R was chosen properly. This has been predicted by the design equation (20). The relationships between the VDD voltage and the total leakage current of conventional diode string and the LLCDS under 125 °C for n = 4 are compared in Fig. 11.

With a bias resistance of 10 kΩ, the ESD robustness of the LLCDS with different numbers of diodes in series is investigated by using the transmission-line-pulse (TLP) generator with a pulse width of 100ns. The dependence of secondary breakdown current (It2) of the conventional diode string and the LLCDS on the diode number (n) in series is shown in Fig. 12, where every diode has the same device dimension of W/L= 40μm/12μm in the layout pattern. However, the It2 of the conventional diode string and the LLCDS using different diode numbers (n) in series did not have an obvious variation. With an It2 of greater than 4A, the diode sting (with n=4) can sustain the human-body-model ESD stress of 6 kV. In Fig. 12, the It2 of LLCDS does not decrease as the diode number increases. From this result, the number of stacked diodes in the diode string can be reasonably increased to get a higher total blocking voltage without degradation in its ESD level.

A comparison of the total leakage currentof the SiGe HBT triggered by the conventional diode string to the leakage current of the LLCDS under different Ro resistances is shown in Fig. 13, where the bias resistance R is 10 kΩ, a diode number of n = 4, a bias condition of VDD = 1.8V, and a temperature of 125 °C. The LLCDS-triggered SiGe HBT has a very low leakage current, as compared to that triggered by the conventional diode string with the same diode number.

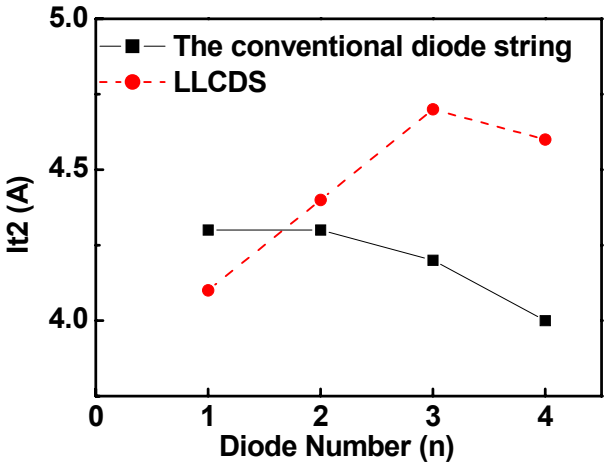

Fig. 12 The dependence of secondary breakdown current (It2) of the conventional diode string and LLCDS on the diode number (n) in series.

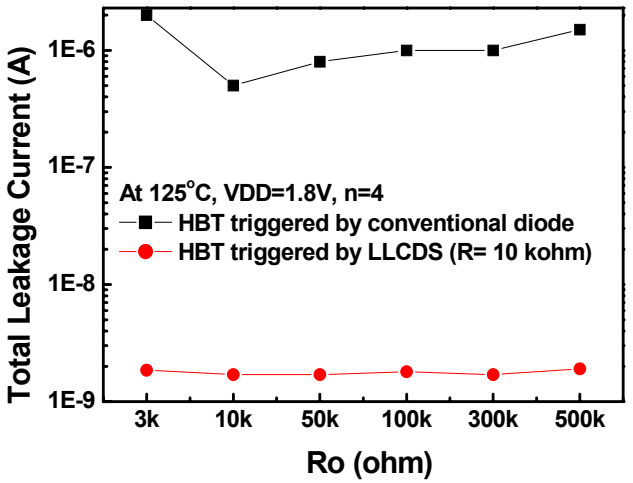

Fig. 13 Comparison on the total leakage currents of the SiGe HBT triggered by the conventional diode string or the LLCDS under different Ro resistances. The bias resistance R is 10 kΩ with the diode number of n=4, bias condition of VDD=1.8V, and the temperatures of 125 °C.

The TLP-measured I-V curves of the SiGe HBT triggered by the conventional diode string or the LLCDS under the measurement conditions of n=4 and R = Ro = 10 kΩ are shown in Fig. 14, where the current is normalized to the emitter area of the SiGe HBT. To sustain a higher ESD level, the SiGe HBT with a larger device dimension should be used in power-rail ESD clamp circuits.

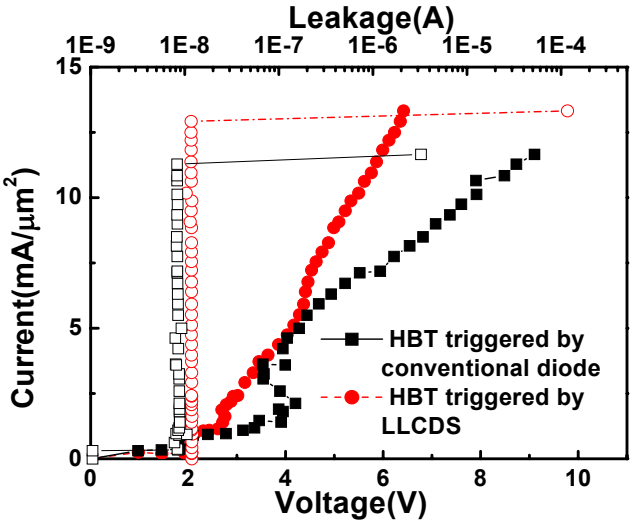

Fig. 14 The TLP-measured I-V curves of the SiGe HBT triggered by the conventional diode string or the LLCDS under the measurement conditions of n=4 and R=Ro=10 kΩ.

VI. Conclusion

A new design to minimize the leakage current of power-rail ESD clamp circuit with diode string for RF

circuits has been proposed and verified in a 0.18-μm SiGe BiCMOS process. With an additional extra bias circuit to supply a small current into the n-well of diodes in the LLCDS, the overall leakage current of LLCDS can be minimized. The design equations to minimize the leakage current in the LLCDS have been also derived. By selecting a suitable bias resistance, the total leakage current of LLCDS can be kept much smaller than that of the conventional diode string. The new proposed LLCDS and the LLCDS-triggered SiGe HBT are very suitable for power-rail ESD clamp circuits in cooperation with the small input ESD diodes to achieve good RF ESD protection design in the BiCMOS SiGe technology.

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