On-Chip ESD Protection Strategies for RF Circuits in CMOS Technology

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Abstract

Electrostatic discharge (ESD) protection design for RF circuits has been one of the key challenges to implement RF ICs in CMOS technology. On-chip ESD protection circuit at the RF I/O pads often cause unacceptable degradation to RF circuits. In this paper, ESD protection design considerations for RF circuits are addressed, and on-chip ESD protection strategies for both narrow band and broadband CMOS RF circuits are also presented and discussed.

1. Introduction

With the advantages of high integration capability and low cost for mass production, radio-frequency integrated circuits (RF ICs) operating in giga-Hz (GHz) frequency bands have been fabricated in CMOS technology. Electrostatic discharge (ESD), which has been a very important issue in IC fabrication, should be taken into consideration during the design phase of all commercial ICs [1], [2]. Therefore, on-chip ESD protection circuits are needed for all I/O pads in integrated circuits. However, applying ESD protection circuits at I/O pads inevitably introduce impacts to circuit performance. As the operation frequency of RF circuits increases, degradation on RF performance due to ESD protection circuits becomes more significant. Therefore, the RF front-end circuit and the ESD protection circuit need to be co-designed to simultaneously optimize the RF performance and ESD robustness.

This paper addresses the ESD protection strategies for RF circuits in CMOS technology. The impacts of ESD protection circuits on RF circuits are presented in section 2. The ESD protection strategies for narrow band RF circuits are shown in section 3. The ESD protection strategies for broadband RF circuits are presented in section 4. Finally, conclusion is provided in section 5.

2. Impacts of ESD Protection Circuits on RF Circuits

In order to provide enough immunity against ESD stresses, ESD protection circuits are placed at all I/O pads in integrated circuits. However, the ESD protection circuits introduce undesired parasitic capacitances and resistances to degrade RF performance. It had been reported that a typical specification on the maximum loading capacitance of the ESD protection device for a 2-GHz RF low-noise amplifier (LNA) is about 200 fF [3]. The impacts and characteristics of the ESD protection devices to RF circuit performance had been investigated [4], [5]. The previous works had demonstrated that RF performances would be significantly degraded by the ESD protection devices, especially for the ESD protection devices with large dimensions. This impact will become more serious as the operation frequency of RF circuits increases. Generally, ESD protection circuits would cause RF performance degradation on three aspects, which are noise figure, power gain, and input matching.

Noise figure is one of the most important merits for RF receivers. Since the RF receiver is a cascade of several stages, the overall noise figure can be obtained in terms of the noise figure and power gain of each stage in the receiver. For example, if there are m stages in the receiver, the total noise figure of the receiver can be expressed as [6]

$$NF_{total} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p1}} + \cdots + \frac{NF_m - 1}{A_{p1} \cdots A_{p(m-1)}} \quad (1)$$

where NF_i is the noise figure of the i-th stage, and Ap_i is the power gain of the i-th stage. According to equation (1), the noise figure contributed by the first stage is a dominant factor to the total noise figure (NF_{total}). With the ESD protection circuit added at the input node of the receiver IC, the ESD protection circuit becomes the first stage in the receiver. Taking only the first two stages, which are the ESD protection circuit and LNA, into consideration, as shown in Fig. 1. The overall noise figure of the LNA with ESD protection circuit is

$$\begin{aligned} NF_{LNA\_ESD} &= NF_{ESD} + \frac{NF_{LNA} - 1}{L^{-1}} \\ &= L + (NF_{LNA} - 1)L = L \cdot NF_{LNA} \end{aligned} \quad (2)$$

where L is the power loss of the ESD protection circuit, and NF_{LNA} and NF_{ESD} are the noise figures of the LNA and ESD protection circuit, respectively. Since the ESD

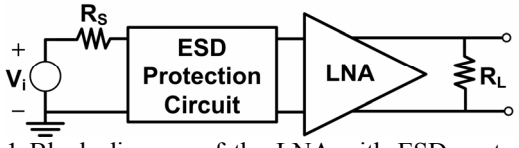

Fig. 1 Block diagram of the LNA with ESD protection circuit.

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protection circuit is a passive reciprocal network, NF_{ESD} is equal to L [6]. This implies if the ESD protection circuit has 1 dB power loss, the noise figure of the LNA with ESD protection will directly increase 1 dB as well. Thus, the power loss of the ESD protection circuit should be carefully considered because it has a significant effect on the total noise figure. Moreover, signal loss due to the ESD protection circuit would also cause power gain degradation.

Another impact caused by the ESD protection circuit is the input matching, which is particularly critical for narrow band RF circuits. With the ESD protection circuit added at the input node, the input matching condition is changed because of the parasitic capacitance from the ESD protection circuit. As a result, the center frequency of the RF circuit is shifted due to input mismatching. In order to provide ESD protection and minimize performance degradation caused by the ESD protection circuits, several works had been reported and will be discussed in sections 3 and 4, respectively.

3. Narrow Band ESD Protection Strategies

ESD protection strategies for narrow band RF circuits can be categorized into four types, which are low-C, impedance cancellation, impedance isolation, and impedance matching.

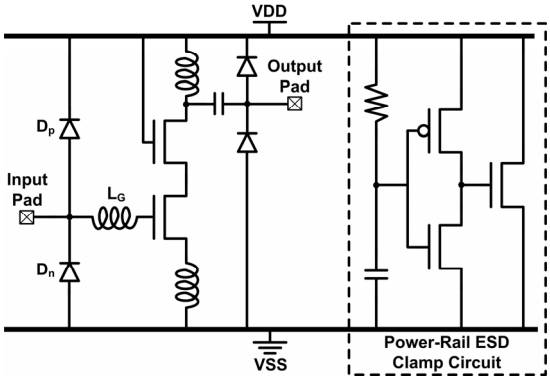

Fig. 2 The LNA with low-C ESD protection strategy.

3.1 Low-C

The LNA with low-C ESD protection strategy is shown in Fig. 2 [7]-[9]. When the ESD protection diodes D_p and D_n are under forward-biased, they can provide discharge paths from input pad to VDD and from VSS to input pad, respectively. With the power-rail ESD clamp circuit providing a discharge path from VDD to VSS, the ESD protection diodes can be operated in the forward-biased mode to achieve high ESD robustness under all ESD test modes [10].

In order to reduce the performance degradation caused by the parasitic capacitances from the ESD protection diodes, the dimensions of ESD protection diodes are decreased to reduce the parasitic capacitance, but the ESD robustness can be kept by using the active power-rail ESD clamp circuit. To further reduce the capacitance from the ESD diodes, the diodes in stacked configuration had been reported for RF ESD protection [11].

3.2 Impedance Cancellation

Besides diodes, the ESD protection strategy using inductor as the ESD protection device had been reported [12]-[15], as shown in Fig. 3. The inductance of the ESD protection inductor (L_{ESD}) was selected to resonate with the parasitic capacitances at the RF operation frequency. With the parallel LC network resonating at the RF operation frequency, the shunt impedance of the ESD protection circuit is very large [12]-[14]. Therefore, the ESD protection strategy using impedance-cancellation technique can reduce the negative impacts on RF performance for narrow band RF circuits.

Based on the same concept, two alternative designs had been reported [15]. In the first design, the ESD protection inductor is connected between VDD and input pad, while a diode is added between VSS and input pad. In the second design, the ESD protection inductor is connected between VSS and input pad, while a diode is added between input pad and VDD. The inductor and the parasitic capacitance of the diode are also designed to resonate at the RF operation frequency.

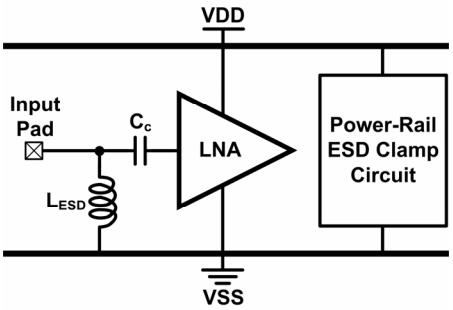

Fig. 3 The impedance-cancellation ESD protection strategy.

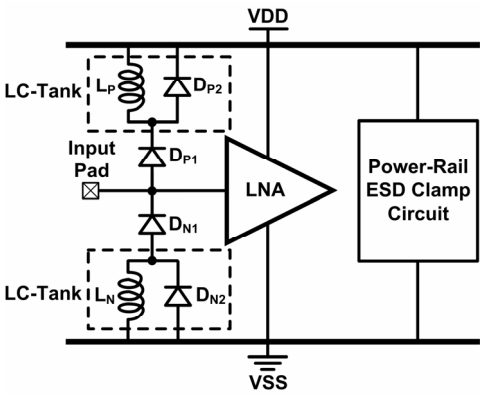

Fig. 4 The impedance-isolation ESD protection strategy.

3.3 Impedance Isolation

Another ESD protection strategy for narrow band RF circuits is the impedance isolation technique. As shown in Fig. 4, two LC-tanks are used between input and VDD, and between input pad and VSS, respectively [16]. The resonant frequencies of the LC-tanks are designed at the RF operation frequency to minimize the impacts of the ESD protection circuit on RF performance.

3.4 Impedance Matching

An input matching co-design of LNA with ESD protection had been reported [17]. This ESD protection strategy manipulates the parasitic capacitance of the ESD protection device as a component in the LNA input matching network. While the impedance cancellation and impedance isolation strategies compensate or tune out the effects of the parasitic capacitance of the ESD protection device (C_{ESD}), the impedance matching ESD protection strategy places the ESD protection device between the gate inductor (L_G) and the input NMOS, as shown in Fig. 5. The performance degradation induced by the ESD protection circuit can be reduced, because the parasitic capacitance of the ESD protection circuit is matched in the matching network.

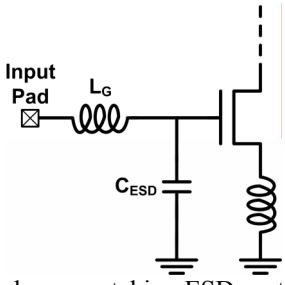

Fig. 5 The impedance-matching ESD protection strategy.

4. Broadband ESD Protection Strategies

For broadband RF circuits, the RF performance should be taken into account for a specific frequency band. Thus, the main challenge for broadband RF ESD protection design is the broadband RF characteristic of the ESD protection circuit, which should be optimized in the frequency band of interest. Broadband ESD protection strategies can be categorized into three types, which are low-C, distributed ESD protection, and T-coil matching.

4.1 Low-C

As discussed in section 3.1, the dimensions of the ESD protection diodes at input node can be reduced to mitigate the impacts on RF performance. Since the parasitic capacitances of the ESD protection diodes are small, low-C ESD protection strategy can be also used in broadband ESD protection for ultra-wideband LNA [18], [19].

Silicon-controlled rectifier (SCR) had been demonstrated to have both high ESD robustness and low parasitic capacitance under a small layout area [20]-[22]. With suitable trigger circuit to enhance its turn-on speed, or to reduce its switching voltage, SCR could be a promising component for broadband RF ESD protection.

4.2 Distributed ESD Protection Scheme

To achieve impedance matching for broadband RF circuits, the equal-size distributed ESD (ES-DESD) protection scheme had been reported, as shown in Fig. 6 [23]. The ESD protection diodes were divided into several sections with the same dimensions and matched by transmission lines (T-lines) or inductors. Such a distributed ESD protection can achieve both good broadband RF matching and high ESD robustness. To further improve the ESD robustness, a modified design of decreasing-size ESD (DS-DESD) protection scheme had been proposed [24]. The DS-DESD protection scheme allocates the ESD protection diodes with decreasing sizes from the input pad to the core circuit. With the same total parasitic capacitance of the ESD protection diodes, the DS-DESD protection scheme had been reported to have higher ESD robustness than that of the ES-DESD scheme because the first pair of ESD protection diodes (D_{P1} and D_{N1}) are larger than those of the ES-DESD protection scheme. Moreover, good broadband RF matching is still maintained in the DS-DESD protection scheme.

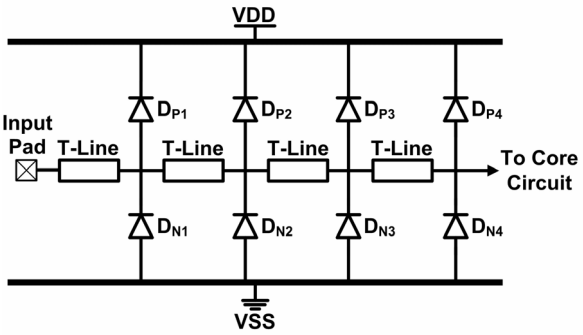

Fig. 6 The equal-size distributed ESD (ES-DESD) protection scheme.

Another distributed ESD protection design is the π-model distributed ESD (π-DESD) protection scheme, as shown in Fig. 7 [25]. Composed of one pair of ESD protection diodes close to the input pad, the other pair close to the core circuit, and a transmission line matching these parasitic capacitances, the π-DESD protection scheme can also achieve both good broadband RF matching and high ESD robustness. The first pair of ESD protection diodes (D_{P1} and D_{N1}) in the π-DESD protection scheme is directly connected to the input pad, but the first pair of ESD protection diodes in the ES-DESD protection scheme is connected to the input

pad through a transmission line. Therefore, the π-DESD protection scheme can sustain higher ESD robustness than that of the ES-DESD protection scheme.

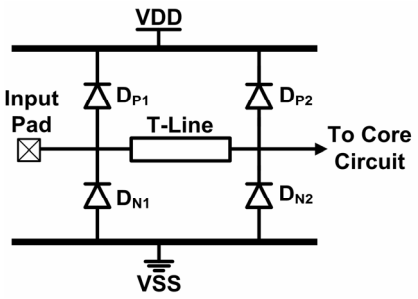

Fig. 7 The π-model distributed ESD protection scheme.

4.3 T-Coil Matching

The broadband ESD protection design with T-coil matching had been reported, as shown in Fig. 8 [26]. With proper matching design, this circuit can provide a purely resistive input impedance, which is independent of frequency and parasitic capacitance of the ESD protection circuit. Thus, this design can achieve good impedance matching in a broad bandwidth of RF circuits.

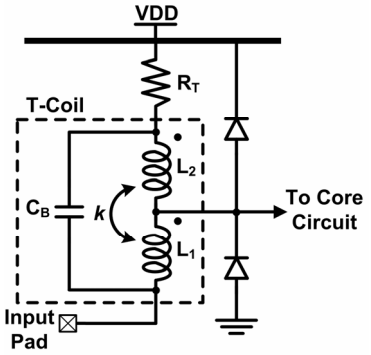

Fig. 8 The ESD protection strategy with T-coil matching.

5. Conclusion

A comprehensive overview on the ESD protection strategies for RF circuits in CMOS technology has been presented. The requirements on ESD protection devices for RF circuits include low parasitic capacitance, low loss, and high ESD robustness. To optimize both RF performance and ESD robustness simultaneously, the undesired parasitic effects from ESD protection devices need to be minimized or cancelled. Therefore, ESD protection circuits and RF circuits should be co-designed to achieve both good RF performance and high ESD robustness. On-chip efficient ESD protection circuits for RF applications will continually be an important design task to implement RF circuits in CMOS technology.

References

[1] S. Voldman, ESD: Circuits and Devices, John Wiley & Sons (2006).

[2] S. Voldman, ESD: RF Technology and Circuits, John Wiley & Sons (2006).

[3] C. Richier, P. Salome, G. Mabboux, I. Zaza, A. Juge, and P. Mortini, EOS/ESD Symp., p. 251 (2000).

[4] M.-D. Ker and C.-M. Lee, IEEE International Symp. Circuits and Systems, p. 297 (2003).

[5] K. Gong, H. Feng, R. Zhan, and A. Wang, IEEE Trans. Microwave Theory and Techniques, vol. 50, no. 1, p. 393 (2002).

[6] B. Razavi, RF Microelectronics, p. 45 (1998).

[7] V. Chandrasekhar, C. Hung, Y. Ho, and K. Mayaram, IEEE European Solid-State Circuits Conf., p. 347 (2002).

[8] M.-D. Ker, W.-Y. Lo, C.-M. Lee, C.-P. Chen, and H.-S. Kao, IEEE Radio Frequency Integrated Circuits Symp., p.427 (2002).

[9] P. Leroux, J. Janssens, and M. Steyaert, IEEE International Solid-State Circuits Conf., p. 410 (2001).

[10] M.-D. Ker, IEEE Trans. Electron Devices, vol. 46, no.1, p. 173 (1999).

[11] M.-D. Ker and C.-Y. Chang, Microelectronics Reliability, vol. 42, p. 863 (2002).

[12] D. Linten, S. Thijs, W. Jeamsaksiri, J. Ramos, A. Mercha, M. I. Natarajan, P. Wambacq, A. J. Scholten, and S. Decoutere, IEEE Symp. VLSI Circuits, p.86 (2005).

[13] P. Leroux and M. Steyaert, IEEE European Solid-State Circuits Conf., p. 295 (2004).

[14] S. Hyvonen, S. Joshi, and E. Rosenbaum, EOS/ESD Symp., p. 188 (2003).

[15] S. Hyvonen and E. Rosenbaum, EOS/ESD Symp., p. 9 (2005).

[16] M.-D. Ker, C.-I. Chou, and C.-M. Lee, IEEE Radio Frequency Integrated Symp., p. 115 (2003).

[17] B.-S. Huang and M.-D. Ker, IEEE International Symp. Circuits and Systems, p. 4891 (2006).

[18] M. Liu, J. Craninckx, N. M. Iyer, M. Kuijk, and A. R. F. Barel, IEEE J. Solid-State Circuits, vol. 54, no. 4, p. 1698 (2006).

[19] R. Salerno, M. Tiebout, H. Paule, M. Streibl, C. Sandner, and K. Kropf, IEEE European Solid-State Circuits Conf., p. 219 (2005).

[20] J.-H. Lee, Y.-H. Wu, K.-R. Peng, R.-Y. Chang, T.-L. Yu, and T.-C. Ong, IEEE Custom Integrated Circuits Conf., p. 93 (2002).

[21] K. Higashi, A. O. Adan, M. Fukumi, N. Tanba, T. Yoshimasu, and M. Hayashi, IEEE Radio Frequency Integrated Symp., p. 285 (2002).

[22] H. Xie, H. Feng, R. Zhan, A. Wang, D. Rodriguez, and D. Rice, IEEE Electron Device Lett., vol. 26, no. 2, p. 121 (2005).

[23] C. Ito, K. Banerjee, and R. W. Dutton, IEEE Trans. Electron Devices, vol. 49, no. 8, p. 1444 (2002).

[24] M.-D. Ker, Y.-W. Hsiao, and B.-J. Kuo, IEEE Trans. Microwave Theory and Techniques, vol. 53, no. 9, p. 2672 (2005).

[25] M.-D. Ker, B.-J. Kuo, and Y.-W. Hsiao, J. Electrostatics, vol. 64, no.2, p. 80 (2006).

[26] S. Galal and B. Razavi, IEEE J. Solid-State Circuits, vol. 38, no. 12, p. 2334 (2003).