

Vertical SCR Structure for On-Chip ESD Protection in Nanoscale CMOS Technology

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Abstract - A vertical silicon-controlled rectifier (SCR) structure utilizing ESD implantation layer was proposed and implemented in nanoscale CMOS technology. Compared with the traditional SCR structure, the proposed structure has lower trigger voltage and high enough ESD protection capability. Therefore, the proposed structure was suitable for ESD protection in nanoscale CMOS process.

I. INTRODUCTION

As CMOS technologies keep scaling down, thin oxide thickness of MOS transistors has made the integrated circuits to be sensitive to the electrostatic discharge (ESD) [1]. In order to protect the IC products against the ESD damages, on-chip ESD protection devices must be equipped for the pads that may be stressed by ESD [2]. The typical on-chip ESD protection design is shown in Fig. 1, which consists of the ESD protection devices between input/output (I/O) pad and V_{DD}/V_{SS} , and the power-rail ESD clamp circuit between V_{DD} and V_{SS} .

Fig. 2 shows the ESD design window of an IC [3], which is defined by the power-supply voltage (V_{DD}) of the IC, the failure level of ESD protection device, and the gate-oxide breakdown voltage (V_{BD}) of MOSFET. First, the trigger voltage (V_{t1}) and holding voltage (V_h) of ESD protection device must be lower than the gate-oxide breakdown voltage of MOSFET to prevent the internal circuits from damage before the ESD protection device is turned on during ESD stresses. Second, the trigger voltage and holding voltage of the ESD protection device must be higher than the power-supply voltage of the IC to prevent the ESD protection devices from being mis-triggered under normal circuit operating conditions. Moreover, the turn-on resistance (R_{on}) of ESD protection device should be minimized to reduce the joule heat generated in the ESD protection device and the clamping voltage of the ESD protection device during ESD stresses. As CMOS technology is continuously scaling down, the gate oxide becomes thinner, which leads to the reduced gate-oxide breakdown voltage of MOSFET. Typically, the gate-oxide breakdown voltage is decreased to only ~ 5 V in a nanoscale CMOS process with gate-oxide thickness of ~ 20 Å. As a result, the ESD design window becomes much narrower in

nanoscale CMOS technologies. Furthermore, ESD protection circuits need to be quickly turned on during ESD stresses in order to provide efficient discharging paths in time.

The scaling-down feature sizes in nanoscale CMOS technologies are expected to improve the area efficiency. However, ESD robustness of IC product needs to be maintained, so the device dimensions of ESD protection devices can not be shrunk. Therefore, the ESD protection devices with higher ESD robustness and smaller layout area are needed in nanoscale CMOS technologies.

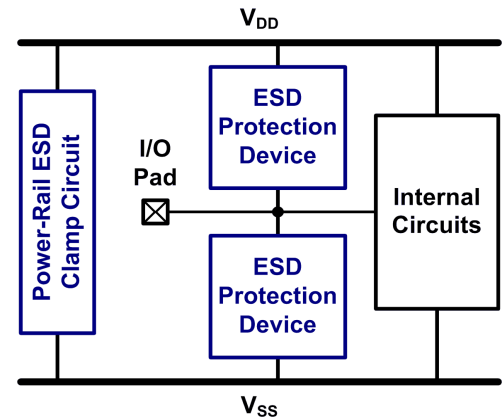


Fig. 1. Whole-chip ESD protection against ESD damages.

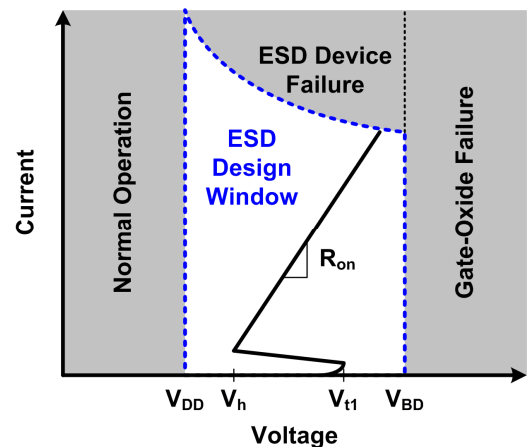


Fig. 2. ESD design window defined by the power-supply voltage (V_{DD}) of the IC, the failure level of ESD protection device, and the gate-oxide breakdown voltage (V_{BD}) of the MOSFET.

The silicon-controlled rectifier (SCR) device has been reported to be useful for ESD protection due to its high ESD robustness, small device size, and excellent clamping capabilities (low holding voltage and small turn-on resistance) [4], [5]. Besides, the SCR device can be safely used without latchup danger in advanced CMOS technologies with the low supply voltage [6]. Fig. 3 shows the traditional SCR structure. The anode is connected to the first P+ and the pickup N+, which are formed in the N-well. The cathode is connected to the second N+ and the pickup P+, which are formed in the nearby P-well. The SCR path consists of P+, N-well, P-well, and N+. The equivalent circuit of the SCR consists of a PNP BJT and a NPN BJT. The PNP is formed by the P+, N-well, and P-well, and the NPN is formed by the N-well, P-well, and N+. As ESD zapping from anode to cathode, the positive-feedback regenerative mechanism of PNP and NPN results in the SCR device highly conductive to make SCR very robust against ESD stresses. However, SCR has some drawbacks, such as higher trigger voltage and slower turn-on speed.

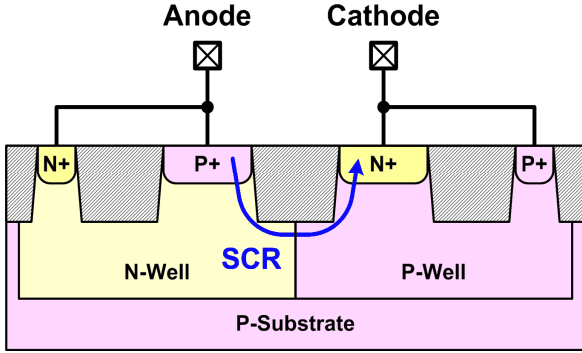


Fig. 3. Cross-sectional view of traditional SCR.

In this work, a novel vertical SCR structure is proposed and investigated in a nanoscale CMOS technology.

II. PROPOSED VERTICAL SCR STRUCTURE

Two vertical SCR are proposed in this work, as shown in Figs. 4(a) and 4(b). The difference between Figs. 4(a) and 4(b) is the metal connection at cathode side. In this design, the P-ESD denotes the p-type ESD implantation. This implantation was typically used to improve the turn-on ability of ESD protection NMOS [7]. At cathode side, the N+ is separated from the P+, and the silicide blocking is used on the surface of this N+ and P+. Beside, the P-ESD layer at cathode side is used to isolate the N-well and N+ region. The vertical SCR consists of P+, N-well, P-ESD, and N+. In Fig. 4(a), the P-ESD/P+ is connected to the cathode (proposed SCR 1). In Fig. 4(b), the P-ESD/P+ is floating (proposed SCR 2). As ESD zapping from the anode to

the cathode, the positive-feedback regenerative mechanism of PNP (P+, N-well, and P-ESD) and NPN (N-well, P-ESD, and N+) results in the vertical SCR structure highly conductive to discharge the ESD current.

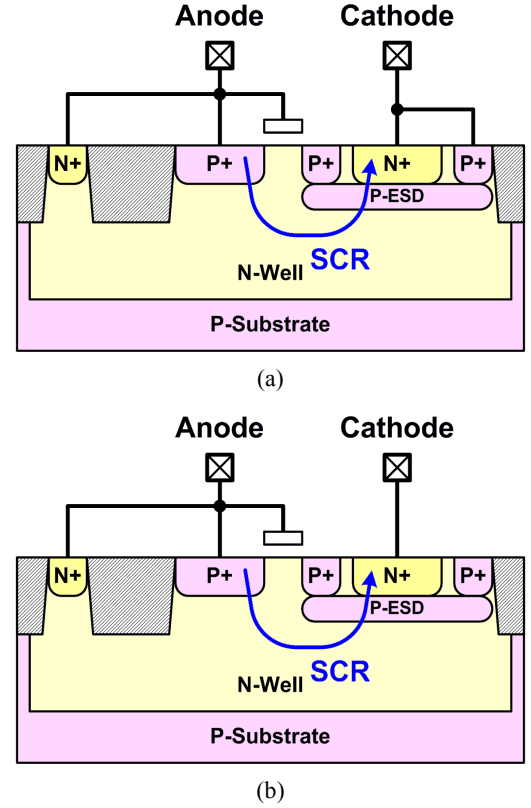


Fig. 4. Cross-sectional view of proposed vertical SCR with (a) P-ESD/P+ connected to cathode (proposed SCR 1) and (b) floating P-ESD/P+ (proposed SCR 2).

III. VERIFICATION IN SILICON

All the traditional SCR, proposed SCR 1, and proposed SCR 2 are implemented in a 0.18 μm CMOS process. Each test device is drawn in multi-finger style with total width of 120 μm . All these dimensions of the test devices are listed in Table I. Fig. 5 shows the chip photograph of the test devices.

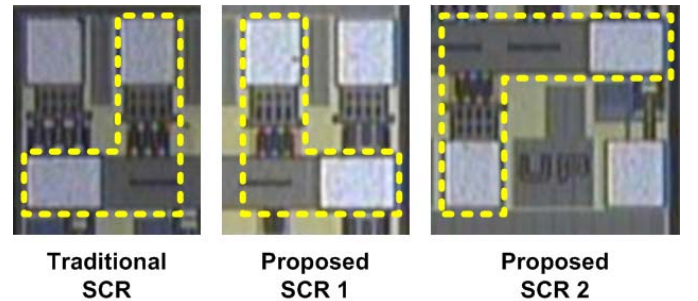


Fig. 5. Chip photograph of test devices.

A. ESD Robustness

The human-body-model (HBM) ESD robustness of the test devices are evaluated by the ESD tester. The failure criterion is defined as the I-V curve seen between test pads shifting over 30% from its original curve after ESD stressed at every ESD test level. All test devices can pass 8kV HBM ESD tests (8kV is the measurement limitation of the given ESD tester).

B. TLP I-V Characteristics

A transmission-line-pulsing (TLP) system with a 10ns rise time and a 100ns pulse width is used to evaluate the trigger voltage (V_{t1}), holding voltage (V_h), turn-on resistance (R_{on}), and secondary breakdown current (I_{t2}) of the test devices in the time domain of HBM ESD event. The TLP-measured I-V curves of the test devices are shown in Fig. 6. The proposed SCR 1 and proposed SCR 2 have the better V_{t1} of 5.5V and 5.2V, while the traditional SCR has much higher V_{t1} . The traditional SCR, proposed SCR 1, and proposed SCR 2 can achieve the TLP-measured I_{t2} of 9.4A, 8.2A, and 8.3A, respectively. All I_{t2} of the test devices are high enough for ESD protection.

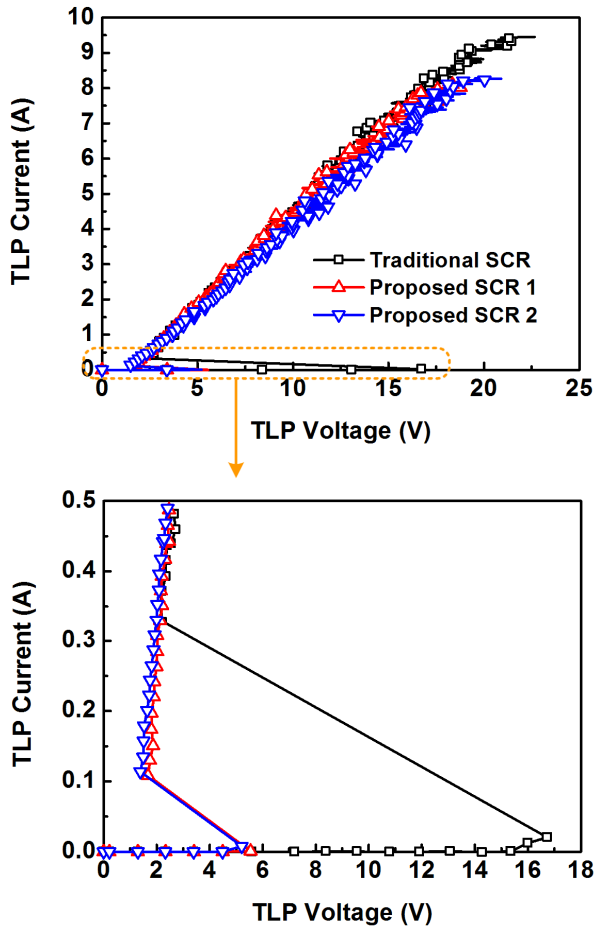


Fig. 6. Measured TLP I-V curves.

C. DC I-V Characteristics

The dc I-V curves of the test devices are shown in Fig. 7. The holding voltages (V_h) of the ESD protection devices under dc measurement are lower than those under TLP measurement due to the self-heating effect [8]. All these measured data are summarized in Table I.

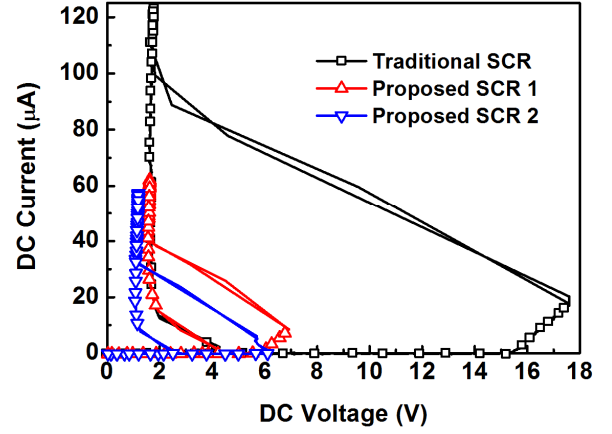


Fig. 7. Measured dc I-V curves.

Table I
Summary on Measurement Results

	Traditional SCR	Proposed SCR 1	Proposed SCR 2
Width (μm)	120	120	120
HBM (kV)	>8	>8	>8
TLP V_{t1} (V)	16.7	5.5	5.2
TLP V_h (V)	2.1	1.7	1.4
TLP R_{on} (V)	2	2	2
TLP I_{t2} (V)	9.4	8.2	8.3
DC V_h (V)	1.6	1.5	1.1

IV. CONCLUSION

The proposed vertical SCR structure has been designed, fabricated, and characterized in nanoscale CMOS technology. Without any trigger circuit, the proposed SCR 1 and proposed SCR 2 have the V_{t1} of 5.5V and 5.2V, which is much better than the traditional SCR. The proposed vertical SCR structure also has high HBM ESD robustness; therefore, it can be a solution for ESD protection in nanoscale CMOS technology.

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