ESD Protection Design for CMOS Integrated Circuits with Mixed-Voltage I/O Interfaces

Wei-Jen Chang
Institute of Electronics
National Chiao-Tung University
Hsinchu, Taiwan
eda.ee87@nctu.edu.tw

Ming-Dou Ker
Institute of Electronics
National Chiao-Tung University
Hsinchu, Taiwan
mdker@ieee.org

Abstract— **With consideration on the gate-oxide reliability, the new ESD protection design with ESD bus for 1.2/2.5-V mixed-voltage I/O interfaces is reported by using the new proposed high-voltage-tolerant power-rail electrostatic discharge (ESD) clamp circuit. This proposed power-rail ESD clamp circuit with only 1.2-V low-voltage NMOS/ PMOS devices can be operated under the 2.5-V input conditions without suffering the gate-oxide reliability issue. The experimental results in a 0.13-μm CMOS process have confirmed that the proposed power-rail ESD clamp circuit has high human-body-model (HBM) and machine-model (MM) ESD robustness and fast turn-on speed. The proposed power-rail ESD clamp circuit is an excellent ESD protection solution to the mixed-voltage I/O interfaces.**

I. INTRODUCTION

In CMOS integrated circuits (ICs), the device dimensions of MOSFET have been scaled down to improve circuit performance and to increase circuit operating speed. In addition, the power supply voltage has been also scaled down to reduce the power consumption. However, some IC components on the system board are still operated with higher power supply voltage. Therefore, most micro-electronic systems or subsystems with different internal power supply voltages often require the ICs to be designed with mixed-voltage I/O interfaces [1]-[3]. For example, a chip which operates with internal power supply voltage of 1.2 V may have the I/O signals of 2.5 V.

To solve the gate-oxide reliability issue without using additional thick gate oxide process (also known as dual gate oxides in some CMOS processes) [2], the stacked NMOS configuration has been widely used in the mixed-voltage I/O interfaces [1]-[3]. But, the stacked NMOS often have much lower electrostatic discharge (ESD) level and slower turn-on speed, as compared with the single NMOS [4]. The disadvantages result from the longer base width of the lateral n-p-n BJT in the stacked NMOS devices. Therefore, additional ESD protection design was used to improve the turn-on speed and ESD robustness of the stacked NMOS in the mixed-voltage I/O interfaces [5].

In this paper, a new high-voltage-tolerant power-rail ESD clamp circuit, which combines the stacked NMOS of low-voltage devices with the substrate-triggered technique, is designed to protect the mixed-voltage I/O interfaces against ESD stresses. The new proposed power-rail ESD clamp circuit realized with the low-voltage devices for 1.2/2.5-V mixed-voltage I/O interfaces is designed without suffering the gate-oxide reliability issue. This high-voltage-tolerant power-rail ESD clamp circuit has been successfully verified in a 0.13-μm 1.2-V CMOS process.

II. NEW ESD PROTECTION SCHEME FOR MIXED-VOLTAGE I/O INTERFACES

To improve ESD robustness of the mixed-voltage I/O interfaces, an ESD design concept by using the dummy ESD bus in the chip was proposed [6]. However, in this prior art, the gate-oxide reliability was not considered in its circuit design. With consideration on the gate-oxide reliability, the new modified ESD protection design with ESD bus for 1.2/2.5-V mixed-voltage I/O interfaces is proposed in Fig. 1. The stacked NMOS and pull-up PMOS (with the gate-tracking circuit and n-well self-biased circuit) are the typical implementation of mixed-voltage output buffer with only thin gate-oxide devices [1].

To receive the input signals with 2.5-V voltage level, the direct diode connection from the pad to VDD of 1.2V is forbidden. Therefore, the ESD protection design in Fig.1 is realized with the diodes Dp, Dn, D1, the ESD bus, the high-voltage-tolerant power-rail ESD clamp circuit, and the low-voltage power-rail ESD clamp circuit.

Under positive-to-VSS (PS-mode) ESD stress on I/O pad, the ESD current is discharged through the diode Dp and the high-voltage-tolerant power-rail ESD clamp circuit (HV) to the grounded VSS. Under positive-to-VDD (PD-mode) ESD

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stress on I/O pad, the ESD current is discharged through Dp, the high-voltage-tolerant power-rail ESD clamp circuit (HV), and then the low-voltage power-rail ESD clamp circuit (LV) to the grounded VDD. Under negative-to-VSS (NS-mode) ESD stress, the ESD current is discharged through the diode Dn in forward-biased condition to the grounded VSS. Under negative-to-VDD (ND-mode) ESD stress, the ESD current is discharged through the diode Dn to the floating VSS, and then through the low-voltage power-rail ESD clamp circuit (LV) to the grounded VDD. The four modes of ESD stresses on the mixed-voltage I/O pad to VDD or VSS have the corresponding well-designed ESD discharging paths in the proposed ESD protection scheme. Moreover, such ESD_BUS and the high-voltage-tolerant power-rail ESD clamp circuit can be shared with other mixed-voltage I/O pads to achieve whole-chip pin-to-pin ESD protection.

D1 is used to keep the initial voltage level of ESD bus at VDD of 1.2V, when the I/O buffer is under normal circuit operating conditions. When the input signals of 2.5V reach to the I/O pad, the ESD bus line will be charged up to 2.5V through Dp. So, in this successful ESD protection design, the high-voltage-tolerant power-rail clamp circuit in the mixed-voltage I/O interfaces must sustain the high-voltage (2.5-V) stress during normal circuit operating conditions. The low-voltage power-rail ESD clamp circuit (LV) can be realized by the traditional RC-based ESD detection circuit with 1.2-V devices [7]. How to design a turn-on efficient power-rail ESD clamp circuit for 2.5-V applications with only 1.2-V devices is the key design issue in such ESD protection scheme for mixed-voltage I/O interfaces.

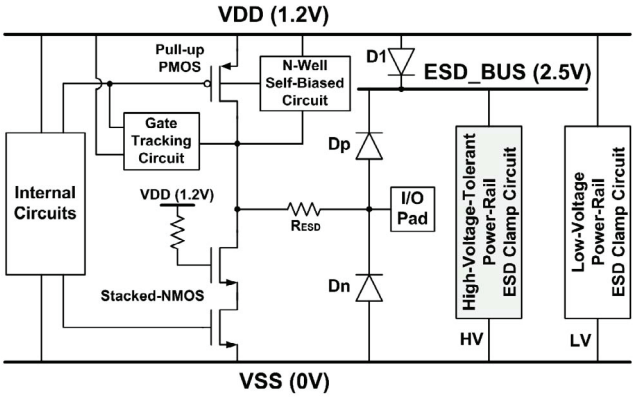

Figure 1. ESD protection scheme for mixed-voltage I/O interfaces with the high-voltage-tolerant power-rail ESD clamp circuit.

III. HIGH-VOLTAGE-TOLERANT POWER-RAIL ESD CLAMP CIRCUIT

The high-voltage-tolerant power-rail ESD clamp circuit [8] realized with only 1.2-V devices for 2.5-V mixed-voltage I/O applications is proposed in Fig. 2, which contains an ESD clamp device and an ESD detection circuit. The ESD clamp device is realized by the stacked NMOS (STNMOS) with the substrate-triggered technique. The STNMOS is formed by two stacked NMOS transistors (Mn1 and Mn2) with 1.2-V gate oxide in the 0.13-μm CMOS process. The drain of Mn2 and the source of Mn1 share a common N+ diffusion region. The gate of Mn1 is biased at VDD of 1.2V through a resistor to avoid the gate-oxide reliability issue, and the gate of Mn2 is connected to VSS (ground) to ensure the off state of the STNMOS during normal circuit operating conditions. The STNMOS is free from gate-oxide reliability issue under ESD_BUS of 2.5V. Under normal circuit operating conditions, the ESD detection circuit is kept inactive and does not interfere with the functions of internal circuits. But, it becomes active to provide the substrate-triggered current to quickly trigger on the STNMOS under ESD stress conditions. The gate voltage of PMOS Mp1 is decided by the RC delay caused by an N-Well resistor R2 and a capacitor (realized by Mp3 in a stand-alone N-well). The time constant of R2 and C (Mp3) should be designed around the order of ~ 1μs to differentiate the power-on transition (the supply voltage with a rise time of several milliseconds) from the ESD transition (the ESD voltage with a rise time of several nanoseconds).

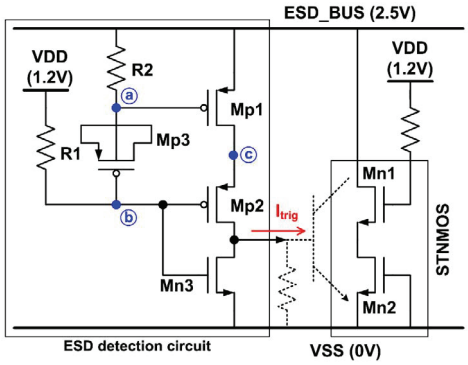

Figure 2. The new proposed high-voltage-tolerant power-rail ESD clamp circuit with 1.2-V devices for operating with ESD_BUS of 2.5V.

A. Normal Circuit Operating Conditions

In normal circuit operating conditions with 2.5-V ESD_BUS and 1.2-V VDD power supply voltages, the gate of Mp1 (node a) is biased at ESD_BUS through the resistor R2, and the gate of Mp2 and Mn3 (node b) are biased at VDD through the resistor R1. Therefore, Mp1 and Mp2 are kept in off state but Mn3 is turned on to bias the substrate of STNMOS at VSS. There is no trigger current generated from the ESD detection circuit into the base of the parasitic n-p-n BJT in the STNMOS, so the STNMOS is guaranteed to be kept off under normal circuit operating conditions. The source-gate voltage of Mp2 is less than the threshold voltage of 1.2-V PMOS transistor (|Vtp|), so the source voltage of Mp2 (node c) is kept between VDD and VDD+|Vtp|. In this situation, all 1.2-V devices are free from gate-oxide reliability issue under normal circuit operating condition with 2.5-V ESD_BUS in the mixed-voltage I/O interfaces.

Fig. 3 shows the Hspice-simulated voltages on some nodes of the ESD detection circuit during normal power-on

transition. In this simulation, the ESD_BUS and VDD are respectively powered on to 2.5V and 1.2V with a simultaneous rise time of 1ms. The gate voltage (node a) of Mp1 in the ESD detection circuit with the selected R2-C (Mp3) value can be validated to follow up the power-on transition of ESD_BUS to keep the PMOS Mp1 off. The Hspice-simulated results show that the voltages across the gate-drain, gate-source, and gate-bulk terminals of every device do not exceed the process limitation (~1.32V in a given 1.2-V CMOS process).

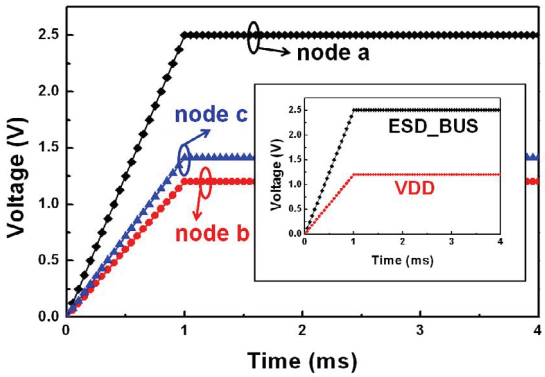

Figure 3. Hspice-simulated voltages on the nodes of ESD detection circuit in the high-voltage-tolerant power-rail ESD clamp circuit under normal power-on transition with a rise time of 1ms.

B. *ESD Transient Event*

When applying ESD transient voltage to ESD_BUS with VSS relatively grounded, the RC delay of R2 and C (Mp3) in the ESD detection circuit will keep the gate (node a) of Mp1 at a relatively low voltage level for a long time. The VDD is initially floating with an initial voltage level of 0V before the ESD voltage is applied across ESD_BUS and VSS. Some ESD transient voltage would be coupled to VDD through the parasitic capacitance during ESD zapping, but the R1 and the parasitic capacitance at the gates of Mp2 and Mn3 will hold the gate of Mp2 at a low voltage level for a long time to keep Mp2 in on state. Therefore, Mp1 and Mp2, whose initial gate voltages are at a low voltage level, can be quickly turned on by the ESD energy to generate the substrate-triggered current (I_{trig}) into the substrate of the STNMOS. After the base-emitter voltage of the lateral n-p-n BJT in the STNMOS is greater than its cut-in voltage, the STNMOS will be triggered into its snapback region to discharge ESD current from ESD_BUS to VSS.

The transient simulation of the ESD detection circuit under ESD transition is shown in Fig. 4. The Hspice-simulated results show that, when a 0-to-5.5V ESD-like voltage pulse with a rise time of 10ns is applied to ESD_BUS, the gate voltage (node a) of Mp1 is kept at a low voltage level due to the time delay of R2 and C (Mp3). The gate voltage (node b) of Mp2 is also kept at a low voltage due to floating VDD. Therefore, Mp1 and Mp2 can be turned on to conduct the substrate-triggered current (I_{trig}) in the ESD detection circuit to trigger STNMOS on. By selecting the suitable device dimensions of R2, Mp1, Mp2, and Mp3, the peak current and the period of the substrate-triggered current can be designed to meet different applications or specifications.

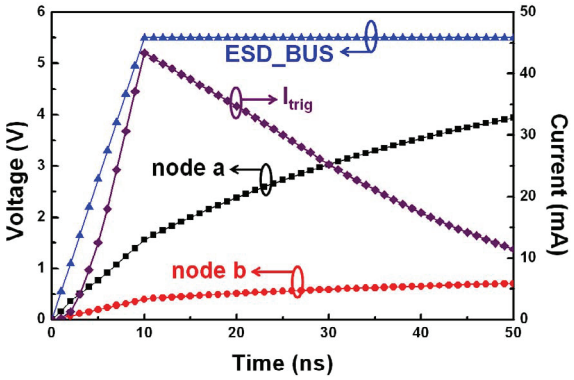

Figure 4. Hspice-simulated voltages on the nodes of ESD detection circuit and the trigger current (I_{trig}) through Mp2 in the high-voltage-tolerant power-rail ESD clamp circuit under 0-to-5.5V ESD-like transition.

IV. Experimental Results

A. *Turn-on Speed*

In order to verify the turn-on efficiency of the new proposed high-voltage-tolerant power-rail ESD clamp circuit, a 0-to-20V voltage pulse with a rise time of 10ns is applied to ESD_BUS with grounded VSS and floating VDD. The turn-on speed of the STNMOS with or without ESD detection circuit is measured and shown in Fig. 5. The overshooting peak voltage of the measured voltage waveform on STNMOS without ESD detection circuit is about 10V, which could cause damage to the gate oxide of the low-voltage devices. On the contrary, the 20-V voltage pulse can be quickly clamped by the STNMOS with ESD detection circuit to a low voltage level without suffering the high overshooting voltage, such that Mp1 and Mp2 in the ESD detection circuit will be turned on to generate the substrate-triggered current to quickly trigger the STNMOS on. The measured voltage waveforms have successfully verified the excellent turn-on efficiency of the new proposed power-rail ESD clamp circuit.

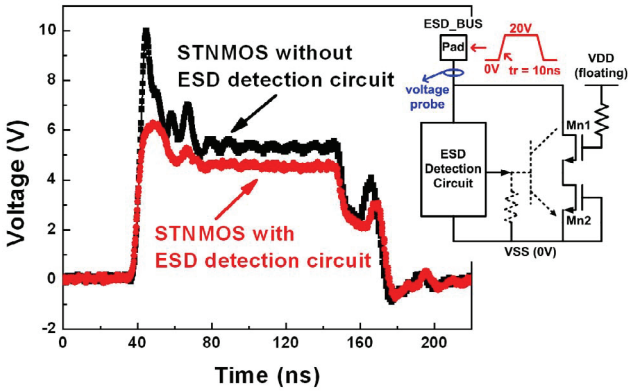

Figure 5. Measured voltage waveforms to verify the turn-on efficiency of the high-voltage-tolerant power-rail ESD clamp circuit with STNMOS.

B. *ESD Robustness*

Transmission line pulsing (TLP) generator with a pulse width of 100ns is used to verify the secondary breakdown current (It2) of the STNMOS with or without ESD detection circuit. The measured TLP I-V curves of the STNMOS with device dimension (W/L) of 240μm/0.2μm are shown in Fig. 6. The STNMOS with ESD detection circuit can be triggered on at a lower voltage level. On the contrary, the STNMOS without ESD detection circuit can not be triggered on until a higher transient voltage level of ~6V is reached. The snapback phenomenon of the STNMOS with ESD detection circuit disappears due to the substrate-triggered current generated by ESD detection circuit. In addition, the turn-on uniformity among the multiple fingers of STNMOS can be improved to enhance its ESD robustness by the substrate-triggered effect [9]. As comparing with the stand-alone STNMOS, the secondary breakdown current (It2) of the STNMOS with the proposed ESD detection circuit can be increased from 1.4A to 2.4A in Fig. 6.

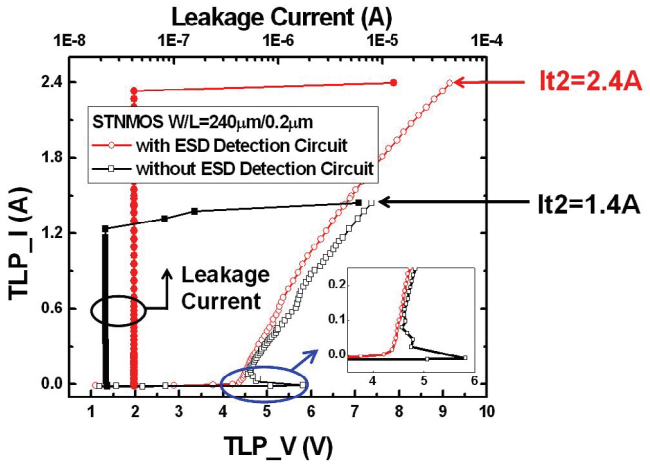

Figure 6. TLP-measured I-V curves of STNMOS with or without ESD detection circuit.

The human-body-model (HBM) and machine-model (MM) ESD level of STNMOS devices with different device dimensions are shown in Table I. In these ESD verifications, the HBM and MM ESD levels are measured by *KeyTek ZapMaster* and the failure criterion is defined as the I-V characteristic curve shifting over 20% from its original curve after three continuous ESD zaps at every ESD test level. With the substrate-triggered current generated from the proposed ESD detection circuit, the turn-on uniformity of STNMOS can be effectively improved. The HBM (MM) ESD levels of the STNMOS with ESD detection circuit under channel width of 240, 360, and 480μm with channel length of 0.2μm are improved from 3, 4, and 5 kV (175, 250, and 275 V) to 4, 5, and 6.5 kV (225, 300, and 400 V), respectively, as compared with the stand-alone STNMOS. Therefore, with better turn-on speed and turn-on uniformity, the new proposed power-rail ESD clamp circuit is superior ESD protection design compared to the stand-alone STNMOS.

Table I

HBM and MM ESD levels of the STNMOS devices with or without the ESD detection circuit.

STNMOS W/L (μm/μm)	HBM ESD Level (kV)		MM ESD Level (V)	
	without detection circuit	with detection circuit	without detection circuit	with detection circuit
240/0.2	3	4	175	225
360/0.2	4	5	250	300
480/0.2	5	6.5	275	400

V. Conclusion

A new high-voltage-tolerant power-rail ESD clamp circuit for 1.2/2.5-V mixed-voltage I/O interfaces has been proposed and successfully verified in a 0.13-μm CMOS process. With the substrate-triggered current generated from the ESD detection circuit, the turn-on speed and ESD robustness of STNMOS has been significantly increased. The HBM (MM) ESD level can be improved from 5kV (275V) to 6.5kV (400V) for the STNMOS with a device dimension (W/L) of 480μm/0.2μm. ESD stresses on the mixed-voltage I/O pad and pin-to-pin ESD stresses can be effectively discharged by the proposed ESD protection scheme with the high-voltage-tolerant power-rail ESD clamp circuit.

Acknowledgement

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