P-45: On-Chip ESD Protection Design for UXGA/HDTV LCoS in 0.35-μm CMOS Technology

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Abstract
A successful electrostatic discharge (ESD) protection design scheme for UXGA/HDTV LCoS product has been proposed and verified in this paper. HBM and MM ESD robustness of the LCoS with both of low-voltage (LV) and high-voltage (HV) ESD protection design can achieve above 3.5kV and 200V. The analysis on I-V curve shifting of I/O pin shows the ESD damages on the GGNMOS in I/O ESD protection.

1. Introduction
Liquid Crystal on Silicon (LCoS) displays can provide high resolution, high brightness, and low power consumption, compared to the traditional CRT or LCD display. LCoS, combined the superiority of excellent picture quality of LCD with the high manufacturing efficiency of the mature CMOS technology, will be a potential low-cost technology for production of high-definition light value [1], [2]. Because the large display area of LCoS filled with Liquid Crystal (LC) sandwiched between the Si substrate and a glass plate, the peripheral I/O circuits are almost core-limited design. For consideration of the large die size with pixel region and high pin counts of LCoS, electrostatic discharge (ESD) protection scheme should be optimized to have efficient ESD discharging paths [3].

In display technology, ESD robustness of TFT-LCD had been studied [4]-[6]. In CMOS technology, ESD protection of high voltage application had also been studied [7]. ESD reliability of LCoS combining the CMOS and display technology will be a worthy issue. Until now, none paper mentioned about how to design the ESD protection in such a large scale LCoS product. In this paper, a successful ESD protection design with multiple efficient power-rail ESD clamp circuits has been demonstrated for 1-inch UXGA/HDTV LCoS display to achieve the HBM and MM ESD robustness of over 3.5kV and 200V, respectively.

2. UXGA/HDTV LCoS Panel
2.1 LCoS panel

The UXGA/HDTV LCoS panel integrates the scan driver, data driver, controller, and pixel region on the Si substrate in 0.35-um HV CMOS process. The location of circuit blocks of this UXGA/HDTV LCoS display is illustrated in

Fig. 1. The resolution of this LCoS with 1920(+24) × 1200(+24) can support to HDTV/UXGA. The detail specification of this LCoS product is shown in Table 1. The die size of the LCoS panel is 20289.6μm × 16841.5μm, which is a challenge to effective ESD protection design.
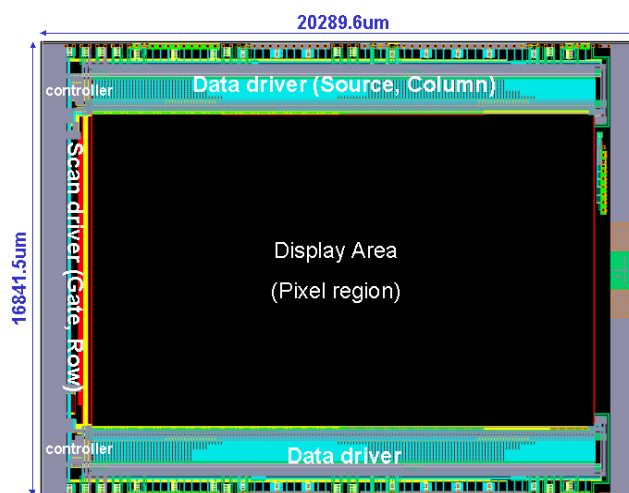

Figure 1 The UXGA/HDTV LCoS panel integrates the scan driver, data driver, controller, and pixel region on the Si substrate.

Table 1 The specification of the LCoS panel.

Resolution	1920(+24)×1200(+24)
Gray scale	8 bits
Frame rate	120 Hz
Aspect ratio	16：9 or 4：3
Display area	1 inch
Cell gap	2 μm
Liquid crystal alignment	Vertical alignment
Contrast ratio	500：1

2.2 ESD protection design for LCoS

LCoS with 140 pin counts has HV and LV circuits, which are shown in Fig. 2. The 3.3V I/O and 12V I/O circuits are separated with independent power (VDD, VDD12A) and

ground (VSS, VSS12A). Whole chip ESD protection design including the I/O ESD cells and the power-rail ESD clamp circuits are shown in Fig. 3. The I/O ESD cell is placed at each pad, and the power-rail ESD clamp circuits should be inserted between the VDD and VSS power lines. The number of the inserted power-rail circuits is dependent on the parasitic resistance along the power lines. Typically, between 1000~1500μm, a power-rail ESD clamp circuit is inserted between the power lines of I/O cells.
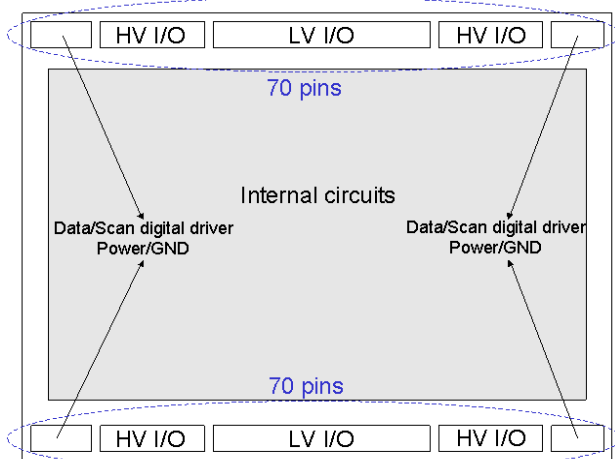

Figure 2 The layout top-view of HV and LV I/O circuits on the LCoS.

The whole-panel ESD protection design is illustrated in Fig. 4. The geometric size of gate-VDD PMOS (GDPMOS) and gate-grounded NMOS (GGNMOS) are 400μm/2μm (400μm/1μm) for I/O ESD protection in HV part (LV part). Moreover, the power-rail ESD clamp circuit with substrate-triggered technique is formed by a field oxide device (FOD) as ESD clamp device and the ESD detection circuit [8]. The power-rail ESD clamp circuit is designed to be turned on when ESD voltage appears across the VDD and VSS power lines. But, this power-rail ESD clamp circuit is kept off when the chip is under the normal power-on condition. To meet these requirements, the RC time constant in the power-rail ESD clamp circuit is designed about 0.1~1μs to achieve the desired operations. The layout top-views of the I/O ESD devices with GDPMOS and GGNMOS and the power-rail ESD clamp circuit are shown in Figs. 5(a) and 5(b), respectively.
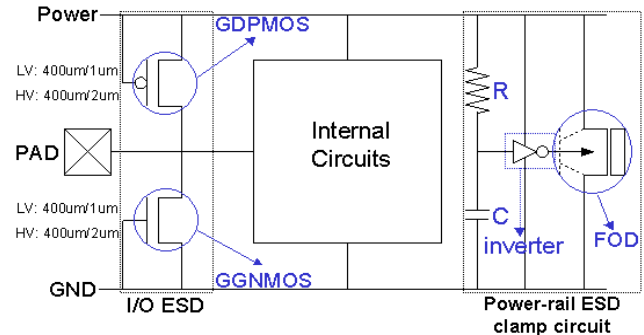

Figure 4 The whole-panel ESD protection design with substrate-triggered power-rail ESD clamp circuit.
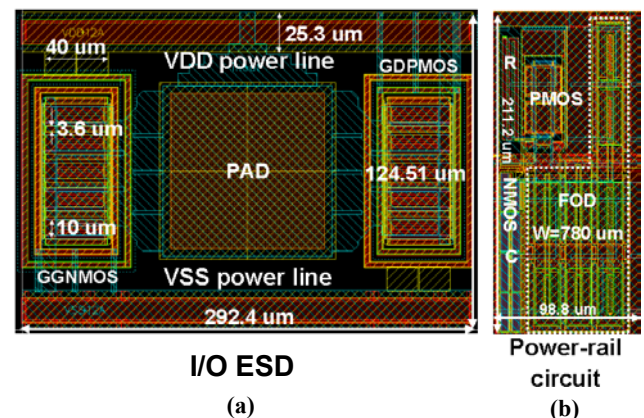

Figure 5 The layout top-views of (a) I/O ESD devices with the GDPMOS and GGNMOS, and (b) power-rail ESD clamp circuit.
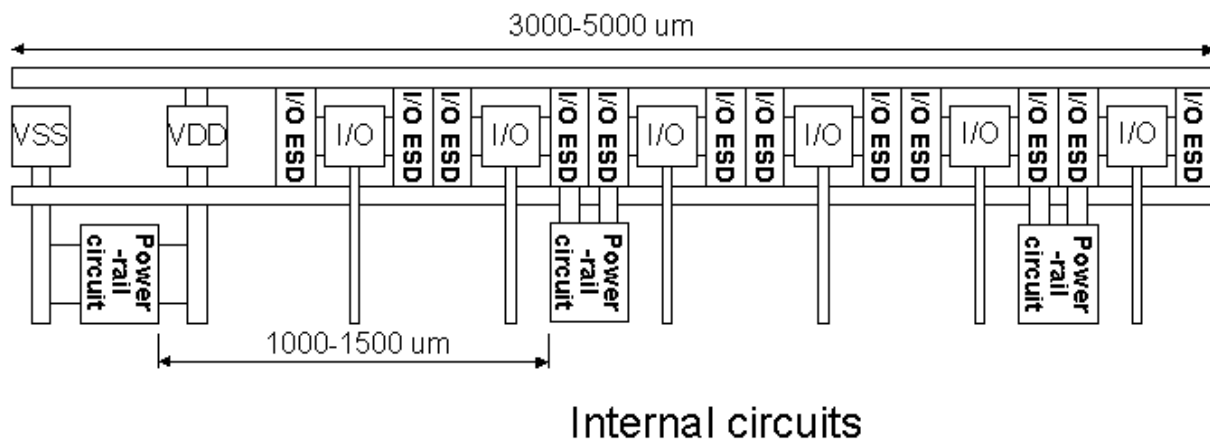

Figure 3 ESD protection design with power-rail ESD clamp circuits to the I/O circuits.

2.3 Efficient VDD-to-VSS ESD Clamp Circuit

To efficiently clamp the ESD voltage between VDD and VSS power lines before the internal circuits are damaged, the ESD-transient detection circuit is used to trigger on the parasitic NPN BJT of VDD-to-VSS ESD clamping FOD [8], as illustrated in Fig. 6. The ESD-transient detection circuit is designed to detect the ESD event and sends a triggering current to the base terminal of the parasitic BJT of the ESD-clamping FOD. Because the ESD-clamping FOD is turned on by the substrate triggering current rather than by the junction breakdown, the FOD can be turned on at a lower voltage to bypass ESD current before the ESD overstress voltage damages the internal circuits. The ESD-transient detection circuit is biased by the ESD energy and triggers the ESD-clamping FOD to provide a low-impedance path between the VDD and VSS power lines to bypass ESD current. Thus, the ESD current can be efficiently discharged through the forward-biased diode Dp1(Dn1), the ESD-clamping FOD, to VSS(VDD) in the PS-mode(ND-mode) ESD zapping [3]. The current path is also shown in Fig. 6.
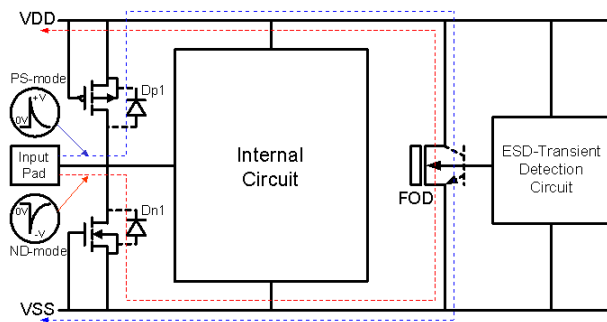

Figure 6 An effective VDD-to-VSS ESD protection design to achieve the whole-panel ESD protection.

3. Experimental Setup
3.1 Models of ESD Events

In IC industry, the standards of ESD stress models have been derived for ESD test methods. The Human Body Model (HBM) and the Machine Model (MM) are the general ESD test methods for commercial ICs. The equivalent circuits of HBM and MM ESD events are introduced in Fig. 7. For general ESD specification of commercial ICs, the HBM and MM ESD robustness of ICs should be at least 2kV and 200V under all pin combinations of ESD zapping [9].
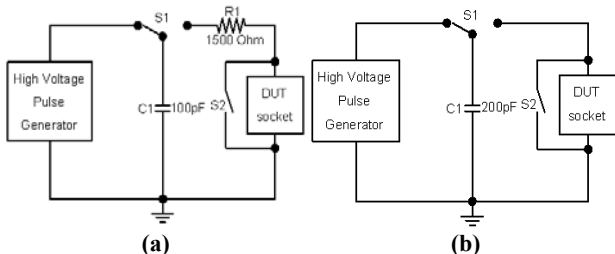

Figure 7 The equivalent circuits of (a) human-body model, and (b) machine model, ESD events.

3.2 ESD Testing

Since ESD charge may have positive or negative polarity, there are four modes of ESD zapping on each I/O pins, such as positive-to-VDD (PD), positive-to-VSS (PS), negative-to-VDD (ND), and negative-to-VSS (NS) modes. Moreover, there are two modes of ESD testing on power pins includes positive VDD-to-VSS and negative VDD-to-VSS modes, as shown in Fig. 8 [3]. After I/O pins and power pins are tested by ESD simulator, ESD robustness of the IC is decided by the worst case.
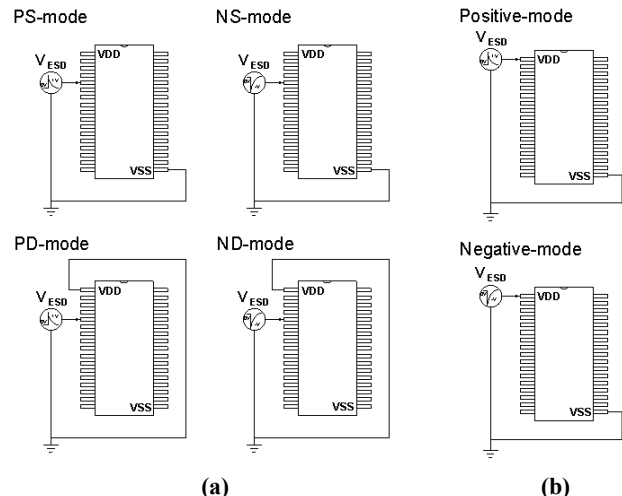

(a)   (b)

Figure 8 ESD testing for IC products with different pin combinations, (a) I/O pin to power pins, and (b) power pin to power pin.

4. Results and Discussion
4.1 ESD robustness of the LV part

Whole-panel ESD protection design in LV part is the same as that in HV part, including the LV I/O cells and LV power-rail ESD clamp circuits with substrate-triggered technique. Due to the high ESD immunity of LV device, the HBM and MM ESD level of LV part is above 6kV and 600V, as shown in Table 2. After the ESD stress of 6kV, the I/O ESD cell has no damages at the LV part.

4.2 ESD robustness of the HV part

Generally, ESD robustness of HV device should be weaker than that of LV device due to high breakdown voltage and high holding voltage. Therefore, the ESD robustness of LCoS with both LV and HV parts will be dominated by the HV part. HBM ESD immunity of the I/O pins in HV part is over 5kV in NS-mode, ND-mode, and PD-mode due to the efficient HV power-rail ESD clamp circuits. In the PS-mode ESD stress, ESD robustness of some I/O pins only pass 3.5kV. DC I-V curve shifting of the I/O pin after PS-mode HBM ESD zapping of 3.75kV is shown in Fig. 9. The tracing method is setup to sweep I/O pin when VDD and VSS are grounded, as shown by the inserted picture of Fig. 9. Due to the junction damage of I/O device, I/O signal

shorts to ground. In order to identify which device or junction is damaged, I/O pin to VDD under VSS floating, and I/O pin to VSS under VDD floating, are measured in Fig. 10 and Fig. 11, respectively. These two figures show that the GDPMOS has no damage but the GGNMOS is shorting to ground after PS-mode ESD zapping. To further increase the PS-mode ESD level, the layout of GGNMOS should be drawn with a wider spacing between the drain contact to its poly-gate edge. In addition, the MM ESD robustness is also over 200V in PS-mode, NS-mode, PD-mode, and ND mode, as shown in Table 2.

**Table 2 The ESD failure voltage of the LCoS panel under PS, NS, PD, ND, VDD(+)and VDD(-) ESD zapping modes.**

|		PS	NS	PD	ND	VDD(+)	VSS(-)
HBM	LV	>6.0 kV	>6.0 kV	>6.0 kV	>6.0 kV	>6.0 kV	>6.0 kV
	HV	~3.75 kV	>6.0 kV	~5.0 kV	>6.0 kV	>6.0 kV	>6.0 kV
MM	LV	>600 V	>600 V	>600 V	>600 V	>600 V	>600 V
	HV	~225 V	~250 V	~250 V	~225 V	~225 V	~225 V

Failure Criteria:

$\triangle V > +/- 30\%$ of V_{REF} (relative method)

V_{REF}: The measured voltage at +/- 1uA before zapping.

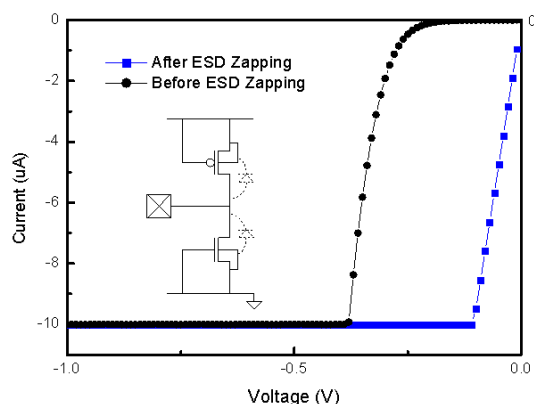$\triangle V$: The voltage changes at +/- 1uA after zapping.
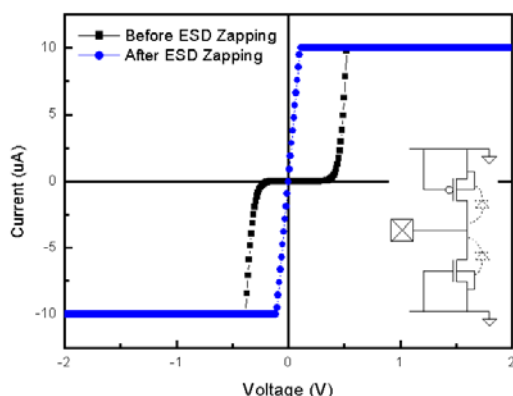
Figure 9 The DC I-V curves shifting of I/O pin with VDD pin and VSS pin grounded after 3.75 kV PS-mode HBM ESD zapping.
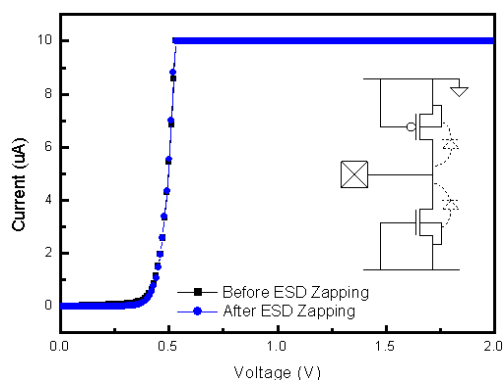
Figure 10 The DC I-V curves shifting of I/O pin with VDD pin grounded and VSS pin floating after PS-mode HBM ESD zapping.

Figure 11 The DC I-V curves shifting of I/O pin with VDD pin floating and VSS pin grounded after PS-mode HBM ESD zapping.

5. Conclusion

The 1-inch UXGA/HDTV LCoS product with successful ESD protection design has been verified with high ESD robustness. ESD protection design including both I/O ESD cells and efficient power-rail ESD clamp circuits can create more ESD current conducting paths. Such ESD protection design applied in large scale LCoS with LV and HV parts can achieve HBM and MM ESD levels of at least 3.5 kV and 200 V, which is dominated by HV part.

6. References

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