Investigation on RF Characteristics of Stacked P-I-N Polysilicon Diodes for ESD Protection Design in 0.18-μm CMOS Technology

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ABSTRACT

An ESD protection design by using the stacked P-I-N polysilicon diodes for CMOS RF integrated circuits is proposed to reduce the input capacitance and to avoid the noise coupling from the common substrate. In this paper, the dc I-V characteristics, RF S-parameters, and ESD robustness of the stacked P-I-N polysilicon diodes are investigated in a 0.18-μm salicided CMOS process. This polysilicon diode with small parasitic capacitance and high ESD robustness is fully process compatible to general CMOS process without extra process modification.

INTRODUCTION

For wireless system applications, the ESD protection device in GHz RF ICs is required to have low parasitic capacitance, broadband and constant capacitance, insensitive to substrate coupling noise [1], and high enough ESD robustness. In order to fulfill these requirements, diodes are commonly used for ESD protection in I/O circuit. Because multiple capacitors stacked in series can result in a total capacitance smaller than that of a single capacitor, the diode string is one solution that has been applied for RF ESD protection design. However, the conventional p+/n-well diode string has the p-n junction located within the common substrate of CMOS ICs, which may cause some issues. First, the substrate noise may be coupled into the RF input node through the conventional diodes to seriously degrade circuit performance of RF IC. Second, the leakage current constructed by the parasitic vertical p-n-p bipolar transistors in the diode string is increased exponentially with increasing the voltage difference from anode to cathode [2]. Third, the additional N-well to P-substrate junction capacitance in every p+/n-well diode structure causes some increase in the total parasitic capacitance.

Therefore, a P-I-N polysilicon diode for ESD protection in RF broadband and wireless system applications was proposed [3]. Because the polysilicon diode is isolated far away from the common substrate by the thick field-oxide layer, it is free from the substrate noise coupling problem and can be connected in series to further reduce the total parasitic capacitance.

In this paper, in order to further understanding the impact to RF performance, S-parameters of the stacked P-I-N polysilicon diode under forward-biased condition are investigated in 0.18-μm CMOS process. The spacing between the N+ and P+ regions and the total width of the P-I-N polysilicon diode may affect the device characteristics, which will be investigated in the experimental test chips.

STACKED POLYSILICON DIODE

The structure of the stacked polysilicon diodes is shown in Fig. 1. The polysilicon layer is drawn with separated P+/N+ doping regions to realize the diode structure [3]. Between the N+ and P+, there is a region indicated "I" without doping impurity. To use polysilicon diode as an effective ESD protection device in GHz RF ICs, the RF characteristics of polysilicon diodes with the center region "I" under different layout spacing S and different total junction perimeters W must be investigated. The fabrication of polysilicon diode is fully process compatible to general CMOS process without extra process modification.

MEASUREMENT RESULTS AND DISCUSSION

The ESD stress is performed with a *Paragon* ESD simulator. The measured ESD robustness of the P-I-N polysilicon diodes with different spacing and width are shown in Table I. Each measurement is performed on 3 samples. In Table I, because a polysilicon diode with smaller layout spacing has a lower turn-on resistance, it has a relatively higher ESD level. When the total junction perimeter (width) is increased, the ESD robustness of the polysilicon diodes is increased. The ESD robustness of the stacked P-I-N polysilicon diodes under forward-biased condition with N+/P+ spacing S of 0.6 μm and junction perimeter (width) of 600 μm are shown in Table II. Increasing the number of polysilicon diodes in the stacked configuration does not reduce its ESD robustness.

The S-parameters of these ESD protection schemes have been measured on wafer with two-port ground-signal-ground (G-S-G) probes from 1-to-10 GHz and make a calibration with de-embedding techniques. The RF measurement system (HP-8510B) is used to measure the S-parameters of the polysilicon diodes under different diode dimensions. The parasitic capacitance can be extracted from the measured S-parameters. Fig. 2 shows the parasitic capacitances of the polysilicon diodes under different junction perimeter (width). The parasitic capacitance and ESD robustness are both increased by the increase of junction perimeter (width) under forward-biased condition. Fig. 3 shows the parasitic capacitance of the polysilicon diodes with junction perimeter (width) of 600 μm but different spacing S. When the spacing S of the polysilicon diode is 0.6 μm and junction perimeter (width) is 600 μm, the capacitance approaches 200 fF. A typical request on the maximum loading for GHz RF ESD protection device was specified as ~200 fF [4]. Therefore, the P-I-N polysilicon diode with the spacing of 0.6 μm and junction perimeter (width) of 600 μm is suitable for GHz RF applications.

Fig. 4 shows the measured total parasitic capacitance for stacked polysilicon diodes with different diode numbers. The parasitic capacitance is decreased apparently when the number of stacked polysilicon diodes is increased. Therefore, for higher RF operating frequency applications such as WiMAX which required much lower input parasitic capacitance, the stacked P-I-N polysilicon diode is a good choice for RF ESD protection. The 1-to-10-GHz S21 and S11 of polysilicon diodes with different numbers of stacked diodes are shown in Fig. 5. The insertion loss S21 of these polysilicon diodes with the same device dimension is decreased when the operation frequency is increased. However, the S21 of the stack-3 polysilicon diodes is with a little decrease during the 1-to-10 GHz frequency band. With less degradation on RF performance and high enough ESD robustness, the proposed stacked polysilicon diodes will be a useful solution to GHz RF ESD protection.

CONCLUSIONS

ESD protection design with stacked P-I-N polysilicon diodes for GHz RF ICs has been experimentally investigated with ESD robustness and RF characteristics in a 0.18-μm salicided CMOS process. The experimental results have shown that the stacked polysilicon diodes with a low enough turn-on resistance in forward-biased condition are good enough to be the ESD clamp device for RF ICs. These polysilicon diodes can be further stacked to significantly

reduce the total input capacitance and to achieve high enough ESD robustness for GHz RF circuits.

REFERENCES

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Table I ESD robustness of the P-I-N polysilicon diodes under different layout parameters.

HBM ESD level		Junction Perimeter (Width) (μm)			
		600	300	240	100
Spacing (μm)	0.4	**6 kV**	**3 kV**	**2.5 kV**	**1 kV**
	0.6	**5 kV**	**2.5 kV**	**2 kV**	**500 V**
	0.8	**4 kV**	**2 kV**	**1.5 kV**	N/A
	1.0	**3 kV**	N/A	N/A	N/A

Table II ESD robustness of the stacked P-I-N polysilicon diodes under different numbers of stacked diodes.

Junction Perimeter (Width)=600 μm , Spacing=0.6 μm			
Stack numbers	Stack 1	Stack 2	Stack 3
HBM ESD level	**5 kV**	**5 kV**	**5 kV**

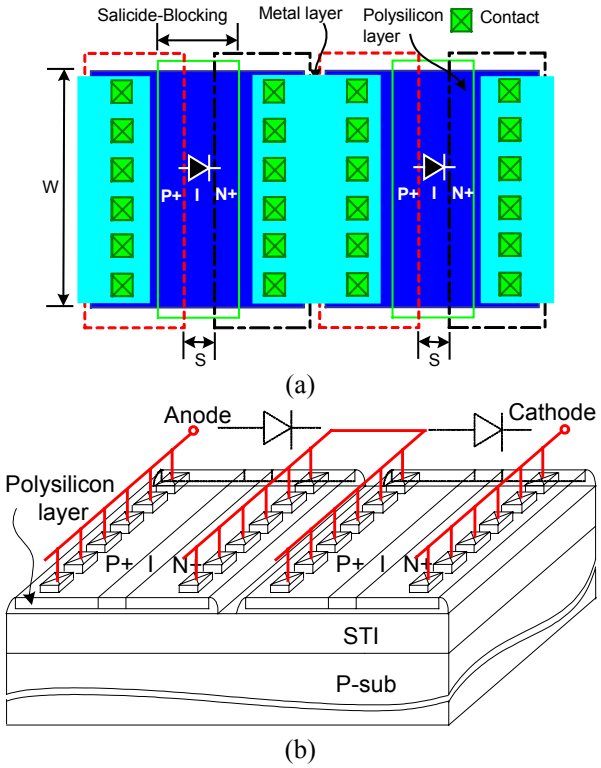

Fig. 1 (a) Layout top view, and (b) device structure, of the stacked polysilicon diodes realized in bulk CMOS technology.

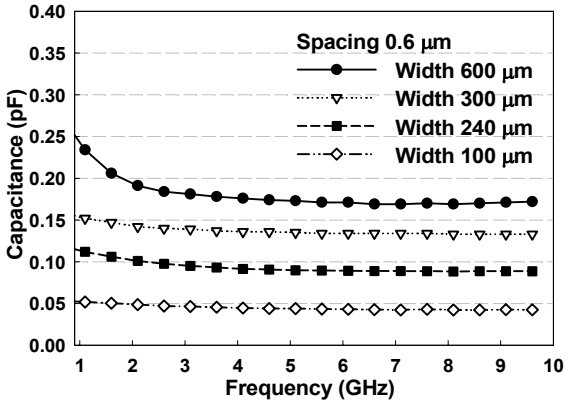

Fig. 2 The extracted parasitic capacitance of the P-I-N polysilicon diodes under different junction perimeter (width).

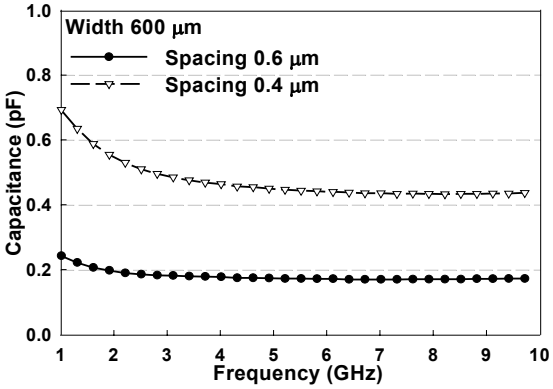

Fig. 3 The extracted parasitic capacitance of the P-I-N polysilicon diodes with different spacing of the center region "I:".

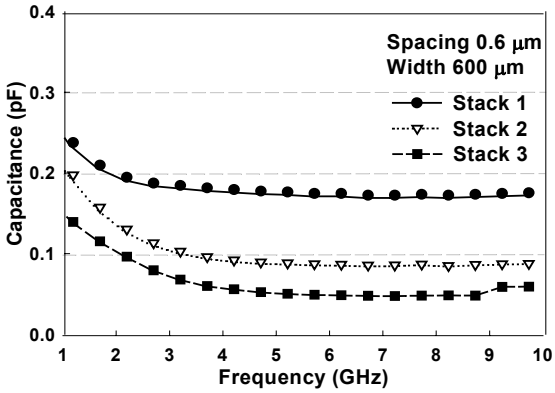

Fig. 4 The extracted parasitic capacitance of stacked polysilicon diodes measured with different numbers of stacked diodes.

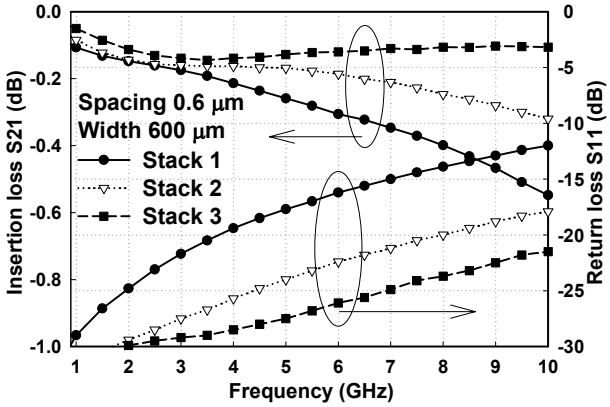

Fig. 5 The measured S21 and S11 of the stacked polysilicon diodes with different numbers of stacked diodes.