ESD Protection Design for Broadband RF Circuits With Decreasing-Size Distributed Protection Scheme

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***Abstract* — The resulting capacitive load, from the large electrostatic discharge (ESD) protection device for high ESD robustness, has an adverse effect on the performance of broadband RF circuits due to the impedance mismatch and bandwidth degradation. The conventional distributed ESD protection scheme using equal four-stage ESD protection can achieve a better impedance match, but degrade the ESD performance. A new distributed ESD protection structure is proposed in this work to achieve both good ESD robustness and RF performance. The proposed ESD protection circuit is constructed by arranging ESD protection stages with decreasing device size, named decreasing-size distributed ESD (DS-DESD) protection scheme, which is beneficial to the ESD level. The experimental results had shown the human-body-model (HBM) ESD robustness of up to 8kV.**

***Index Terms* — Electrostatic discharge (ESD), distributed ESD (DESD), coplanar waveguide, broadband RF circuits.**

I. Introduction

ESD is one of the most serious reliability issues in IC manufacturing. With the continuous scaling of CMOS technology and rapid increase of operating frequencies, providing effective ESD protection to protect the circuits has become a challenge. The main ESD protection design tradeoff in wireless (RF) and high-speed (broadband) applications is to achieve high ESD protection level (beyond 4 kV HBM ESD level) and not to affect the performance of the core circuits under normal circuit operating conditions. Therefore, the protection devices in such RF circuits are designed with small size [1], and placed close to the I/O pins. However, with the continuously increasing frequencies, this scheme has its limitation due to the parasitic capacitances of the small protection devices, causing severe impedance mismatch. To improve the impedance match, a distributed ESD protection scheme, which employs line segments between ESD protection devices, was proposed, as that shown in Fig. 1. In recent works, the distributed ESD protection scheme has achieved either great ESD protection or excellent broadband RF performance, but not both of them [2]-[5]. In [2], the protection devices, gate-grounded NMOS devices, were designed with series N-well resistors in the drains of the NMOS, beneficial for uniform turn-on during ESD events, to achieve high ESD level, but due to the large thermal noise contributed by the resistors, they are not compatible in high frequency systems. In [3]-[5], a four-stage distributed ESD protection using ESD devices (p-diodes and n-diodes) with equivalent size attained a superior impedance match over a broad frequency range in theory, but the ESD robustness was not proven in any silicon chips. The first stage of the four-stage distributed ESD protection structure will be first damaged by ESD energy, therefore to cause a low ESD robustness.

In this paper, a new distributed ESD protection scheme is proposed to provide both excellent RF performance and ESD robustness. The experimental test chip in a 0.25-μm CMOS process has demonstrated the ESD robustness of up to 8kV.

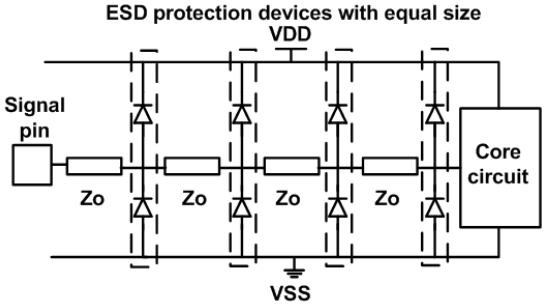


Fig. 1. The traditional distributed ESD protection design with equal-size diodes in four protection stages [3]-[5].

II. New Distributed ESD Design

A. Concept of the New Distributed ESD Design

From the perspective of ESD protection, the protection devices should be designed with large size to sustain ESD discharging current (typically, a 2-kV HBM ESD event with a peak ESD current of 1.3A) and placed near the signal pins, as shown in Fig. 2. But, for broadband RF performance, the protection devices are preferred to be divided into many small units with the same size connected by transmission lines (T lines) or inductors, as those shown in Fig. 1. The dilemma is overcome by the new proposed ESD protection scheme, as that illustrated in Fig. 3. This new proposed ESD protection structure allocates the ESD protection devices with decreasing size from the signal pin to the core circuit, which is called as the decreasing-size distributed ESD (DS-DESD) protection scheme.

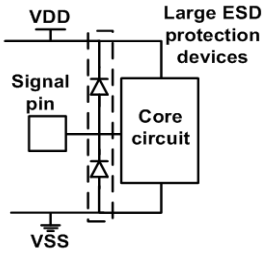


Fig. 2. The traditional ESD protection design with large devices close to the signal pin to sustain the ESD stress.

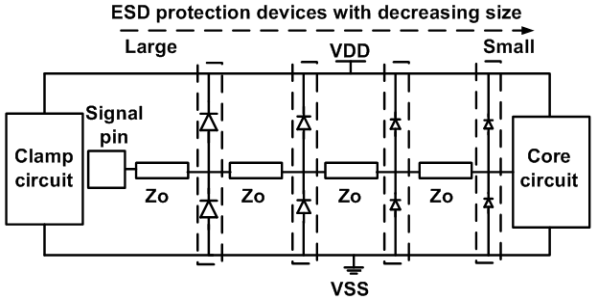


Fig. 3 The new proposed decreasing-size distributed ESD (DS-DESD) protection scheme.

B. RF Performance Analysis with Smith Chart

S-parameter is often used in RF system to show the performance of the network. Starting with a standard 50-Ω system which is commonly found in RF systems, two different implementations of ESD protection schemes are investigated, as those shown in Figs. 4(a) and 4(b). Fig. 4(a) shows the traditional equal-size distributed ESD (ES-DESD) protection scheme [3]-[5]. The new proposed DS-DESD protection is shown in Fig. 4(b). The source and internal resistances are both 50 Ω. In each circuit, the protection devices are modeled as capacitances. It was demonstrated that ESD protection using coplanar waveguide with under grounded shield (CPWG) can provide excellent RF performance for frequencies over 10 GHz [6], so they were used in this ESD protection design with a characteristic impedance of Zo.

Diodes are commonly used for ESD protection in RF systems due to their low capacitances. Here, the shallow-trench-isolation (STI) diodes are employed due to their high Q value and great ESD robustness [7]. Initially, the total ESD capacitance, Cesd, is assumed to be 200 fF, a value sufficient to reach the 2-kV ESD protection level [8], and the characteristic impedance (Zo) is employed as 70 Ω. S-parameter simulations over the frequency range 1 - 15 GHz were performed on these two circuits using the microwave circuit simulator ADS to generate the reflection parameter S11 and the transmission parameter S21 with the neglect on the loss in CPWG. The S11, related to the impedance match, is the main consideration to compare these two ESD protection schemes in Fig. 4. The match principles using Smith chart expressions, with the operating frequency set to 10 GHz, are both shown in Fig. 5. Each CPWG length has been optimized to reach the best match in each circuit and the centered point of Smith chart is normalized to 50 Ω. The serial number labeled on each point indicates the match procedure contributed by these components between the source and the core circuit.

Fig. 5(a) shows the S11 locus of Fig. 4(a), which introduces a good match condition. Fig 5(b) displays a similar match procedure as that of Fig. 5(a).

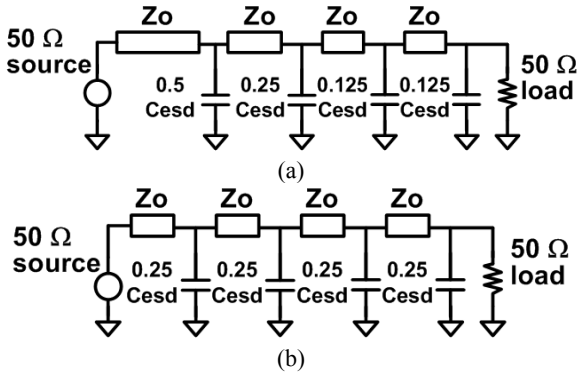


Fig. 4 Equivalent RF circuit models of (a) the traditional ES-DESD protection scheme and (b) the DS-DESD protection scheme. The total parasitic capacitance (200fF) of the ESD protection devices (diodes) is modeled as Cesd to ac ground.

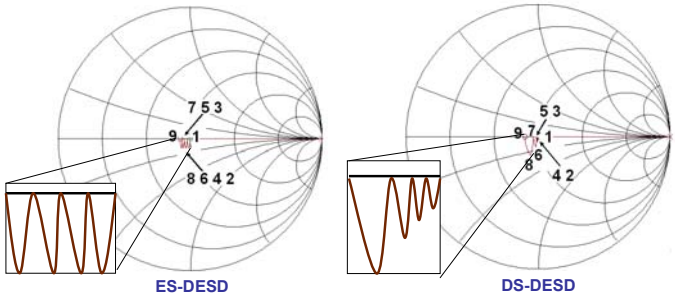


Fig. 5 The matching procedures of the ESD protection schemes in Fig. 4, expressed on Smith chart.

C. Considerations on RF ESD Protection

For an input pin, there are four modes of pin combinations during ESD stress, which are positive-to-VSS, negative-to-VSS, positive-to-VDD, and negative-to-VDD ESD stresses. The ESD level of an input pin is defined as the lowest ESD level among the four modes of ESD stresses. Therefore, the on-chip ESD protection design should provide effective discharge paths for the four-mode ESD stresses. The turn-on efficient VDD-to-VSS ESD clamp circuit, with RC-Inverter-NMOS ESD protection circuit, is applied to ensure the ESD protection devices operating in the forward-biased condition under the four ESD-stress modes on the I/O pad [9], [10].

To compare and analyze the ESD performance, the resistive ladder model of the ES-DESD protection scheme is employed, as shown in Fig. 6. According to [2], the large values of the series resistance of CPWG (Rc) and the resistance of ESD device (Resd) degraded ESD robustness when the ESD-generated power across them. Therefore, in order to enhance ESD protection level, to minimize Resd or Rc is, no doubt, the first way to be considered. The new proposed DS-DESD protection scheme reduces the Resd of the first stage, usually the most possible place to be damaged, by enlarging the size of the first pair of ESD protection devices. So, the proposed DS-DESD protection scheme will have better ESD robustness, as compared to that of ES-DESD protection scheme.

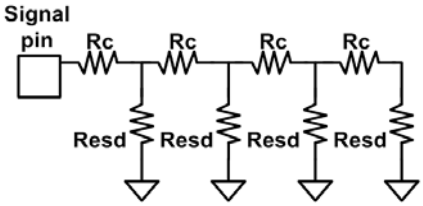
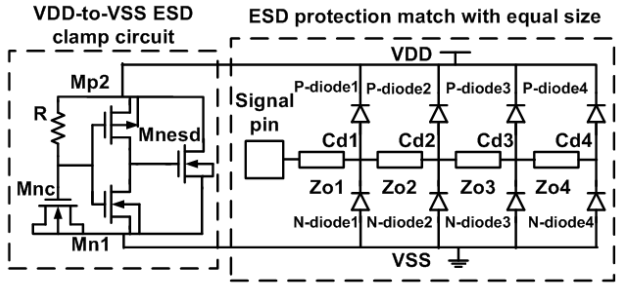
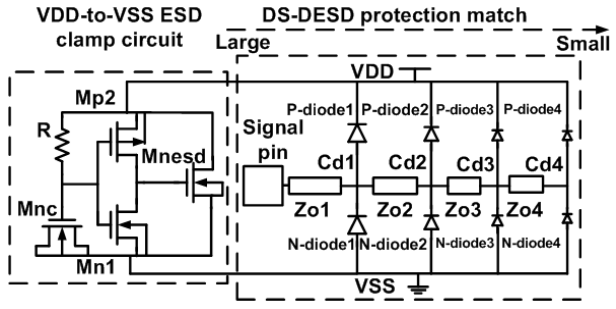


Fig. 6 The resistive ladder of the traditional ES-DESD scheme.



(a)



(b)

Fig. 7 (a) ES-DESD protection scheme, and (b) DS-DESD protection scheme, with the VDD-to-VSS ESD clamp circuit realized in a 0.25-μm CMOS technology.

III. Chip Implementation

To investigate ESD robustness of the new proposed DS-DESD scheme, the experimental test chip had been designed and fabricated in a 0.25-μm CMOS technology with 5 metal layers. The CPWG employed the top metal as the signal line and metal-1 as the grounded shield, hence the thickness of the signal line and the height between the signal line and metal-1 were fixed. The ways to adjust the characteristic impedance (Zo) of the CPWG were to change the width of the signal line and the spacing between the signal line and the coplanar ground. The impedance of 70 Ω with the signal-line width of 5.5 μm and spacing of 7.4 μm were chosen to make the resistive-ladder effect more obvious. Based on the fixed dielectric constant, the required length of CPWG can be determined. The STI p-diodes and n-diodes were chosen to shunt the ESD paths to VDD or VSS. Each pair of p- and n-diodes with a dimension of $5.5\times1.2\ \mu m^2$ contributes a parasitic capacitance of about 25 fF. The ES-DESD and DS-DESD protection schemes with the total parasitic capacitance 200 fF of ESD diodes and the VDD-to-VSS ESD clamp circuits were implemented and shown in Fig. 7

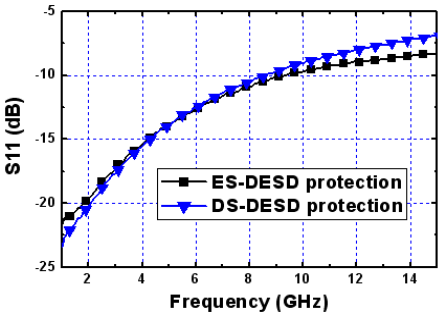
IV. Experimental Results and Discussion

Fig. 8(a) and 8(b) show the measurement results of the ES-DESD and DS-ESD protection schemes in Fig. 7. Comparing these two curves of S11 and S21, the performances between these two schemes only have some difference when the frequency up to 10 GHz. The S11 of ES-DESD scheme is a little smaller than that of DS-DESD when the frequency up to 10 GHz. But, the S21 of DS-DESD scheme is better than that of ES-DESD when the frequency up to 10 GHz. This is due to the loss of longer CPWG in the ES-DESD scheme (the DS-DESD scheme has a shorter length of total CPWG), which is realized by top metal 5 in a 0.25-μm CMOS technology. According to the results of Fig. 8, the DS-DESD protection scheme indeed achieves a good broadband RF performance as that of ES-DESD protection scheme.

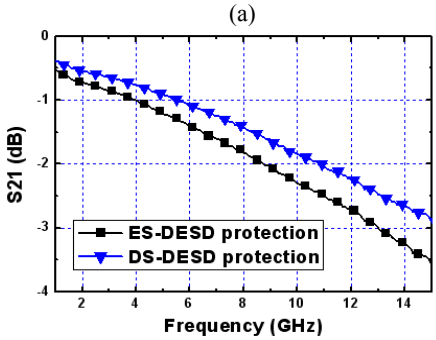
The human-body-model (HBM) ESD test results between these two ESD protection schemes, under the failure criterion of 30% I-V curve shifting at 1-μA current, are summarized in Table I which includes the negative-to-VDD (ND) and positive-to-VSS (PS) modes ESD stresses. The ND and PS modes of ESD stresses are the weakest modes in ESD protection for I/O pin with diodes as ESD protection devices [10]. The typical I-V curves shifting before and after ESD stress are shown in Fig. 9. The Mnesd in VDD-to-VSS ESD clamp circuit for both ES-DESD and DS-DESD ESD protection schemes is realized with device dimension of W/L=520μm/0.35μm in the test chip. The traditional ES-DESD protection scheme can sustain the HBM ESD level of 5.5kV, but that of DS-ESD can be improved up to >8kV.

The new proposed DS-DESD protection scheme

successfully provides much higher ESD levels in both ND and PS modes than that of ES-DESD. In order to make sure the ESD result consistent with the principle of the resistive ladder model, the failed circuits were de-processed to find the failure location. The EMMI (photon emission microscope) picture in Fig. 10 shows that the ESD damage is located on the junction of the first p-diode with a shining area after 5.5-kV HBM PS-mode ESD stress. The evidence in Fig. 10 has proved that the concept of the resistive-ladder model is correct.



(a)



(b)

Fig. 8 Measurement results on (a) S11, and (b) S21, of the ES-DESD and DS-DESD protection schemes in Fig. 7.

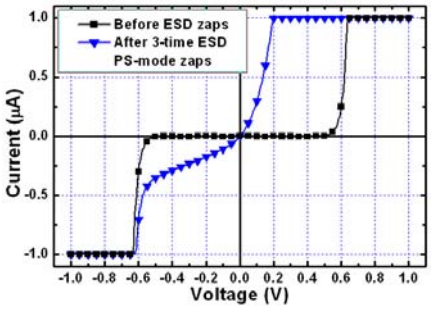


Fig. 9 I-V curves of the input diodes before and after ESD stress. The I-V curves are measured with both VDD and VSS relatively grounded.

TABLE I
HBM ESD LEVEL OF THE ESD PROTECTION SCHEMES IN FIG. 7.

Match type	ES-DESD Fig.7(a)	DS-DESD Fig.7(b)
ND-mode (kV)	5.5	> 8.0
PS-mode (kV)	5.5	> 8.0

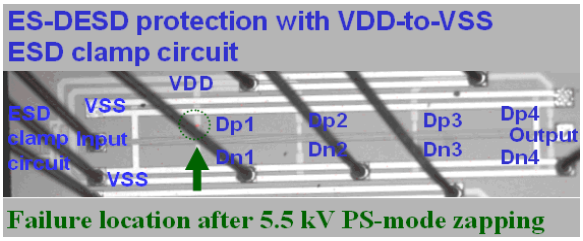


Fig. 10 The EMMI pictures to show the location of ESD damages on the ES-DESD protection circuit after PS-mode stress.

V. CONCLUSION

A new distributed ESD protection circuit with excellent broadband RF performance and great ESD level have been proposed and verified in a 0.25-μm CMOS process. Compared to the traditional equal-size distributed ESD protection scheme, the new proposed decreasing-size distributed ESD protection scheme has presented a comparable RF match and better ESD robustness. This new broadband ESD protection scheme is more useful for ESD design in broadband RF ICs.

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