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Investigation on seal-ring rules for IC product reliability in 0.25-μm CMOS technology

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Abstract

The distance between active region and the seal-ring location has been investigated in a 0.25-μm CMOS process. From the experimental results, this distance can be shrunk to only 5 μm without increasing leakage current and decreasing ESD robustness of the ESD protection devices after reliability tests of High-Accelerated Stress Test (HAST) and Temperature Cycling Test (TCT).

1. Introduction

In CMOS integrated circuits, the seal-ring structure is a necessary and important component for product reliability. The seal-ring structure is used to avoid introducing die-sawing stress and contaminants into the circuits of the chip. Therefore, the circuits of the whole chip should be enclosed by the seal-ring structure according to the foundry design rules. In addition, the scribe street surrounding the seal-ring structure is used for die saw requirements. The seal-ring structure consists of the contact/via strip and metal layers surrounding the active area of the chip. This contact and via must be a continuous ring uninterrupted by any gaps to block mobile ions from moving into the chip. In addition, P-type diffusion is placed underneath the contact as an extra substrate contact [1]. The typical seal-ring structure in a single-poly-five-metal (1P5M) 0.25-μm CMOS process is shown in Fig. 1 [2]-[4].

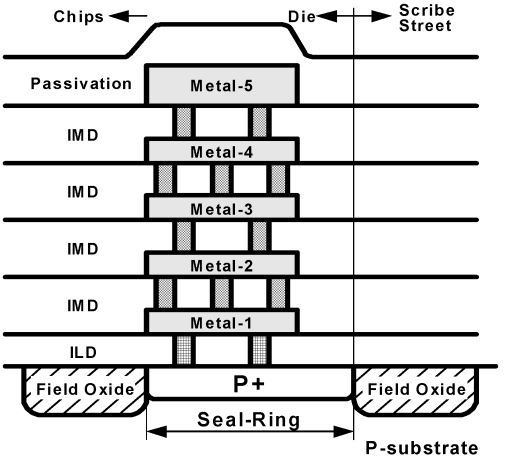

Fig. 1. The cross-sectional view of the seal-ring structure in a 0.25-μm CMOS process.

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Recently, the seal-ring structure has been co-designed with an ESD protection scheme to improve ESD robustness of the chip. The seal-ring structure has been modified and used as the on-chip ESD bus to overcome internal damages inside the IC with multiple separated power pins [5]. The distance from the seal-ring structure to the active devices are distinctly different from the layout styles of the I/O structures. In Figs. 2(a) and 2(b), the assembly distance is defined as the spacing between the seal-ring edge and the chip edge. However, the influence of this distance on the reliability of the active device may be different even with the same assembly distance. Therefore, the active distance, specially defining the distance between the seal-ring edge and the diffusion edge of the active devices, is used to really reflect the reliability concern of the active devices.

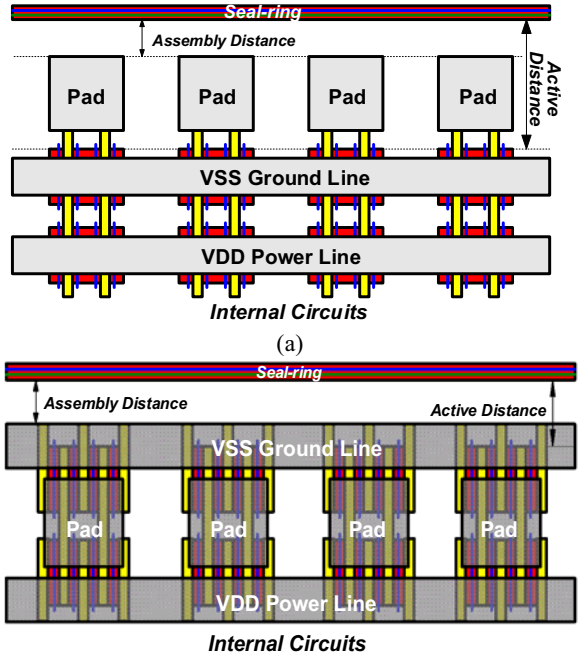


Fig. 2. Layout arrangements of (a) traditional I/O pads and (b) the I/O cells with the devices under pads. The active distance and the assembly distance are indicated in the figures, where the active distances are different in these two I/O layouts.

In this work, the ESD protection devices are placed between the seal-ring structure and the bonding pads to investigate the influence of active distance on the reliability of ESD protection devices. Furthermore, the influence of seal-ring dimension on the reliability of the ESD protection devices is also investigated. The testchips have been fabricated in a 0.25-μm salicided 1P5M CMOS process and assembled with the DIP-40-pin package for this investigation.

2. Device layout and reliability test

2.1. Device layout

The ESD protection devices including NMOS, N(P)-type field-oxide device (FOD), P+/N-well junction diode, silicon-controlled rectifier (SCR), are studied in this work. In order to investigate the influence of the layout style on the reliability concern, each ESD protection device is drawn with both horizontal layout style and vertical layout style. The layout arrangements of ESD protection devices between bonding pads and seal-ring are shown in Figs. 3(a) and 3(b). The detailed layout views of such ESD protection devices are illustrated in Fig. 4. The active distance (D1) is varied from 25 μm to 5 μm in each ESD protection device to investigate the influence of this distance on the reliability of devices. Furthermore, the seal-ring dimension is reduced to 5 μm (the original one is 10 μm) to investigate the reliability of the ESD protection devices with such a small seal-ring dimension. To eliminate the influence of the scribe street width on the results, the width of scribe street is kept at 80 μm.

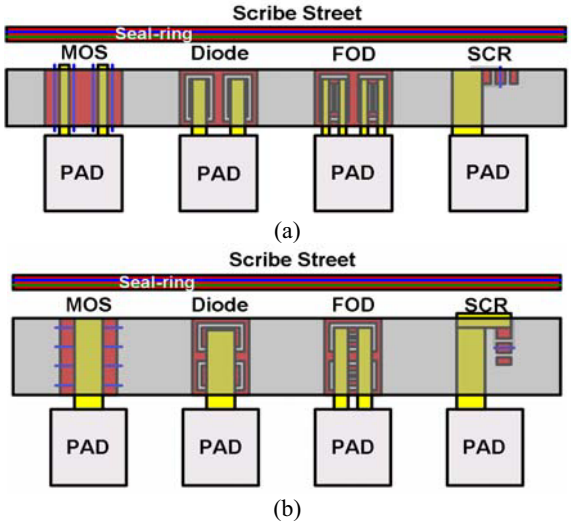


Fig. 3. Layout arrangements of the ESD protection devices with (a) horizontal layout style, and (b) vertical layout style, fabricated in a 0.25-μm CMOS process.

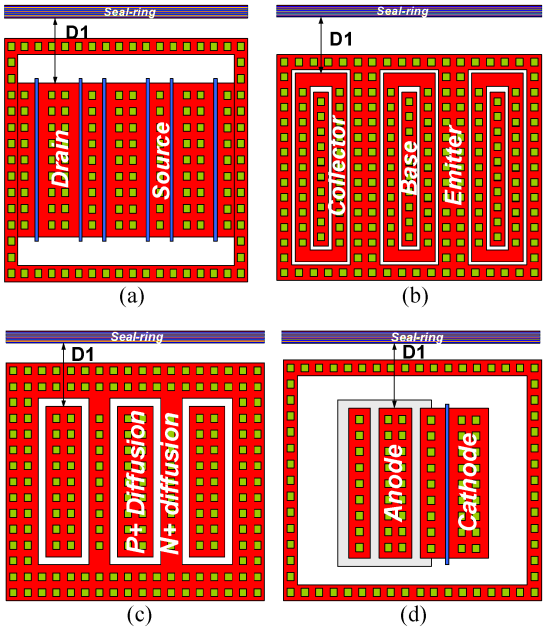


Fig. 4. The layouts of ESD devices (a) MOS, (b) FOD, (c) diode, and (d) SCR with indication of the active distance (D1) in each device.

2.2. Reliability test

In order to investigate the reliability of the ESD protection devices after die saw treatment, the devices are subjected to the stress from Highly-Accelerated Temperature and Humidity Stress Test (HAST) [6] and Temperature Cycling Test (TCT) [7]. The test conditions of HAST are with temperature of 130 °C, relative humidity of 85 %, and duration time of 100 hours according to the standard of JESD 22-A110-B [6]. In TCT, all specimens are placed in the thermal shock chamber under 100 cycles of high-low temperature stress. The conditions of high temperature and low temperature stresses are 150 °C and –65 °C, respectively, with the duration of 10 minutes at each temperature according to the standard of MIL-STD-883E method 1010.7 [7].

3. Experimental results

3.1. The influence of active distance

To confirm the function of the seal-ring structures, the leakage current (off-state current) of each test device was measured at 1.1 times of the normal maximum operation voltage (VDD). The leakage currents of the NMOS devices with the same channel width of 240 μm are below 1 nA in all active distances, as shown in Fig. 5 for the horizontal layout style. In addition, the measured results of the NMOS devices with the vertical layout style are shown in Fig. 6. The leakage currents of the NMOS after HAST and TCT did obviously not increase significantly for any of the experimental conditions. The leakage values of 4 pA/μm are related to the 0.25-μm technology specification. Figs. 7(a), 7(b), 7(c), and 7(d) show the leakage currents of N-type FOD, SCR, P-type diode, and P-type FOD, respectively, before and after reliability stresses. These leakage currents are also below 1 pA/μm in all test devices. According to these experimental results, the active distances can be reduced to 5 μm without increased reliability problems.

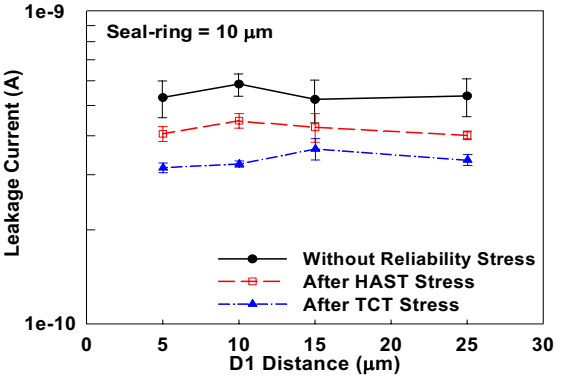


Fig. 5. The leakage currents of horizontal layout style NMOS devices with the same channel width of 240 μm are below 1 nA after die sawing and the reliability tests of HAST and TCT under the seal-ring dimension of 10 μm.

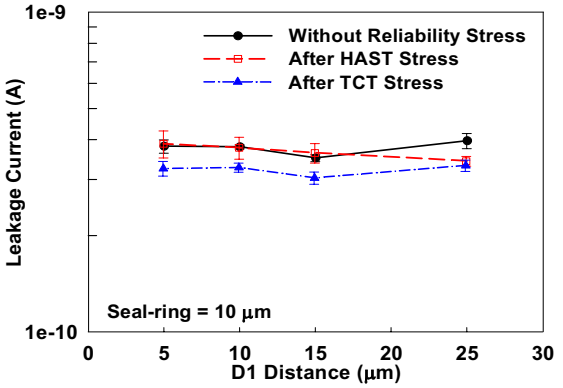
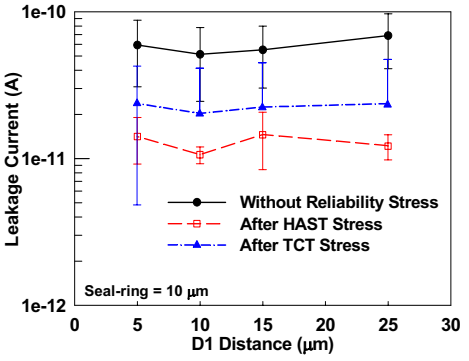
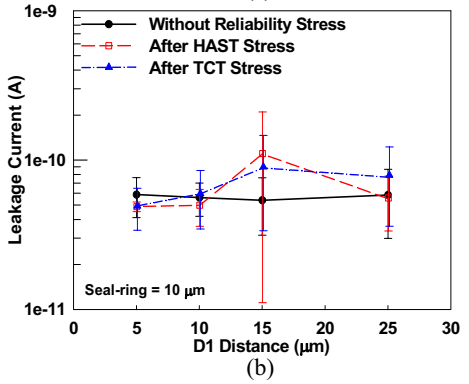


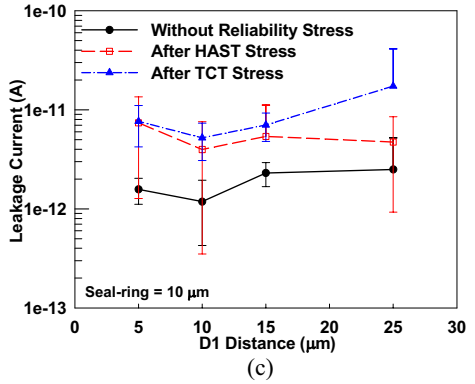
Fig. 6. The leakage currents of vertical layout style NMOS device with the same channel width of 240 μm are below 1 nA after die sawing and the reliability tests of HAST and TCT under the seal-ring dimension of 10 μm.



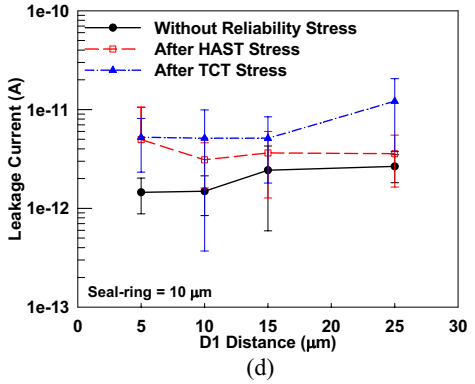
(a)



(b)

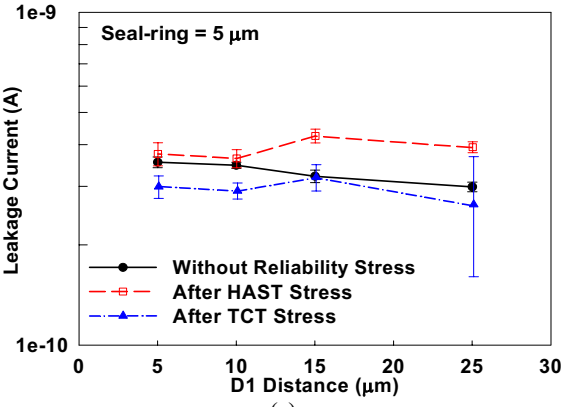


(c)

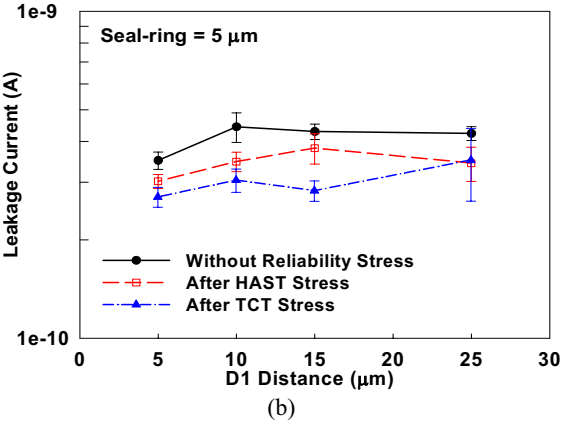


(d)

Fig. 7. The measured leakage currents in (a) N-type FOD, (b) SCR, (c) P-type diode, and (d) P-type FOD, which are below 1 pA/μm after HAST and TCT stresses.



(a)

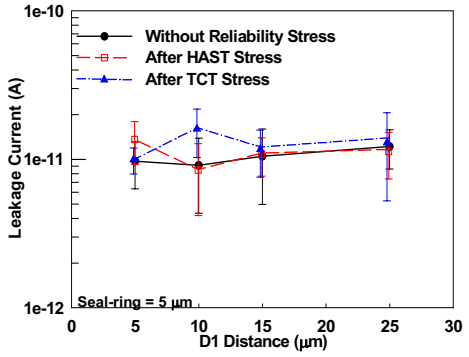


(b)

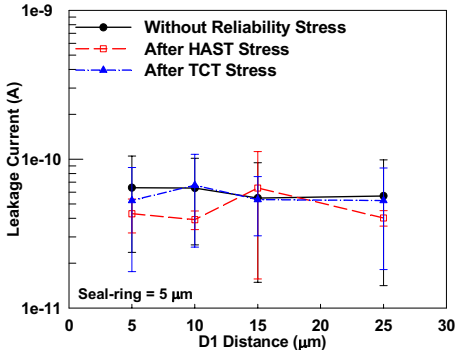
Fig. 8. Leakage currents of the NMOS devices with (a) horizontal layout style, and (b) vertical layout style, under a shrunk dimension of 5 μm in the seal-ring structure.

3.2. The Influence of seal-ring dimension

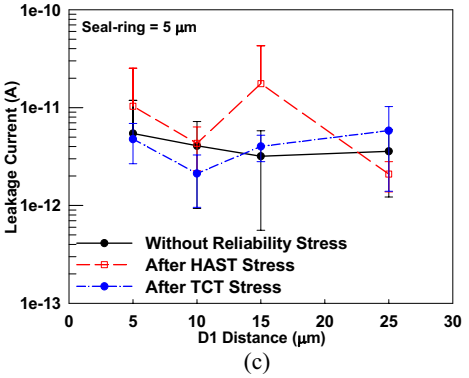
In order to investigate the efficiency of the seal-ring structure with reduced dimension of 5 μm, the leakage currents of the test devices with different D1 distances are also measured at the aforementioned experimental conditions. Figs. 8(a) and 8(b) show the leakage currents of the NMOS devices with different layout styles under the shrunk seal-ring structure of 5 μm (the original rule is 10 μm). The leakage currents are below 1 nA (4 pA/μm) for all active distances. The measured results of other test devices, such as N-type FOD, SCR, P-type diode, and P-type FOD are shown in Figs. 9(a), 9(b), 9(c), and 9(d), respectively. To clarify the impact of e.g. the die-sawing equipment, on the reliability concern of the test devices with the compact seal-ring structures, these testchips have been sawed and assembled in different back-end factories. However, the whole experimental results confirm that leakage currents are still within the 0.25-μm process specification.



(a)



(b)



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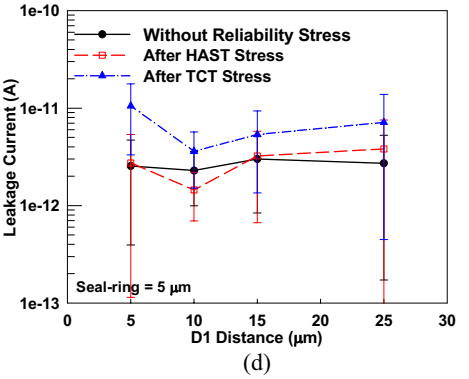
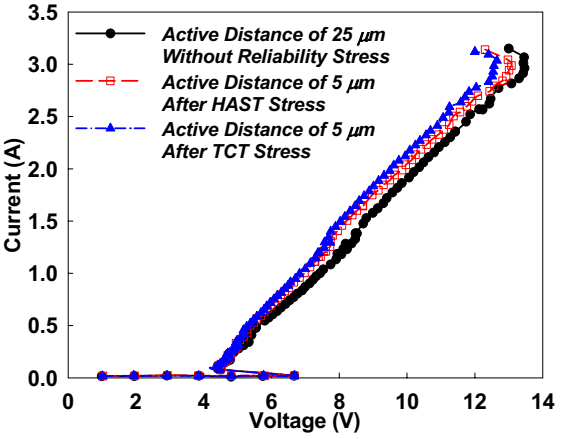


(d)

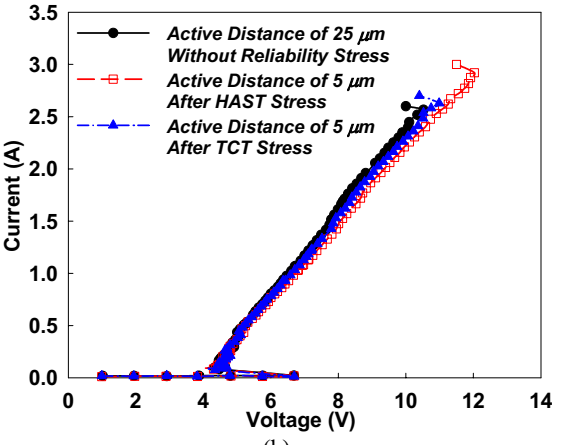
Fig. 9. Leakage currents of the (a) N-type FOD, (b) SCR, (c) P-type diode, and (d) P-type FOD with the shrunk seal-ring of only 5 μm.

3.3. TLP I-V curves

The Transmission Line Pulsing (TLP) system [8] is used to evaluate the turn-on behavior and ESD robustness of the ESD protection devices. To verify ESD robustness of NMOS devices in the different layout styles with the modified seal-ring structure, the measured TLP I-V curves are shown Figs. 10(a) and 10(b). In Figs. 10(a) and 10(b), the TLP I-V curves of the gate-grounded NMOS devices with active distances of 25 μm and 5 μm show no significant difference after reliability tests in both layout styles. From the experimental results, the device characteristics such as triggering voltage (V_{t1}), turn-on resistance (R_{on}), holding voltage (V_h), and second breakdown current (I_{t2}), are not obviously degraded after reliability tests with the reduced distance and dimension of seal-ring structure.



(a)



(b)

Fig. 10. TLP-measured I-V curves of the NMOS devices with (a) horizontal layout style and (b) vertical layout style before and after HAST and TCT stresses.

4. Conclusion

From the measured results, the device characteristics and ESD robustness of the ESD devices drawn with reduced distance and dimension of seal-ring structure show no obvious degradation after reliability tests. In addition, the active distance can be reduced from 25 μm to 5 μm, and the dimensions of the seal-ring structure can be shrunk from 10 μm to 5 μm without increasing the leakage currents of the devices after reliability stresses. The die area can be effectively reduced by such new compact seal-ring rules without causing increased reliability problems.

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