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Optimization on Layout Structures of LTPS TFTs for On-Panel ESD Protection Design

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1. Introduction

The electrostatic discharge (ESD) becomes the most critical issue on liquid crystal display (LCD) panel [1]. The ESD-generated heat cannot be immediately dissipated by the LCD panel with low thermal conductivity, and then causes the permanent damages on the panel. Some earlier studies [1]-[4] demonstrated the failure phenomena on threshold voltage, transconductance, and capacitance of thin-film transistor (TFT) after different over-voltage stresses. However, no high-current transient characteristics or ESD robustness of TFTs was discussed. In this work, three different layout structures of diode-connected n-channel TFTs (N-TFTs) fabricated by low-temperature polysilicon (LTPS) process are tested to evaluate their ESD robustness with the secondary breakdown current (It2) measured by wafer-level transmission line pulsing (TLP) system.

2. TLP Measurement Setup

The LTPS N-TFT is drawn in finger style and diode -connected configuration. The diode-connected N-TFT can be operated in forward-biased condition to discharge ESD current, when a power-rail ESD clamp circuit is built on the panel to achieve whole-panel ESD protection [5]. The channel length (L) and the channel width (W) of N-TFT are varied from 5μm to 20μm and 100μm to 500μm, respectively. The N-TFTs with the same W/L ratio of 100 are also drawn in different device dimensions to verify the impact on ESD robustness.

Fig. 1 shows the wafer-level TLP system used to simulate human body model (HBM) ESD event on N-TFT. The transmission line is initially charged by the high voltage source, and then generates a 100-ns current pulse with 10-ns rise time into the N-TFT. The abruptly changed TLP waveforms, as shown in Fig. 2, present a break point in the TLP-measured I-V curve. Therefore, the It2 of the diode-connected N-TFT, which can sustain the maximum TLP current without permanent damage, can be determined.

3. Experimental Results and Discussion

Fig. 3 shows the TLP-measured I-V curves of the diode-connected N-TFTs with different channel widths under forward TLP stress. The top view of the diode-connected N-TFT with W/L=200μm/5μm is inserted in Fig.3. The diode-connected N-TFT with longer channel width has a lower turn-on resistance, so that it can sustain higher current under forward TLP stress. The It2 and the fresh leakage currents of the diode-connected N-TFTs with different channel widths are shown in Fig. 4. The It2 of the diode-connected N-TFT is increased from 0.14A to 0.6A when the channel width is increased from 100μm to 500μm. But, increasing channel width always accompanies the increased fresh leakage current which causes extra standby power dissipation on LCD panel.

The TLP I-V curves of the diode-connected N-TFTs with different channel lengths under forward TLP stress are shown in Fig. 5. When the channel length is varied from 5μm to 20μm, the It2 is kept between 0.55A to 0.7A. The longer channel length of the N-TFT with the same channel width enlarges the device dimension to provide larger heat dissipation area under forward TLP (ESD) stress. Fig. 6 shows the It2 and the fresh leakage currents of the diode-connected N-TFTs with different channel lengths.

The TLP I-V curves of the diode-connected N-TFTs with the same W/L ratio of 100 under forward TLP stress are shown in Fig. 7. The diode-connected N-TFT with the longest channel width of 2000μm, which has the largest heat dissipation area, has the highest It2 level. Fig. 8 shows the TLP It2 and the fresh leakage currents of the diode-connected N-TFTs with the same W/L ratio of 100. The fresh leakage current is kept below 3nA. When the channel width of the diode-connected N-TFTs with the same W/L ratio is linearly increased from 500μm to 2000μm, the It2 is increased from 0.6A to 1.6A. Therefore, enlarging the channel width under the same W/L ratio of the diode-connected N-TFT can improve the ESD robustness, as well as, keep a low fresh leakage current.

4. Conclusions

The ESD robustness among different layout structures of the diode-connected LTPS N-TFTs on panel is investigated. Enlarging the channel width can improve the It2 level, but accompanies the increased fresh leakage current. However, enlarging channel length is less sensitive both on the It2 level and the fresh leakage current. The N-TFT drawn in the same W/L ratio with the increased channel width can greatly improve the It2 level due to the large heat dissipation area. Finally, the diode-connected N-TFT with W/L=2000μm/20μm can pass the 1.6-A TLP current stress (corresponding to the HBM ESD level of 2.4kV), which is suitable for on-panel ESD protection design.

Acknowledgements

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References

[1] F. R. Libsch *et al.*, "ESD: how much protection is need for AMLCDs," in *Dig. Tech. Papers*, *SID*, *1994*, pp. 255–258.
[2] S. Uchikoga *et al*., "Deterioration mechanism of α-Si:H TFT caused by ESD," in *Proc*. *AM-LCD*, *1994*, pp. 128–131.
[3] N. T. Golo *et al.*, "Transmission line model testing of top-gate amorphous silicon thin film transistors," in *Proc*. *IRPS*, *2000*, pp. 289–294.
[4] S.-C. Lee *et al.*, "Electrostatic discharge effects on polysilicon TFTs for AMLCD," in *Dig. Tech. Papers*, *SID*, *2002*, pp. 212–215.
[5] M.-D. Ker *et al.*, "Successful electrostatic discharge protection design for LTPS circuits integrated on panel," in *Dig. Tech. Papers*, *SID*, *2003*, pp. 1400–1403.

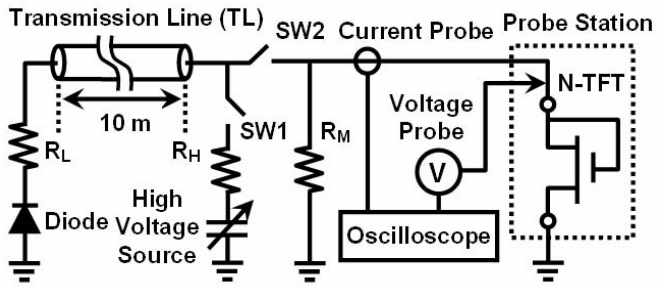

Fig. 1. The configuration of the wafer-level TLP system used to measure the TLP I-V curves of the LTPS N-TFT.

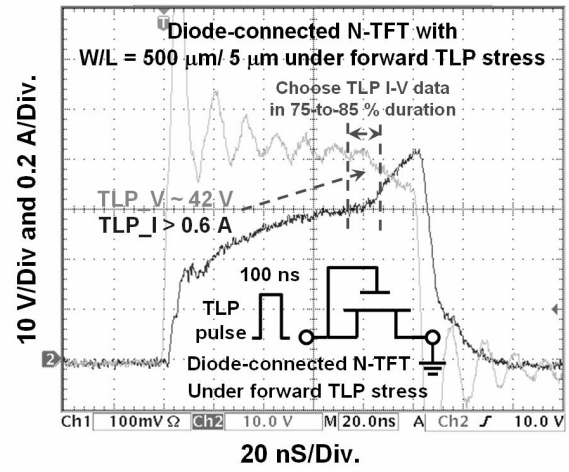

Fig. 2. The I-V waveforms of the diode-connected N-TFT with W/L = 500μm/5μm after over 0.6-A forward TLP-current stress.

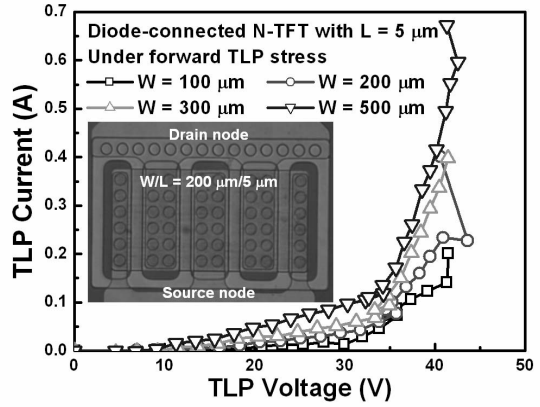

Fig. 3. The TLP I-V curves of the diode-connected N-TFTs with different channel widths under forward TLP stress.

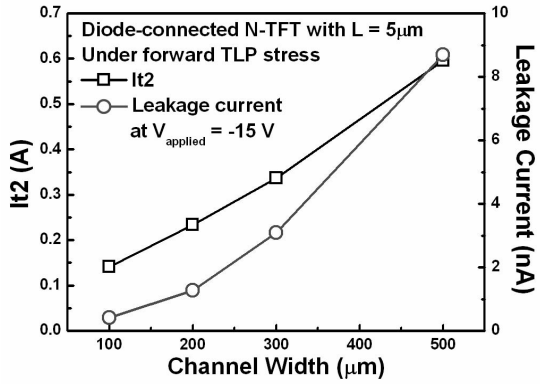

Fig. 4. The dependence of the It2 and the fresh leakage currents on the channel widths of the diode-connected N-TFTs.

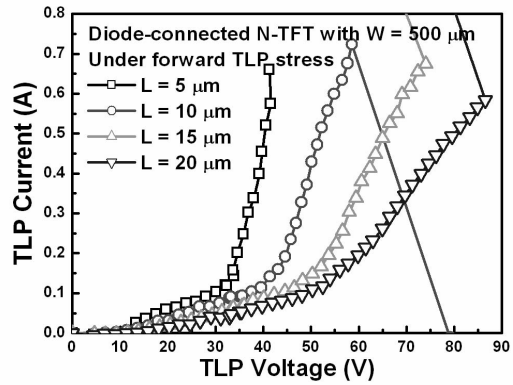

Fig. 5. The TLP I-V curves of the diode-connected N-TFTs with different channel lengths under forward TLP stress.

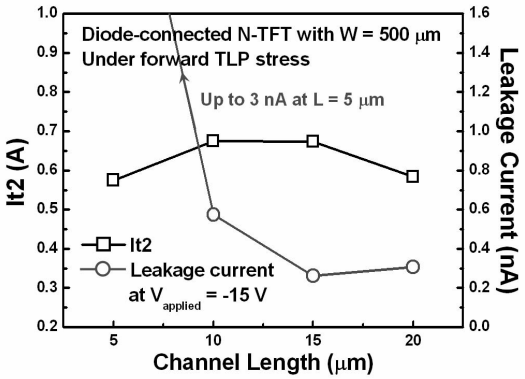

Fig. 6. The dependence of the It2 and the fresh leakage currents on the channel lengths of the diode-connected N-TFTs.

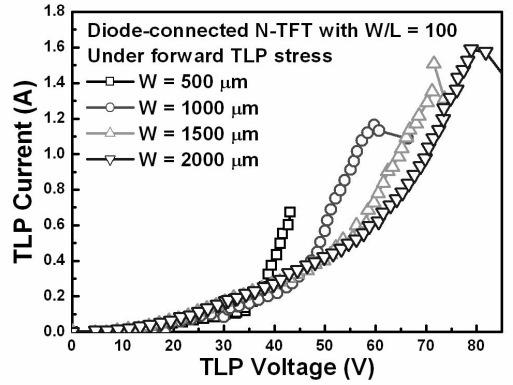

Fig. 7. The TLP I-V curves of the diode-connected N-TFTs with the same W/L ratio of 100 under forward TLP stress.

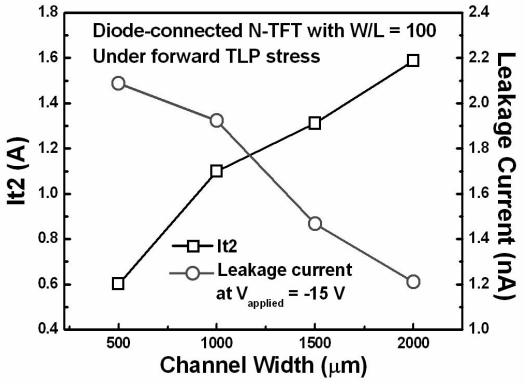

Fig. 8. The dependence of the It2 and the fresh leakage currents on channel width of the diode-connected N-TFTs with the same W/L ratio of 100.