A 70nW, 0.3V Temperature Compensation Voltage Reference Consisting of Subthreshold MOSFETs in 65nm CMOS Technology

Ting-Chou Lu[1, 2], Ming-Dou Ker[2], and Hsiao-Wen Zan[3]

[1] Information and Communications Research Laboratories, Industrial Technology Research Institute, Hsinchu, Taiwan.
[2] Department of Electronics Engineering & Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.
[3] Department of Photonics & Institute of Electro-Optical Engineering, National Chiao Tung University, Taiwan

***Abstract* -- Being operated with 0.3V supply voltage in a standard 65nm CMOS process, a new CMOS temperature compensated voltage reference circuit is proposed with subthreshold transistors and native nMOS. The reference drain current provided by the gate voltage of a subthreshold nMOS output transistor is nearly independent of temperature due to the existence of mutual compensation of mobility and threshold voltage variation. The new proposed temperature compensated voltage reference circuit functions well with the output voltage V_{REF} of 168 mV at room temperature as no extra laser trimming is needed after fabrication. The total power consumption is about 70nW. With the VDD power supply of 0.3V, the temperature coefficient (TC) of voltage reference circuit is 105 ppm/°C as temperature varies from -20°C to 100°C. The chip size of the fabricated bandgap reference circuit is 0.0053mm^2.**

***Index Terms*—Bandgap Reference Circuit (BGR), Subthreshold Region, Native nMOS**

I. INTRODUCTION

Nowadays, ultra-low voltage (ULV) circuits have attracted considerable interest for applications to the wearable biomedical devices, smart sensor network and passive Radio-frequency identification (RFID) due to their excellent energy optimization [1]. MOSFETs operated in the subthreshold region are becoming increasingly popular in the low voltage and low power circuit designs because of the low gate to source voltage (VGS) which is lower than the threshold voltage (V_{th}) and its low bias current [2]. Therefore, subthreshold MOSFETs not only reduce power dissipation but also offer efficient use of the available headroom of the low voltage circuit. Furthermore, native transistors with approaching zero threshold voltage are the other familiar solution for low voltage application [3]. Recently, the extra mask and process of native transistors are becoming generally purposed process; hence native transistors had been widely applied in realistic product.

A voltage reference is one of the important key blocks for analog, digital, as well as mixed-signal circuit systems in micro-electronics. It generates a constant reference voltage for various fundamental components such as operational amplifiers, comparators, and AD/DA converters, and so on [4], [5]. The bandgap reference (BGR) circuit is the key design to generate a stable DC voltage with low sensitivity to Process, supply Voltage and Temperature (PVT) variations. The most common bandgap reference circuit for on-chip integration is implemented in standard CMOS technology exploiting parasitic vertical bipolar junction transistors (BJTs) or diodes. Conventional BGR circuits with BJTs generate a nearly temperature independent reference, of about 1.2 V [6], [7]. Therefore, a higher supply voltage which might not meet the low-voltage constraints for low-power applications is necessary. Recently, modified BJT BGR circuits generate a nearly temperature independent reference about 0.75V had been purposed by using switching capacitors [8]. However, V_{BE} which is 0.7V is the limitation of BJT eventually. In [9]-[10], subthreshold region voltage reference circuits are in replace of BJT bandgap circuits to become popular in low power design because of its ultra-low operating voltage and low power dissipation. A subthreshold voltage reference circuit with 0.45V supply voltage and 2.6 nW had been proposed for low power application [11].

A new CMOS temperature compensation voltage reference circuits operated with 0.3V supply voltage in a standard 65nm CMOS process is equipped with subthreshold transistors and native nMOS and introduced in this paper. Being verified with the output voltage V_{REF} of 168 mV at room temperature, the new proposed temperature compensated voltage reference circuit works without laser trimming after fabrication.

II. OPERATING PRINCIPLE

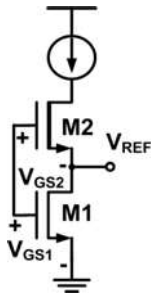

FIGURE 1. SCHEME OF PRINCIPLE OF A PROPOSED VOLTAGE REFERENCE.

The voltage reference in this work can be simply expressed as a current source and two diode connected transistors which act as active load shown in Fig. 1. Similar structures had been used in prior art [8]-[9]. One current source and one diode connected transistor operated in saturated region or subthreshold region. The NMOS provides a temperature

978-1-4673-9498-7/16/$31.00 ©2016 IEEE

compensation reference voltage (V_{REF}). The reference voltage V_{REF} in this work can be modified as following.

$$V_{REF} = V_{GS1} - V_{GS2} \tag{1}$$

Where transistor M1 is operated in subthreshold region, and M2 is the native NMOS. Native NMOS is not implanted in P-well but directly in P-substrate. The characteristic of native NMOS is intermediate between enhancement and depletion modes and the threshold voltage is nearly zero.

The function of the subthreshold drain current of a MOSFET is an exponential function of the gate-source voltage and the drain-source voltage, and I-V characteristics of nMOS operated in subthreshold region is given by

$$I_D = \mu S V_T^2 \exp(\frac{V_{GS} - V_{th}}{\eta V_T})[1 - \exp(-\frac{V_{DS}}{V_T})] \tag{2}$$

Where μ is the electron mobility, S = COX(W/L)(η-1) (COX is the gate oxide capacitance per unit area, (W/L) is the transistor aspect ratio, and η is the subthreshold slope factor), $V_T = k_B T/q$ is the thermal voltage (k_B is the Boltzmann constant, q is the elementary charge and T is the absolute temperature), V_{th} is the MOSFET threshold voltage, V_{GS} and V_{DS} are the gate-to-source and the drain-to-source voltages, respectively. As $V_{DS} \geqq 4V_T \simeq 0.1V$, the current I_D is almost independent of V_{DS}, and V_{GS} can be approximated by

$$V_{GS} = V_{th} + \eta V_T \ln(\frac{I_D}{\mu S V_T^2}) \tag{3}$$

Where V_T is proportioned to absolute temperature (PTAT) and V_{th} which decreases with absolute temperature linearly is shown as [13]

$$V_{th}(T) = V_{th}(T_0) + \alpha(T - T_0) \tag{4}$$

Where T_0 is the reference temperature which is 300˚K and α is a negative value.

The current operated in saturation region is shown as following

$$I_D = \frac{1}{2} S_2 \mu_2 (V_{GS2} - V_{th2})^2 \tag{5}$$

Where V_{th2} is threshold voltage of native nMOS transistor, and its value is approach to zero. Therefore, the output voltage can be rewritten as

$$V_{REF} = V_{GS1} - V_{GS2} = V_{th1} + \eta V_T \ln(\frac{I_D}{\mu_1 S_1 V_T^2}) - V_{th2} - \sqrt{\frac{2I_D}{S_2 \mu_2}} \tag{6}$$

The temperature coefficient of output voltage can be formulated as

$$\frac{dV_{REF}}{dT} = (\alpha_1 - \alpha_2) + \frac{k}{q}\eta \ln(\frac{I_D(T)}{\mu_1 S_1 V_T^2}) + \frac{kT}{q}\eta \frac{\partial}{\partial T}\ln(\frac{I_D(T)}{\mu_1 S_1 V_T^2}) - \frac{1}{2}(\frac{2I_D}{S_2\mu_2})^{-\frac{1}{2}} \frac{\partial}{\partial T}(\frac{2I_D(T)}{S_2\mu_2}) \tag{7}$$

A zero TC can be achieved to have the temperature compensation of output voltage. The following equation has to be satisfied

$$\frac{dV_{REF}}{dT} = 0 \tag{8}$$

Therefore, finding out the dependence between bias current and temperature is essential to clarify the temperature compensated mechanism.

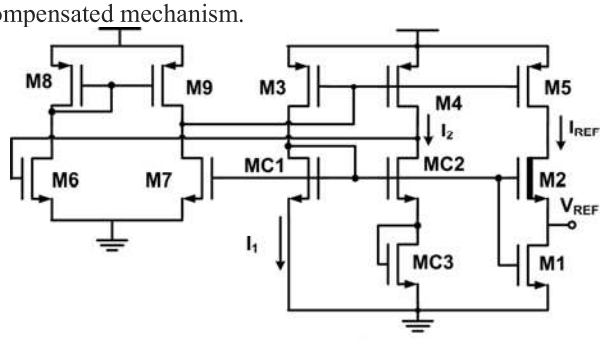

FIGURE 2. SCHEME OF PROPOSED TEMPERATURE COMPENSATED VOLTAGE REFERENCE

III. PROPOSED CURRENT REFERENCE CIRCUIT

The architecture of the proposed voltage reference is illustrated in Fig. 2. The self-biased current source has no resistors and all MOSFETs work in the subthreshold region. It generates the current to be injected in the active load transistors due to the low power characteristics, such as high mobility and uniform amorphous structure. It is to provide a stable current which compensates temperature effects on V_{REF}, and voltage variations can be reduced the supply by OP Amp and bypass capacitors. The current I_D in (8) can be obtained by taking into account a linear combination of nMOS voltages in the sub-threshold region. Among the possible solutions for the current reference we chose a self-biased configuration where only three subthreshold operated NMOSs perform such combination. By using the virtual short characteristic of OP Amp, the DC equation of current source can be explained as

$$V_{GSc1} = V_{GSc2} + V_{GSc3} \tag{9}$$

Substitute V_{GS} with (3), (9) can be rewritten as follows

$$V_{thc1} + \eta V_T \ln(\frac{I_{D1}}{\mu_{c1} S_{c1} V_T^2}) = V_{thc2} + \eta V_T \ln(\frac{I_{D2}}{\mu_{c2} S_{c2} V_T^2}) + V_{th} + \eta V_T \ln(\frac{I_{D2}}{\mu_{c3} S_{c3} V_T^2}) \tag{10}$$

Let $V_{th} = V_{thc2} + V_{thc3} - V_{thc1}$ and assume the electron mobilities μ are almost the same ($\mu_{c1} = \mu_{c2} = \mu_{c3}$). The current ratio can be decided by PMOS aspect ratio ($I_2/I_1 = (W_4/L_4)/(W3/L_3) = a$). We can express the current I_1 as

$$I_1 = A\mu V_T^2 \exp(-\frac{\Delta V_{th}}{B V_T}) \tag{11}$$

Where $A = (S_2 S_3 / a^2 S_1)$, and $B = (\eta_2 + \eta_3 - \eta_1)$. The generated current I_1 is mirrored to the active load by the current mirror consisted of M3, M4, and M5. Assume the ratio of mirror

($I_{REF}/I_1 = (W5/L5)/(W3/L3)$)is β, therefore, (6) can be rewritten as

$$V_{REF} = V_{GS1} - V_{GS2} = V_{th1} - V_{th2} + \eta V_T \ln(\frac{A\beta}{\mu S_1 V_T^2}) - \frac{\Delta V_{th}}{BV_T} - \sqrt{\frac{2AV_T^2}{S_2}\exp(-\frac{\Delta V_{th}}{BV_T})} \quad (12)$$

The Taylor series of nature logarithm (ln) can be express as

$$\ln x = \sum_{n=1}^{\infty} \frac{(-1)^{n+1}}{n}(x-1)^n = (x-1) - \frac{1}{2}(x-1)^2 + \frac{1}{3}(x-1)^3 ..... \quad (13)$$

As the order of current is less than 10^{-8} (about 10nA), the square root term of (12) is about 10^{-4}. It affects the Taylor series is lower than 10th terms; therefore, the square root term in (12) can be neglected under Nano-Amp scale. Reference voltage can be approach as

$$V_{REF} = V_{GS1} - V_{GS2} = V_{th1} - V_{th2} - \frac{\Delta V_{th}}{BV_T} + \eta V_T \ln(\frac{A\beta}{\mu S_1 V_T^2}) \quad (14)$$

We can find that the temperature dependence of voltage reference is V_{th} and V_T. The temperature compensation can be design by setting $\delta V_{REF}/\delta T=0$, and find out the fitting ratio of (W1/L1) and (W2/L2). The gate of M1 and M2 are also connected to the gate of MC1 and MC2, its purpose is to keep M1 and M2 always on by the diode connected transistor MC3.

A differential operational amplifier with active-loaded MOS pair is designed to be used in the reference core. It employs a differential input pair, consisting of transistors M1 and M2 used low threshold voltage devices and operated in weak inversion, so sufficient headroom remains available for ultra-low supply voltage. The amplifier is self-biased from the supply and consumes 110nA of current, providing a DC gain of 20dB. It provides higher PSRR and its characteristic of virtual short for circuit design.

The stability of with variations mainly depends on the current generator's insensitivity to supply voltage variations. This characteristic is achieved by the self-biased current source architecture. The common improvement of the reference voltage line sensitivity and the power supply rejection ratio (PSRR) can be obtained by using an additional current mirror, stacking transistors, and transimpedance differential OP Amp (PIA)[6], [9]. However, the addition current mirror would increase the power consumption and stacking transistors isn't accommodated for low voltage design.

The feedback mechanism of OP Amp is a suitable way to improve PSRR. Process variations are generally discriminated in Die to Die (D2D or inter-die) variations and variations With-in Die (WID or intra-die) [13]. D2D variations, instead, influence the absolute accuracy of transistor parameters and their effects are not compensated in the proposed configuration. WID variations causes mismatch between transistors of the same chip and influences the relative accuracy of transistor parameters. Well-designed layout techniques and large channel length of transistors, are practical methods presently.

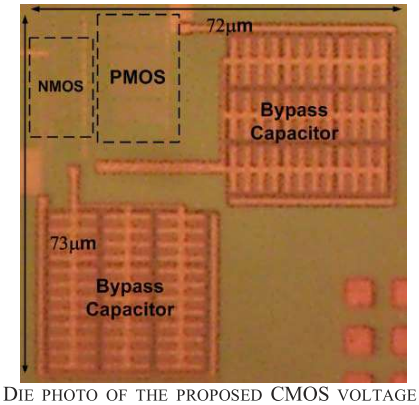

FIGURE 3. DIE PHOTO OF THE PROPOSED CMOS VOLTAGE REFERENCE CIRCUIT

IV. EXPERIMENT RESULT

The new proposed voltage reference circuit has been fabricated in TSMC 65nm General Purpose (GP) CMOS technology. The chip photo of the fabricated voltage reference circuit is shown in Fig. 3. The chip size of the fabricated bandgap reference circuit is 0.0053mm^2 (72 × 73 μm^2). The threshold voltage of Low V_T (LVT) NMOS and PMOS are 0.246V and -0.257V separately. The threshold voltage of native NMOS is -0.045V, and the Table I shows the size of transistors.

The power supply voltage V_{DD} is set to 0.3 V, and the total operating current is 193 nA. The measured results of the output voltage V_{REF} are shown in Fig. 4, the measured temperature coefficient of the fabricated bandgap reference circuit is around 105 ppm/°C (without laser trimming after fabrication) from -20 to 100 ˚C, whereas the output voltage (V_{REF}) is kept at 168 mV. The linear regulation shown in Fig. 5 is 4.8% from V_{DD} 0.3V to 1V. The linear regulation is higher than proper value because the transistors which are LVT MOSFETs are operated in saturation region instead of subthreshold region as supply voltage is higher than 0.65V. Besides, the dimensions of transistors are designed reasonable for 65nm GP CMOS process instead of large channel length which is used for reducing process variation and improving PSRR performance. The total power consumption of full circuit at V_{DD} =0.3V is about 70nW. Table II summarizes the characteristics of our device in comparison with other low-power CMOS voltage references.

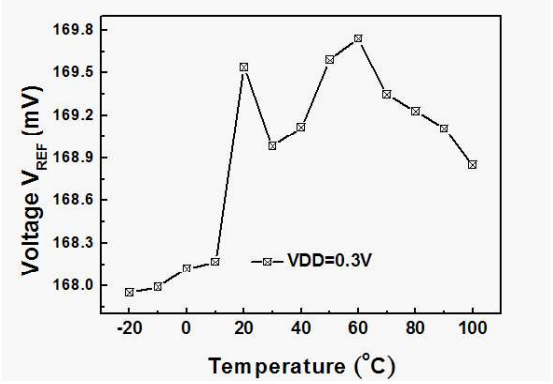

FIGURE 4. MEASURED OUTPUT VOLTAGE AS A FUNCTION OF TEMPERATURE. SUPPLY VOLTAGE SETS TO 0.3 V. TC IS 105 PPM/˚C.

TABLE1. COMPARISON WITH LOW VOLTAGE TEMPERATURE COMPENSATED CIRCUIT

	[6]	[8]	[9]	[10]	[11]	This work
Supply voltage (V)	1.4~3	0.75~1.4	1.4~3	1.2	0.45~2	0.3
Technology (nm)	600	130	350	120	180	65
Multi-Phase	1	1	1	1	1	8
Temperature Range (˚C)	0~100	-20~85	-20~80	-25~125	0~125	-20~100
VREF(mV)	309	184	745	295	265	168
Power (mW)	29.1 at 3V	0.17	0.3 at 1.4V	4.3m	3.2n	70n
TC(ppm/˚C)	36.9	40	7	109	1500	142
Linear regulation	800ppm/V	50ppm/V	20ppm/V	N.A.	0.44%	4.8%
Area (mm^2)	0.23	0.07	0.055	0.23	0.043	0.0053

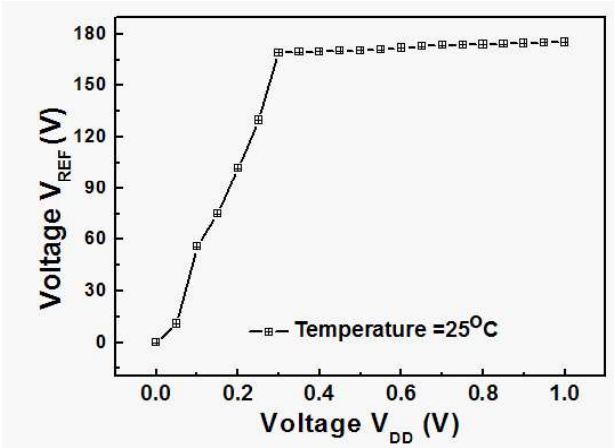

FIGURE. 5.MEASURED OUTPUT VOLTAGE VREF AT ROOM TEMPERATURE (T=25˚C) AS A FUNCTION OF POWER SUPPLY. LINE REGULATION WAS 4.8% FOR SUPPLY VOLTAGES 0.3-1.0V.

IV. CONCLUSION

In this paper, a new CMOS temperature compensated voltage reference circuits has been proposed with subthreshold transistors and native nMOS which is successfully operated with 0.3V supply in a standard 65 nm CMOS process. Without additional laser trimming after fabrication, the new proposed temperature compensated voltage reference circuit has been verified with the output voltage V_{REF} of 168 mV at room temperature. This voltage applied to the gate of a subthreshold nMOS output transistor provides a reference drain current nearly independent of temperature by mutual compensation of mobility and threshold voltage variations. The circuit topology allows compensation of threshold voltage variation due to process parameters. The TC of voltage reference circuit with temperature compensation output voltage is 105 ppm/˚C under V_{DD} power supply of 0.3 V when the temperature varies from -20˚C to 100˚C. The total power consumption is about 70nW. The linear regulation is 4.8% from V_{DD} 0.3V to 1V.

ACKNOWLEDGEMENT

The authors would like to thank Mr. Yuan-Hua Chu, Mr. Jen-Chieh Liu and Mr. Yu Li of Industrial Technology Research Institute (ITRI) for their valuable technical discussion and suggestion.

REFERENCES

[1] A. Wang, B. H. Clhoun, and A. P. Chandracasan, *Sub-threshold design for ultra low-power systems.* new york: Springer, 2006.
[2] A. P. Chandrakasan, D. C. Daly, J. Kwong, and Y. K. Ramadass, "Next generation micro-power systems," in *Proc. IEEE Symp. VLSI Circuits*, 2008, pp. 2–5.
[3] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui, "A CMOS bandgap reference circuit with sub-1-V operation," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 670-674, May 1999.
[4] M. McCorquodale, J. O'Day, S.Pernia, G. Carichner, S. Kubba, and R. Brown, "A monolithic and self-referenced RF LC clock generator compliant with USB 2.0," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 385-399, Feb. 2007.
[5] T. C. Lu, M. D. Ker, and H. W. Zan et al., "Design of bandgap voltage reference circuit with all TFT devices on glass substrate in a 3-μm LTPS process," in *Proc. IEEE Custom Integrated Circuit Conference*, 2008, pp. 471-474.
[6] K. N. Leung and P. K. T. Mok, "A sub-1-V 15 ppm/˚ C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE J. Solid-State Circuits*, vol. 37, no. 4, pp. 526–530, Apr. 2002.
[7] K. N. Leung and P. K. T. Mok, "A CMOS voltage reference based on weighted △Vth for CMOS low-dropout linear regulators," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 146–150, Jan. 2003.
[8] V. Ivanov, R. Brederlow, and J. Gerber, "An ultra-low power bandgap operational at supply from 0.75 V," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp.1515-1523, Jul. 2012.
[9] K. Ueno, T. Hirose, T. Asai, and Y. Amemiya, "A 300 nW, 15ppm/˚C, 20 ppm/V CMOS voltage reference circuit consisting of subthreshold MOSFETs," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp.2047-2054, Jul. 2009.
[10] G. Giustolisi, G. Palumbo, M. Criscione, and F. Cutri, "A low-voltage low-power voltage reference based on subthreshold MOSFETs," *IEEE J. Solid-State Circuits*, vol. 38, no.1, pp. 151-154, Jan. 2003.
[11] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6 nW, 0.45 V temperature-compensated subthreshold CMOS voltage reference," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp.465-474, Feb. 2011.
[12] I. M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *IEEE Trans. Circuits Syst. I*, vol. 48, no. 7, pp. 876–884, Jul. 2001.
[13] B. Razavi, *Design of Analog CMOS Integrated Circuits.* New York: McGraw Hill, 2001.