# Methods to Improve Machine-Model ESD Robustness of NMOS Devices in Fully-Salicided CMOS Technology

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## ABSTRACT

NMOS with dummy-gate structure is proposed to significantly improve machine-model (MM) electrostatic discharge (ESD) robustness in a fully-salicided CMOS technology. By using this structure, the ESD current is discharged far away from the salicided surface channel of NMOS, therefore NMOS can sustain a much higher ESD level, especially under the machine-model ESD stress.

## INTRODUCTION

In deep-sub-micron fully-salicided CMOS technology, the MOSFETs are fabricated with salicidation process to improve circuit performance. Salicidation process reduces sheet resistance of drain/source side of MOSFETs, but its ESD robustness is dramatically degraded. ESD robustness of salicided NMOS is degraded to 30% of that of unsalicided NMOS [1]. This is primarily due to current crowding within the salicided layer and non-uniform turn-on issue on ESD protection device. To improve ESD robustness, some CMOS processes provide one extra salicide blocking (SAB) mask to modify the ESD protection NMOS of I/O circuits without the salicided structure. However, the salicide blocking (SAB) method is expensive because it needs an extra mask and more process procedures.

In the past, most of ESD design efforts were focused to improve HBM ESD robustness of IC products. The ESD voltage ratio between the HBM and MM ESD robustness of CMOS IC products were around ~10 in the submicron (1.0 ~ 0.5 μm) CMOS processes [2]. With a high HBM ESD robustness, the IC products also had a high enough MM ESD level. However, the MM ESD robustness of IC products has been found to degrade much worse than its HBM ESD robustness in the deep-sub-micron fully-salicided CMOS processes [3].

The actual ESD current waveforms flowing through the ggNMOS with a device dimension of W/L = 300 μm/0.5 μm under 4-kV HBM and 400-V MM ESD stresses are measured and shown in Figs. 1 and 2, respectively. The current peak of 4-kV HBM ESD stress in Fig. 1 is 3.54 A, whereas that of 400-V MM ESD stress in Fig. 2 is as high as 4.94 A. As comparing these two ESD current waveforms, the MM ESD stress has a much higher ESD current peak within a shorter current pulse width. This implies that the MM ESD events generate more heat in a shorter time period to burn out the device, and therefore cause a much lower ESD robustness. How to effectively improve MM ESD robustness of IC products has become a challenge in the deep-sub-micron fully-salicided CMOS processes. In this work, NMOS with dummy-gate structure is proposed to significantly improve machine-model (MM) electrostatic discharge (ESD) robustness in a fully-salicided CMOS technology [4].

## DEVICE STRUCTURE

In deep-sub-micron CMOS technology, the NMOS is fabricated with salicidation process to improve circuit performance as shown in Fig. 3. However, due to current crowding issue, salicidation process degrades ESD performance of ggNMOS dramatically. To improve ESD robustness, some CMOS processes provide one extra salicide blocking (SAB) mask to modify the ESD protection NMOS of I/O circuits without the salicided structure. In the prior art, the FOX NMOS is used as salicided blocking layer to improve ESD robustness without an extra mask as shown in Fig. 4. To significantly improve ESD robustness of ESD protection NMOS of I/O circuits, dummy-gate structure NMOS transistor with N-well resistors, is proposed as shown in Fig. 5. In Fig. 4, the FOX structure blocks the salicidation region of drain side of NMOS transistor, and the N-well covers the drain side to increase the ballast resistance. In Fig. 5, the dummy-gate structure blocks the salicidation region of drain side of NMOS transistor, and the N-well covers the drain side to increase the ballast resistance.

When a positive ESD voltage is applied to the pad with the VSS relatively grounded. The salicied drain region of NMOS is blocked by the FOX or dummy-gate structure, therefore the ESD current is discharged far away from the weakest salicidation layer of the NMOS. On the other hand, the drain region of NMOS, which is covered by the N-well structure, has a lager drain ballast resistance, therefore the multiple fingers of NMOS can be uniformly triggered on. So, the ESD robustness of NMOS can be effectively improved.

## RESULTS AND DISCUSSION

Fully-salicided NMOS, FOX NMOS, and the proposed dummy-gate NMOS, were drawn with the same device dimension (W/L = 240 μm/0.25 μm) in a 0.25-μm fully-salicided CMOS process without using any optional process step and extra mask. To simplify compare the ESD robustness of fully-salicided NMOS, FOX NMOS, and dummy-gate NMOS, the layout spacing of the drain contact to poly gates (LDG, which is indicated in Figs. 3, 4, and 5) is fixed at 5 μm in the experimental test chips. The fabricated devices are measured by the *ZapMaster* ESD simulator to investigate HBM and MM ESD robustness. The HBM and MM ESD levels of these three kinds of ggNMOS are compared in Table I. The HBM ESD robustness of these three kinds of ggNMOS is all over 3 kV, but MM ESD level of fully-salicided ggNMOS is only 150 V. However, MM ESD levels of the FOX NMOS and dummy-gate NMOS transistors are improved to 231 V and 394 V, respectively. Under the same layout area of the ggNMOS, the MM ESD level can be improved 162 % by using the proposed dummy-gate structure. HBM/MM ESD ratio of the fully-salicided ggNMOS has a value of 23.5. However, HBM/MM ESD ratio of ggNMOS can be reduced to 8.4 by the dummy-gate structure.

In order to clarify the failure current paths and failure locations of these NMOS devices, some failure analysis on these zapped devices has been observed by the optical microscopy and scanning electron microscopy (SEM). SEM pictures of fully-salicided NMOS and the dummy-gate NMOS after MM ESD stress are shown in Figs. 6 and 7, respectively. The failure regions of fully-salicided NMOS only located within a few gate regions, which is due to current crowding within the weak salicided surface channel. However, the failure regions of dummy-gate NMOS uniformly located among all the contact regions of drain side. So, MM ESD robustness of transistor with the proposed dummy-gate structure is better than that of fully-salicided structure.

## CONCLUSIONS

NMOS with dummy-gate structure used to significantly improve

which is process compatible to general fully-salicided CMOS processes without any additional mask, is very cost-efficient for application in the IC products to improve their MM ESD robustness.

## REFERENCES


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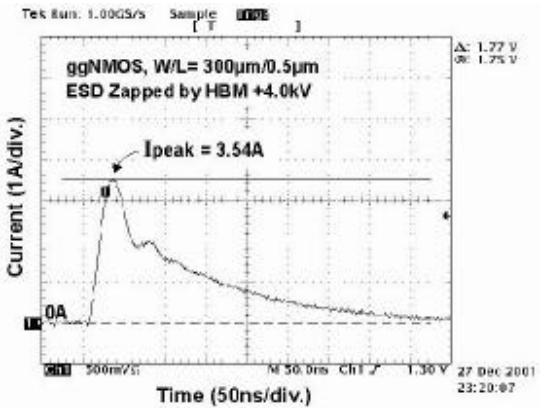


Fig. 1. The measured ESD current discharging waveform through the ggNMOS, which is zapped by 4-kV HBM ESD voltage.

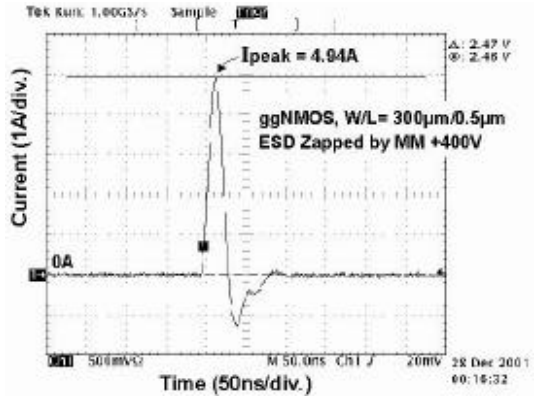


Fig. 2. The measured ESD current discharging waveform through the ggNMOS, which is zapped by 400-V MM ESD voltage.

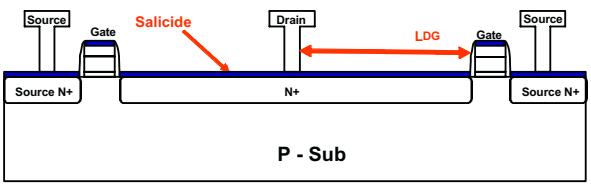


Fig. 3. Cross-sectional view of fully-salicided NMOS transistor.

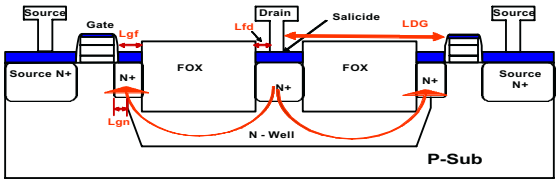


Fig. 4. Cross-sectional view of FOX NMOS transistor with N-well ballast resistor.

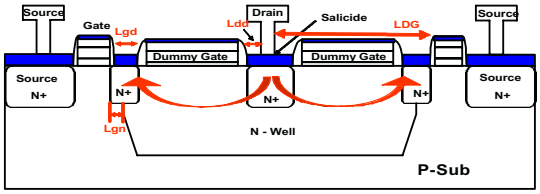


Fig. 5. Cross-sectional view of dummy-gate NMOS transistor with N-well ballast resistor.

TABLE I
HBM, MM ESD LEVELS, AND HBM/MM RATIO OF THREE KINDS OF GGNMOS TRANSISTORS

| | HBM (kV) | MM (V) | HBM/MM Ratio |
|---|---|---|---|
| Fully-salicided NMOS | 3.53 | 150 | 23.5 |
| FOX NMOS | 3.63 | 231 | 15.7 |
| Dummy-gate NMOS | 3.30 | 394 | 8.4 |

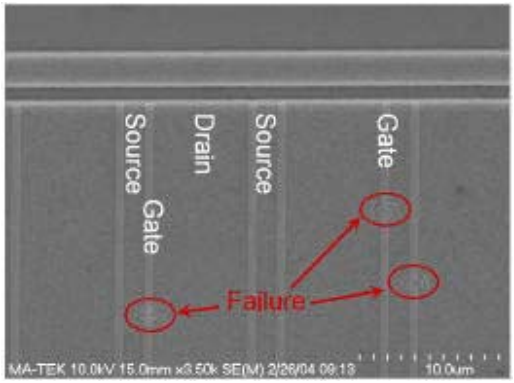


Fig. 6. SEM picture of fully-salicided NMOS transistor after 200-V MM ESD zapping.

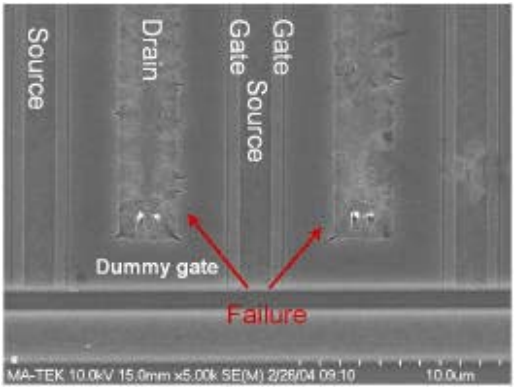


Fig. 7. SEM picture of dummy-gate NMOS transistor after 400-V MM ESD zapping.