Self-Substrate-Triggered Technique to Enhance Turn-on Uniformity of Multi-Finger ESD Protection Devices

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Abstract – A novel self-substrate-triggered (SST) technique is proposed to solve the non-uniform turn-on issue of the multi-finger GGNMOS for ESD protection. The first turned-on center finger is used to trigger on all fingers in the GGNMOS structure with self-substrate-triggered technique. So, the turn-on uniformity and ESD robustness of GGNMOS can be greatly improved by the new proposed self-substrate-triggered technique.

INTRODUCTION

With the process evolution, the device size has been continually scaled down with salicided diffusion to improve the operating speed of CMOS ICs. However, the electrostatic discharge (ESD) robustness of devices in the advanced CMOS technologies becomes weaker, therefore on-chip ESD protection devices must be added into the chips [1]. The typical ESD levels of general commercial IC products are 2 kV in human-body-model (HBM) ESD test and 200 V in machine-model (MM) ESD test. To achieve the desired ESD robustness in CMOS ICs, on-chip ESD protection devices were often designed with large device dimensions, which were traditionally drawn with the multi-finger layout style to reduce the total occupied silicon area. In the multi-finger gate-grounded NMOS (GGNMOS) surrounding by P+ guard ring, the parasitic npn BJT of center-finger NMOS with higher base resistance is always triggered on faster than other fingers under ESD stress [2]. As long as the center-finger NMOS is triggered on, the ESD overstress voltage is clamped to its snapback holding voltage. Therefore, the ESD current will be only discharged through some local region to cause the non-uniform turn-on phenomenon [2]. In this work, a novel self-substrate-triggered technique is proposed to improve turn-on uniformity of GGNMOS and to significantly increase its ESD robustness.

SELF-SUBSTRATE-TRIGGERED GGNMOS

Fig. 1 shows the equivalent circuit of self-substrate-triggered GGNMOS (SST_GGNMOS). During ESD stress, the initial ESD current will flow through the first triggered-on center finger to the base (substrate) terminals of all other parasitic BJTs in the multi-finger NMOS structure. Thus, all fingers of SST_GGNMOS can be turned on more efficiently and uniformly to discharge ESD current due to the substrate-triggered effect [2]. Figs. 2(a) and 2(b) show the layout diagram and the cross-sectional view of this new design, respectively. No extra masks or external triggering circuits are needed. So, the layout area of this SST_GGNMOS is kept almost the same as that of traditional GGNMOS.

EXPERIMENTAL RESULTS

The novel SST_GGNMOS has been realized in a standard 0.13-μm CMOS process with gate-oxide thickness of 25Å. To guarantee that the center-finger device can be turned on first to trigger on the other fingers, the channel length (Lcf) of the center-finger NMOS is drawn with the minimum rule of 0.13 μm, whereas those of the other fingers are drawn with 0.18 μm in the SST_GGNMOS structure. The traditional multi-finger GGNMOS with all channel length of 0.18 μm is also fabricated in the same chip for comparison. The finger widths of these two devices are 30μm, and the maximum finger number is as many as 20. The automatic transmission line pulsing (ATLP) system, the ESD simulator, and the Emission Microscope (EMMI) are used to investigate the efficiency of the new proposed SST technique.

Figs. 3 and 4 show the ATLP-measured I-V curves and the corresponding leakage currents of the traditional GGNMOS and the new proposed SST_GGNMOS under different channel widths, respectively. The dependence of secondary breakdown current (It2) on the channel width of traditional GGNMOS and the new proposed SST_GGNMOS is compared in Fig. 5. The It2 per micron of traditional GGNMOS decreases from 7.4mA/μm to 5.8mA/μm, when the channel width (finger number) increases from 240um (8) to 480μm (16). Due to the non-uniform turn-on effect, the It2 per micron of the traditional GGNMOS cannot be kept at the same level with the increase of channel width or finger number. On the contrary, the It2 per micron of SST_GGNMOS are all higher than 7.4mA/μm, when the channel width (finger number) increases from 360um (12) to 600μm (20).

The relationship between the HBM ESD levels and their channel widths of traditional GGNMOS and the proposed SST_GGNMOS has been also investigated in Fig. 6. The devices are tested under the positive-to-VSS ESD stress. In Fig. 6, under the same device dimensions, the HBM ESD levels of SST_GGNMOS are apparently higher than those of GGNMOS. While the channel width is increased, HBM ESD level of GGNMOS is only increased slightly. However, the HBM ESD level of self-substrate-triggered GGNMOS can be linearly increased with the increase of the channel width.

To verify turn-on uniformity of SST_GGNMOS, the continuous current pulses are applied to the drain of SST_GGNMOS with the channel width of 600μm, i.e. the finger number of 20. EMMI is used to observe the locations of hot spots, where the current flows. The hot spots are uniformly distributed among all fingers of SST_GGNMOS, as shown in Fig. 7 (with color in light bule). The self-substrate-triggered technique can indeed improve turn-on uniformity among all multiple fingers of ESD protection NMOS to increase ESD robustness significantly.

CONCLUSION

A novel self-substrate-triggered technique has been proposed to improve the turn-on uniformity of multi-finger GGNMOS, which has been successfully verified in a standard 0.13-μm CMOS process. From the experimental results, HBM ESD level and It2 per micron of SST_GGNMOS are both higher than those of traditional GGNMOS. The EMMI photograph has also confirmed that all fingers of the SST_GGNMOS can be uniformly turned on under ESD stresses. The proposed SST_GGNMOS is more suitable for applications in nano-scale CMOS technology as the efficient ESD protection devices.

REFERENCES

[1] S. Voldman, *ESD Physics and Devices*, New York: Wiley, 2004.
[2] T.-Y. Chen and M.-D. Ker, "Investigation of the gate-driven effect and substrate-triggered effect on ESD robustness of CMOS devices," *IEEE Trans. on Device and Material Reliability*, pp. 190-203, 2001.

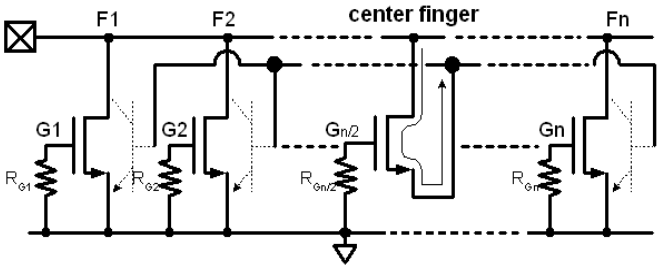
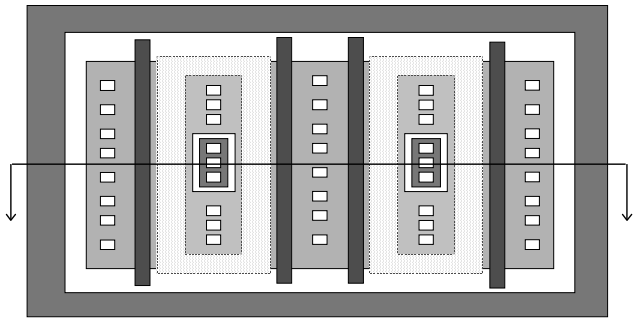
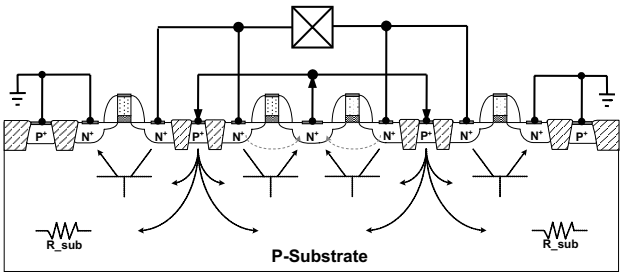


Fig. 1 The equivalent circuit of self-substrate-triggered GGNMOS (SST_GGNMOS).



(a)



(b)

Fig. 2 (a) The layout diagram, and (b) the cross-sectional view, of SST_GGNMOS. The P+ diffusions inserted to the drain of each finger as the substrate-triggered nodes are connected to the source terminal of the center-finger NMOS.

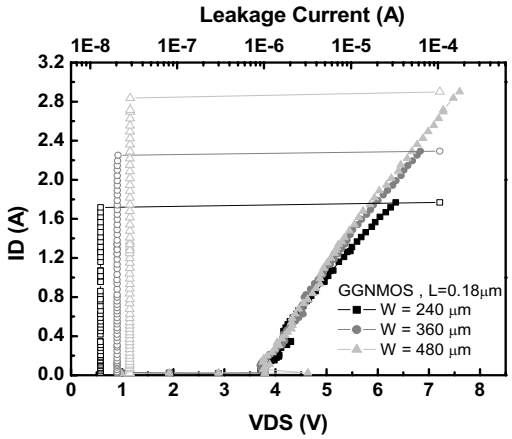


Fig. 3 ATLP-measured I-V curves of traditional GGNMOS under different channel widths, including the corresponding leakage currents.

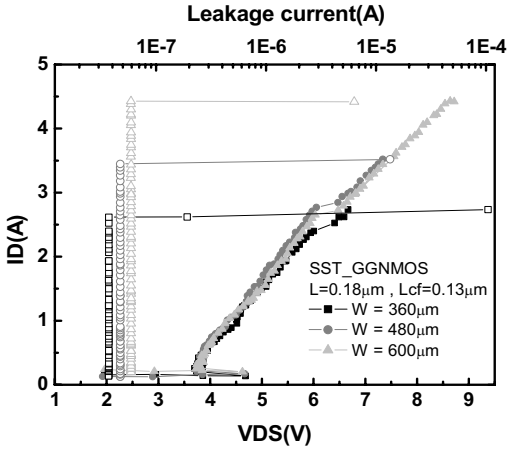


Fig. 4 ATLP-measured I-V curves of SST_GGNMOS under different channel widths, including the corresponding leakage currents.

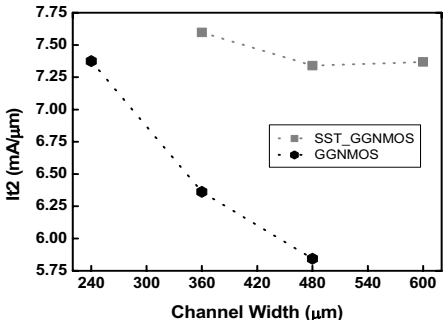


Fig. 5 The dependence of It2 per micron on channel widths of the traditional GGNMOS and the proposed SST_GGNMOS.

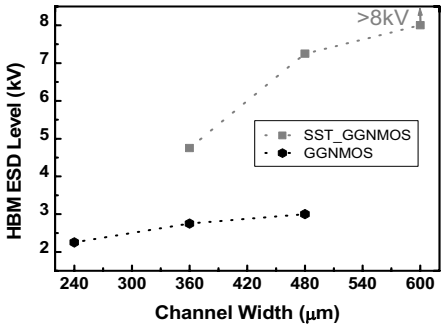


Fig. 6 The relationship between the HBM ESD levels and channel widths of traditional GGNMOS and the proposed SST_GGNMOS.

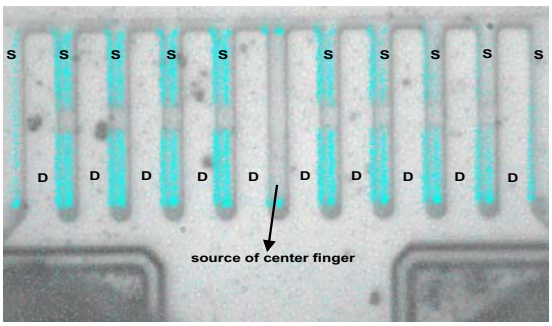


Fig. 7 EMMI photograph on SST_GGNMOS (W/L=600μm/0.18μm, Lcf=0.13μm) to observe its turn-on behavior under current pulse stress. The current distribution is shown by the light-blue color in this picture, where it is among all fingers of SST_GGNMOS.