Active ESD Protection for Input Transistors in a 40-nm CMOS Process

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***Abstract*— This work presents a novel design for input ESD protection. By replacing the protection resistor with an active switch that isolates the input transistors from the pad under ESD stress, the ESD robustness can be greatly improved. The proposed designs were designed and verified in a 40-nm CMOS process using only thin oxide devices, which can successfully pass the typical industry ESD-protection specifications of 2-kV HBM and 200-V MM ESD tests.**

Keywords—ESD, CMOS ICs, ESD protection, Reliability.

I. INTRODUCTION

Electrostatic discharge (ESD) is a major reliability issue in CMOS processes [1]. ESD are high-energy fast transients, as the result of charge balance between two bodies (*e.g.*, an operator with static charges in his body, touching an IC). ESD currents may peak up to several amperes and several thousands of volts, which may damage the internal structures of an IC. In order to avoid ESD damage, special circuits and devices are carefully placed around the IO interface. These circuits detect any ESD that may harm the IC and discharge the ESD current through a safe path. A typical realization for a whole-chip ESD protection scheme is shown in Fig. 1. The ESD diodes (D_{p1}, D_{n1}, D_{p2}, and D_{n2}) together with the power-rail ESD clamp circuit can provide safe discharge paths for any pin-to-pin combination [2].

ESD protection becomes more challenging in the nanoscale CMOS processes. With the shrink in transistors size, the gate oxide of CMOS has been scaled down to less than 2nm. Such a thin oxide has very low breakdown voltage (~5V for 40-nm) and thus becomes very sensitive to ESD damage. Another issue with the thin oxide is the large leakage current due to the tunneling current effect [3]. CMOS processes also offer thick oxide devices to design more robust IO circuits and to comply with legacy IO voltages (such as 2.5V and 3.3V) without large leakage currents, but at the expense of extra steps in the fabrication process. Although some previous works have reported high-voltage tolerant IO circuits implemented only using thin oxide devices [4], [5], for a simple low voltage input buffer, such as shown in Fig. 1, the ESD protection circuits should be oversized to guarantee adequate ESD protection. In addition, the impact in silicon footprint and leakage current could be unacceptable.

This work proposed a novel ESD protection technique for input buffers which can withstand more than 2kV HBM and 200V MM with small silicon area utilization.

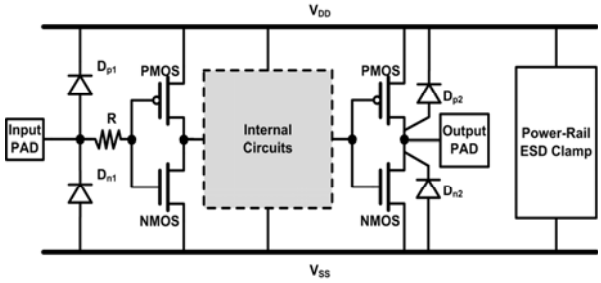

Fig. 1. The whole-chip ESD protection scheme realized with the active power-rail ESD clamp circuit [2].

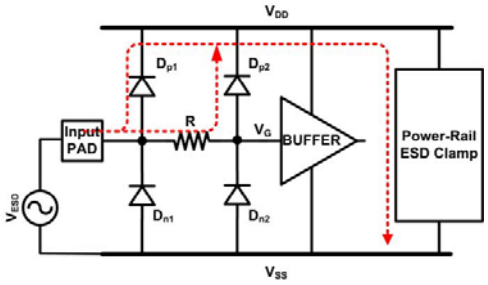

Fig. 2. Traditional ESD protection for the input buffer under positive-to-V_{SS} (PS) stress.

II. ESD PROTECTION FOR INPUT BUFFERS

Traditional ESD protection at the input buffer consists of a pair of ESD diodes connected to V_{DD} and V_{SS} and a protection resistor (R). Usually, a smaller second pair of ESD diodes is placed after the protection resistor to further increase the ESD protection. The function of the protection resistor is to limit the current that may flow directly to the transistors gate. Under a positive ESD stress at the pad, with V_{DD} floating and V_{SS} grounded, the ESD first couples through the ESD diodes to V_{DD}, where the power-rail ESD clamp circuit turns-on and clamps the voltage to its holding voltage. The voltage at the pad is then the holding voltage of the power-rail ESD clamp circuit plus the voltage drop across the ESD diode. The secondary ESD diode conducts some current through the protection resistance to further reduce the voltage at the gate (V_G). All the ESD devices are design such as the maximum gate voltage at a specified stress voltage is lower than the gate oxide breakdown voltage. A schematic of the traditional ESD protection for the input buffer under ESD stress is shown in Fig. 2. Fig. 3 shows a simulation result in a 40-nm CMOS process. For this simulation, the stress is realized following the human body model (HBM), whereas a 100pF capacitor is initially charges with 2kV and then discharges through a 1.5kΩ resistor

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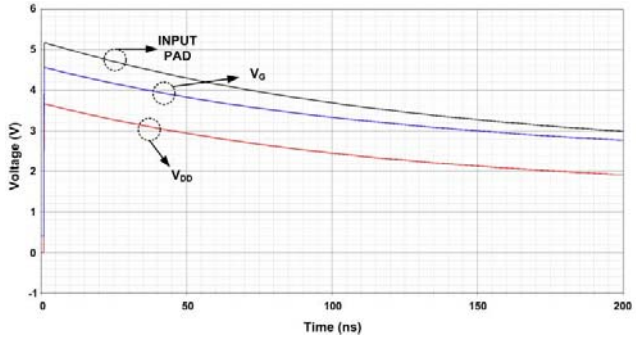


Fig. 3. Simulation results of the traditional input ESD protection for a PS mode 2kV HBM stress.

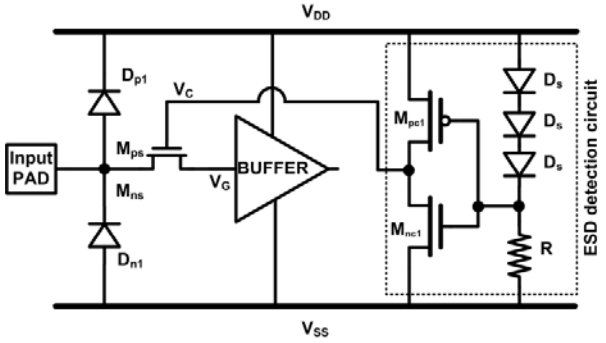


Fig. 4. Schematic of the proposed input ESD protection using an NMOS switch.

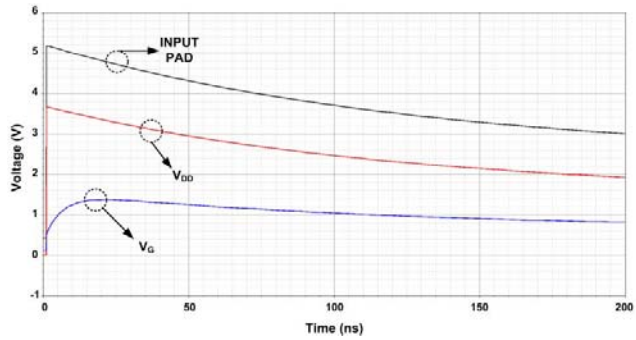


Fig. 5. Simulation results of the proposed input ESD protection using an NMOS switch for a PS mode 2kV HBM stress.

to the circuit. The pad, V_{DD}, and gate voltage (V_G) were measured. The power-rail ESD clamp circuit used in the simulation was a simple BIGFET with an ideal RC detection circuit, designed to provide a clamping voltage just below the gate oxide breakdown voltage. In real applications though, more efficient circuits would be used [6], [7].

III. Proposed Active ESD Protection for Input Buffers

Even though the protection resistor at the input buffer is important for ESD protection, it also impacts the signal integrity as it adds delay. Ideally, it should be small enough to not affect the signal, but also large enough to provide good ESD protection. Therefore, the value of R results as a compromise between ESD robustness and signal integrity. Typical values for the resistor range from 50Ω to 300Ω. The compromise arises as a fact of the value of the resistor cannot be changed on the fly. This work proposes to replace the

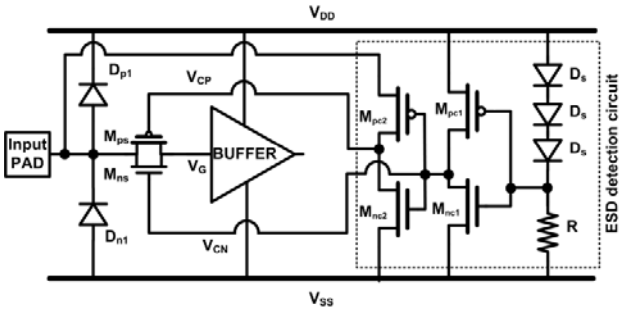
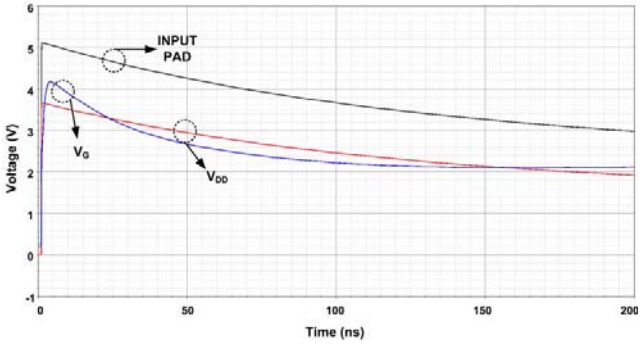
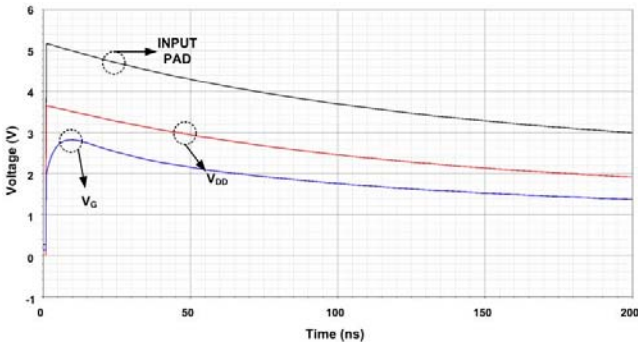


Fig. 6. Schematic of the proposed input ESD protection using a CMOS switch.



(a)



(b)

Fig. 7. Simulation results of the proposed input ESD protection using a CMOS switch for a PS mode 2kV HBM stress. (a) PMOS bulk connected to V_{DD}, and (b) PMOS bulk connected to the input pad.

protection resistor by a switch, which is closed under normal circuit operation, providing a low impedance path to the signal, and open during ESD stress, to isolate the gates and thus provide exceptional ESD protection.

The first realization of the proposed technique is with an NMOS transistor as switch, as shown in Fig. 4. The transistor M_{ns} is controlled by an ESD detection circuit, which can be shared among similar input buffers to reduce area and power consumption. The number of diodes (D_s) in the ESD detection circuit is selected according to the desired trigger voltage. Although an RC delay could be used, the used circuit proved to be more area and power efficient [6]. Under normal circuit operation, V_{DD} is at the stable supply voltage, which is lower than the trigger voltage of the diode string. Thus, there is no current flowing through R, M_{pc} is turned on to drive V_C to the

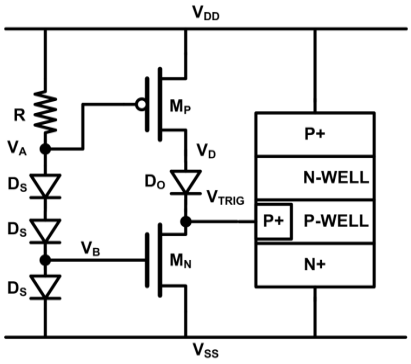


Fig. 8. Schematic of the SCR based power-rail ESD clamp circuit utilized in this work [6].

V_{DD} voltage, and therefore M_{ns} is turned on. The size of M_{ns} can be set to match the desired impedance. Under ESD stress, the diode string would conduct and turn M_{nc} on, driving V_C low and thus keeping M_{ns} off and avoiding damage to the gates. A simulation result for this circuit is shown in Fig. 5. It can be noticed that the voltage at which the gate is held is much lower than for the traditional protection.

Even though the NMOS switch can achieve excellent ESD robustness, it cannot provide full voltage swing (V_G can only go up to V_{DD}-V_{TN}). To overcome this problem, the switch can be implemented with a couple of NMOS and PMOS. Fig. 6 shows a realization of the proposed ESD input protection using a CMOS switch. The ESD detection circuit requires an extra inverter to provide the control signals to both NMOS (V_{CN}) and PMOS (V_{CP}). The M_{pc2} drain has to be connected to the pad and not to V_{DD} because during ESD stress the source will be at the pad voltage, and to fully turn M_{ps} off the gate also has to be at the pad voltage, otherwise M_{ps} would never be fully turned off, and some ESD current may conduct to cause damage to the gates. In addition, the bulk of the PMOS should also be connected to the pad instead of V_{DD}. Otherwise, under ESD stress some current would conduct through the parasitic source/bulk diode from pad to V_{DD}, causing the parasitic bipolar on the PMOS to be triggered and conducting some current to the gate, thus increasing the risk of damage. Fig. 7 shows the simulation results for the proposed circuit of Fig. 6. Notice that for the circuit using M_{ps} bulk connected to V_{DD}, the overshoot at the gate voltage is higher, as expected.

IV. Silicon Verification

A. Test chip

The proposed ESD protection circuits for input buffers were fabricated in a 40-nm CMOS process. The power-rail ESD clamp circuit used in the test circuits is shown in Fig. 8. The SCR is fabricated with 100µm width, and the SCR trigger transistor dimension is W/L=100µm/100nm. The switch transistors (M_{ns} and M_{np}) are designed with dimension of W/L 5µm/100nm, and the ESD diodes area is 40µm^2. For the proposed circuit with the CMOS switch, only the design with the PMOS bulk connected to the pad is implemented. The test buffer used to measure the ESD robustness in the test circuits is a single CMOS inverter with both transistors realized with dimension W/L = 20µm/100nm. The protection resistor for the traditional ESD input protection is 300Ω. The implemented designs of Fig. 2, Fig. 4, and Fig. 6 are labeled in the figures as "TRAD", "NMOS", and "CMOS", respectively.

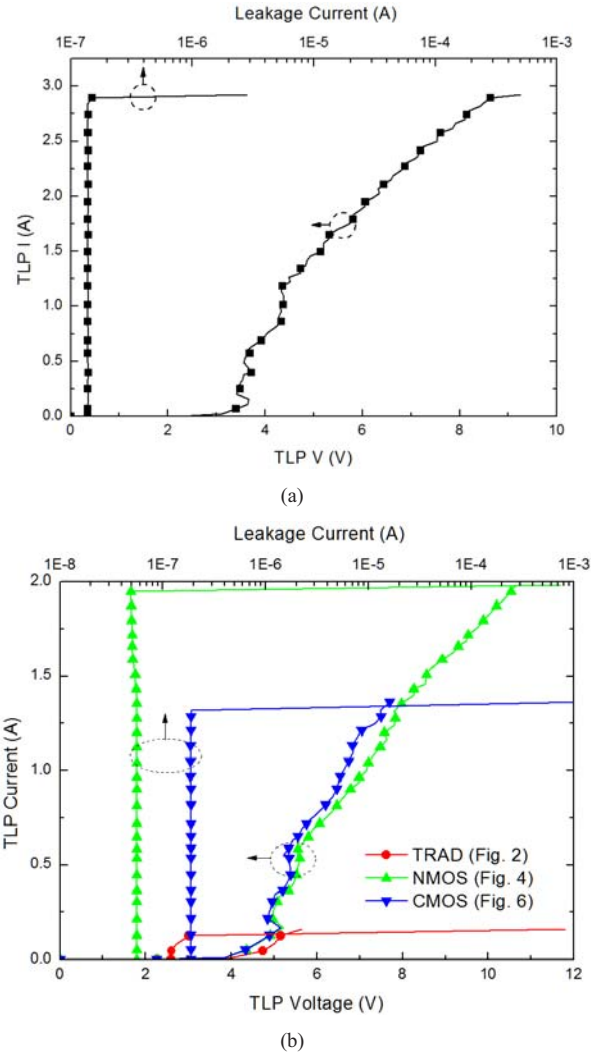


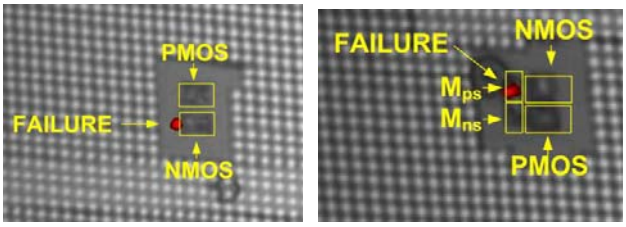
Fig. 9. TLP measurement results for (a) the standalone power-rail ESD clamp circuit (Fig. 8), and (b) the fabricated input ESD protection circuits.

B. TLP measurements

Transmission line pulsing (TLP) is an important verification tool for ESD protection circuits [8]. The measured results are shown in Fig. 9. The traditional design fails at a very low stress, which indicates the ESD protection is not enough to prevent damage at the gates. The I_{t2} currents for the proposed designs are 2A and 1.4A for the NMOS switch and CMOS switch, respectively.

C. ESD robustness

ESD robustness is measured with the HBM [9] and MM [10] models. The stress is increased in steps of 250V (25V) and up to 4kV (400V) for HBM (MM) test. After each stress, the IV curve is measured and compared with the original one. Failure is defined as 30% deviation in the IV curve. Results are summarized in Table I.



(a) (b)

Fig. 10. Failure analysis of the implemented devices using OBIRCH. (a) Traditional design after 250V HBM stress and (b) proposed design using the CMOS switch after 2.75kV HBM stress.

Failure analysis was done after ESD stress to identify the failure mechanism. After ESD stress, the chips are observed using optical beam induced resistance charge (OBIRCH). During design, an unmetallized window is left on top of the designs to facilitate the image capture. FA images are shown in Fig. 10. The traditional design failure spot after HBM stress is located at the NMOS transistor of the input buffer, as indicated by the TLP results. The failure spot for MM stress is also located in the NMOS. The failure spot for the proposed circuit using the CMOS switch after HBM stress occurs at the PMOS switch transistor (M_{ps}). Adding silicide block to the source connection would increase the HBM robustness of this design. For the proposed circuit using the NMOS switch, the failure after MM stress is located at the power-rail ESD clamp circuit.

These results show that the used power-rail ESD clamp circuit does not provide enough protection for the traditional design, although it provides adequate protection for the proposed designs. In order to provide the same protection level to the traditional design, the ESD diodes and power-rail ESD clamp circuit would have to be largely oversized, thus increasing considerably the silicon area utilization and overall standby leakage current.

TABLE I

ESD ROBUSTNESS LEVELS

CIRCUIT	HBM	MM
Standalone power-rail ESD clamp circuit (Fig. 8)	> 4kV	300V
TRAD (Fig. 2)	< 250V	< 25V
NMOS (Fig. 4)	> 4kV	300V
CMOS (Fig. 6)	2.5kV	275V

V. CONCLUSION

A new technique to enhance the ESD robustness of input buffers has been presented and verified in silicon in a 40-nm CMOS process. Using only thin-oxide devices, the proposed circuits can surpass the industry standard of 2-kV HBM and 200-V MM by using a relatively small power-rail ESD clamp circuit, whereas it would not pass the ESD tests when the traditional input ESD protection was used.

VI. ACKNOWLEDGMENTS

The authors would like to thank to TSMC and CIC for chip fabrication. This work was supported in part by the Ministry of Science and Technology (MOST), Taiwan, under Contracts of MOST 103-2622-E-009-006, and MOST 103-2221-E-009-197-MY2.

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