ESD Protection Design for Giga-Hz High-Speed I/O Interfaces in a 130-nm CMOS Process

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ABSTRACT

The electrostatic discharge (ESD) protection design for high-speed input/output (I/O) interfaces in a 130-nm CMOS process is proposed in this paper. First, the ESD protection devices were designed and fabricated to evaluate their ESD robustness and the parasitic effects in giga-hertz frequency band. With the knowledge on the dependence of device dimensions on ESD robustness and the parasitic capacitance, the ESD protection circuit for high-speed I/O interfaces was designed with minimum degradation on high-speed circuit performance but satisfactory high ESD robustness.

I. INTRODUCTION

With the advantage of low cost and high integration, more and more commercial integrated circuits (ICs) had been fabricated in CMOS processes, including the high-speed input/output (I/O) interface circuits. Electrostatic discharge (ESD), which has been a one of the most important reliability issues for CMOS ICs, must be taken into consideration during the design phase. There are two main design considerations in ESD protection design for giga-hertz high-speed I/O interfaces. First, ESD protection circuits for high-speed I/O interfaces must sustain high enough ESD robustness to effectively protect the thin gate oxide in the internal circuits against ESD stress. Second, the degradation of high-speed circuit performance due to the parasitic effects of ESD protection devices needs to be minimized [1].

Traditional ESD protection devices, which have large parasitic capacitance, would significantly degrade high-speed circuit performance. Therefore, traditional ESD protection schemes are no longer suitable for giga-hertz high-speed I/O applications because of the intolerable parasitic effects. It had been reported that the largest design budget on parasitic capacitance at I/O pads, which includes the parasitic capacitances of bond pads and ESD protection circuits, in 2-GHz high-frequency applications is 200 fF [2]. This implies that the ESD protection circuit should be carefully designed to have the smallest parasitic capacitance. With proper design, the double-diode ESD protection scheme in cooperation with active power-rail ESD clamp circuit can be used to realize the whole-chip ESD protection scheme for giga-hertz high-speed I/O applications with minimum degradation on circuit performance. In order to minimize the parasitic capacitance of the ESD devices and to achieve satisfactory ESD robustness, the high-frequency characteristics of the ESD devices in a 130-nm CMOS process had been evaluated in this work to find out the dependence of device size on ESD robustness and parasitic capacitance for high-speed I/O applications. After determining the dimensions of ESD protection devices, whole-chip ESD protection scheme was designed with the active power-rail ESD clamp circuit [3].

In this paper, experimental results on ESD robustness and parasitic capacitance of the fabricated ESD diodes in a 130-nm CMOS process are reported and discussed. The whole-chip ESD protection design for a 2.5-GHz high-speed I/O interface circuit in a 130-nm CMOS process is presented.

II. ESD PROTECTION DESIGN

A. ESD Diodes

The shallow-trench-isolation (STI) diodes used as the input ESD protection device in forward-biased condition can sustain high ESD robustness under a small device size. In a 130-nm CMOS process, device models of P+/N-well diode (D_P) and N+/P-well diode (D_N) were provided by the

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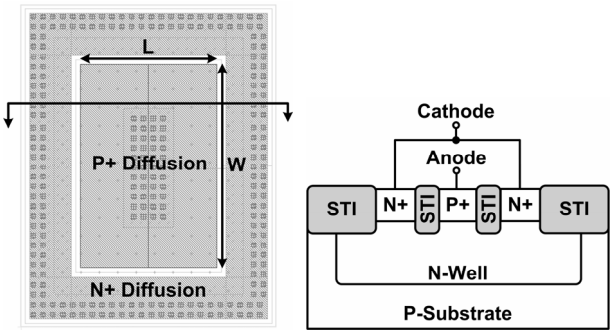
foundry. With the device models, the parasitic capacitance of the ESD diode can be simulated by the simulator such as HSPICE. The P+/N-well diode is used to provide ESD path between the I/O pad and VDD, while the N+/P-well diode is used to provide ESD path between VSS and the I/O pad. The layout top view of a P+/N-well diode is shown in Fig. 1(a). The cross-sectional view of the P+/N-well diode is shown in Fig. 1(b), where the P+ diffusion and N+ diffusion are separated by the STI. The design target was that the total parasitic capacitance at the input pad is lower than 200 fF, including the parasitic capacitance of the bond pad. The relationship between device size and diode capacitance can be obtained from simulation, which helps to determine the dimensions for ESD diode primarily. The diodes with junction perimeters (PJ) of 20 μm, 40 μm, and 80 μm had been designed and fabricated to evaluate their ESD robustness and parasitic capacitance.



(a) (b)

Figure 1: (a) Layout top view of a P+/N-well diode. (b) The cross-sectional view of a P+/N-well diode.

B. ESD Robustness of Diodes

The behaviors of the fabricated diodes in high-current regions can be characterized by the transmission line pulsing (TLP) system [4]. The TLP-measured I-V curves of the P+/N-well diodes and N+/P-well diodes with different dimensions under forward-biased condition are shown in Figs. 2(a) and 2(b), respectively. The secondary breakdown current (It2) is the highest current that the device can handle under ESD stresses, which is the current at the failure point. The It2 of the P+/N-well diodes with junction perimeters of 20 μm, 40 μm, and 80 μm are 0.62 A, 1.47 A, and 4.18 A, respectively. The It2 of the N+/P-well diodes with junction perimeters of 20 μm, 40 μm, and 80 μm are 0.55 A, 1.56 A, and 3.75 A, respectively. To meet the commercial standard of 2-kV human-body-model (HBM) ESD robustness, the corresponding It2 is 1.33 A [5]. Fig. 3 shows the HBM ESD levels of the P+/N-well diode and N+/P-well diode under different device dimensions. Since the diodes with 40-μm junction perimeter have the It2 of more than 1.33 A, they can sustain HBM ESD stress of more than 2 kV.

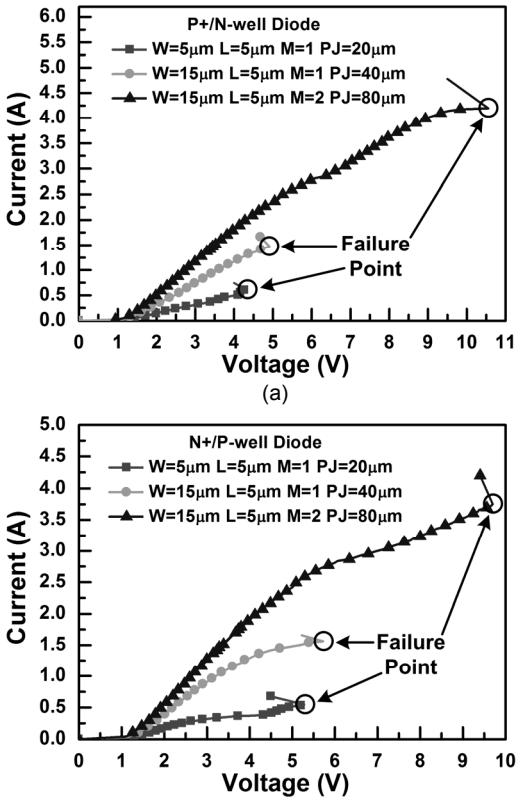


Figure 2: TLP-measured I-V curves of (a) P+/N-well diodes and (b) N+/P-well diodes with different device dimensions under forward-biased condition.

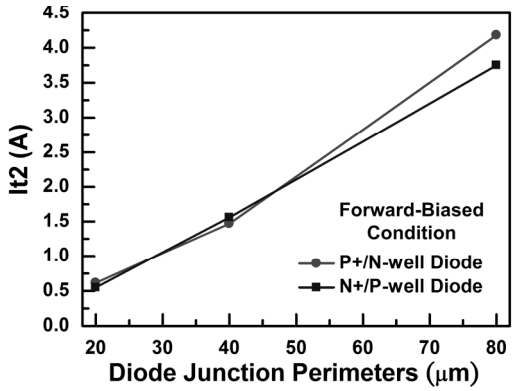


Figure 3: HBM ESD robustness of P+/N-well diodes and N+/P-well diodes under different device dimensions.

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C. Parasitic Capacitance of Diodes

To use the diodes as ESD protection devices for giga-hertz high-speed I/O interfaces, the parasitic capacitance of the ESD diodes must be evaluated. The two-port S-parameters of the fabricated ESD diodes were characterized by on-wafer measurement with Cascade Infinity ground-signal-ground (G-S-G) microwave probes and Agilent E8364B network analyzer. Port 1 and port 2 of the network analyzer were connected to the two terminals of the fabricated ESD diodes in S-parameter measurement. With the conversions between two-port S-parameters and Z-parameters, the parasitic capacitance (C_{diode}) of the ESD diodes was extracted as $C_{diode} = -1 / [\omega\ \mathrm{Im}(Z_{11})]$, where Z_{11} parameter is the impedance seen from port 1 with port 2 open. Fig. 4 shows the extracted parasitic capacitances of the ESD diodes with different device dimensions.

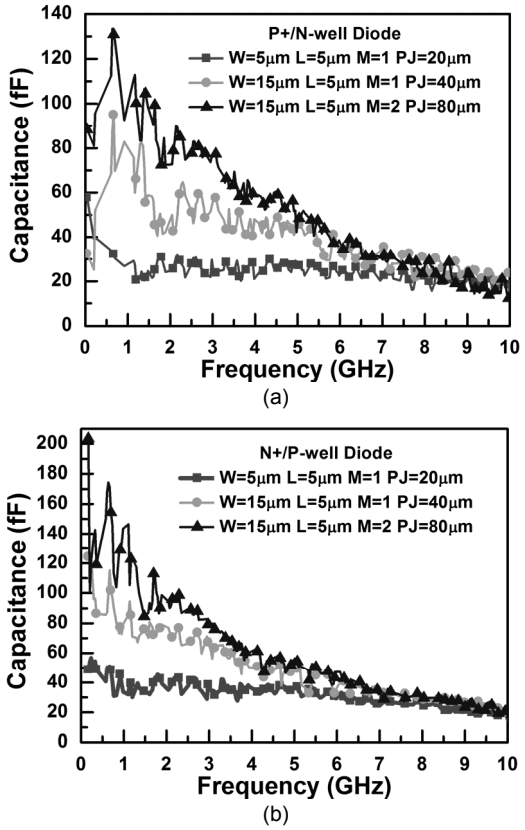

Figure 4: Measured parasitic capacitances of (a) P+/N-well diodes and (b) N+/P-well diodes with different device dimensions under frequency up to 10 GHz.

The parasitic capacitance of ESD diode becomes larger when the diode size increases. This is because larger junction area contributes larger junction capacitance. Since the design goal is that the total parasitic capacitance at input node is lower than 200 fF, the ESD diode with 80-μm is too large to meet such a design goal.

III. WHOLE-CHIP ESD PROTECTION DESIGN

A. Receiver NMOS with ESD Protection

To provide comprehensive ESD protection against all ESD-test modes, including positive-to-VSS mode (PS-mode), positive-to-VDD mode (PD-mode), negative-to-VSS mode (NS-mode), and negative-to-VDD mode (ND-mode), whole-chip ESD protection is needed, which is illustrated in Fig. 5 [1]. With ESD diodes (D_P and D_N) at the input pad, the power-rail ESD clamp circuit is necessary to provide ESD current discharging path between VDD and VSS power lines during ESD stresses [3]. The ESD clamp device between VDD and VSS used in this work is the p-type substrate-triggered silicon-controlled rectifier (P-STSCR) [6]. Silicon-controlled rectifier (SCR) has been demonstrated to have the highest ESD robustness under the smallest device size, so it was used as the ESD clamp device in this work. In PS-mode ESD test, a positive ESD stress is applied to the input pin, with VSS pin grounded and VDD pin floating. During PS-mode ESD stresses, ESD energy is conducted to VDD by D_P. The RC delay keeps the gate potential of M_P low enough to turn on M_P. When M_P is turned on, some ESD current is conducted by M_P from VDD line to trigger on the P-STSCR to provide ESD path between VDD and VSS. With the active power-rail ESD clamp circuit, the ESD diodes are assured to be operating in the forward-biased condition rather than the reverse-biased condition under all ESD-test modes, which leads to higher ESD robustness.

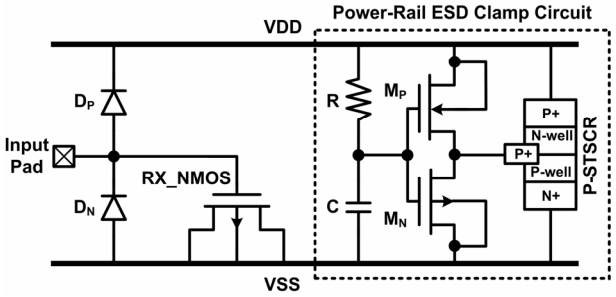

Figure 5: The dummy RX_NMOS used as test circuit to verify the effectiveness of the proposed ESD protection scheme (diodes + active power-rail ESD clamp circuit).

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To verify the ESD robustness of the whole-chip ESD protection scheme, the circuit shown in Fig. 5 had been designed and fabricated in a 130-nm CMOS process. In Fig. 5, an NMOS (RX_NMOS) was added with its gate terminal connected to the input pad and its drain, source, and bulk terminals connected to VSS. RX_NMOS was used to evaluate the ESD protection capability for a receiver, which is protected by the proposed ESD protection scheme. The It2 levels of the ESD protected RX_NMOS with different ESD diode dimensions are listed in Table 1. With the diode junction perimeter of 55 μm, the It2 level is greater than 1.33 A, which corresponds to HBM ESD robustness of over 2 kV.

Table 1: It2 of RX_NMOS under Different ESD-Test Modes

D_P PJ (μm)	D_N PJ (μm)	It2 (A)			
		PS	PD	NS	ND
45	45	1.31	1.66	1.53	2.71
55	55	1.49	1.71	1.68	2.68

B. 2.5-GHz Receiver Circuit with ESD Protection

The whole-chip ESD protection circuit had been applied to a 2.5-GHz receiver interface circuit in a 130-nm CMOS process. As shown in Fig. 6, the two differential input pads were protected by the ESD diodes. To save the chip area and reduce the parasitic capacitance at the input pad, the ESD diodes, M_P, M_N, and P-STSCR were placed under the bond pad. The layout top view of the 2.5-GHz receiver interface circuit with ESD protection is shown in Fig. 7. The HBM ESD robustness of the fabricated receiver interface circuit had been evaluated by the ESD simulator. The measured HBM ESD level of the fabricated receiver interface circuit is larger than 3 kV under the four ESD-test modes.

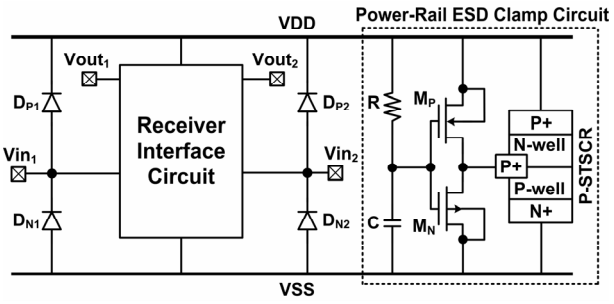

Figure 6: The 2.5-GHz receiver circuit with whole-chip ESD protection design.

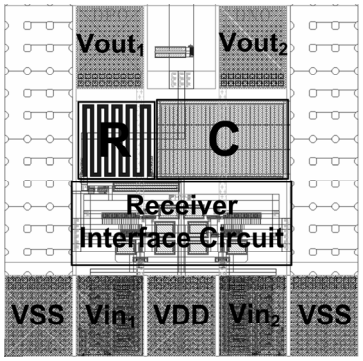

Figure 7: Layout top view of a 2.5-GHz receiver interface circuit with whole-chip ESD protection in a 130-nm CMOS process.

IV. CONCLUSION

The ESD protection design for giga-hertz high-speed I/O interfaces has been addressed. With the proposed ESD protection design, the two most important requirements of ESD protection design for giga-hertz high-speed I/O interfaces, which are ESD robustness and parasitic capacitance, can be met simultaneously.

ACKNOWLEDGEMENT

This work was supported in part by the National Science Council (NSC), Taiwan, under Contract NSC 95-2221-E-009-330, and in part by the Faraday Technology Corporation, Taiwan.

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