Design on New Tracking Circuit of I/O Buffer in 0.13-μm Cell Library for Mixed-Voltage Application

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***Abstract*— This paper presents a new tracking circuit design without standby leakage current issue for 2.5V/3.3V tolerant I/O buffer, which is suitable for the I/O cells in the mixed-voltage applications with different driving capabilities. One set of mixed-voltage I/O cell with the new proposed 2.5V/3.3V tolerant I/O buffer circuit has been designed and drawn in a 0.13-μm salicided CMOS process. The new tracking circuit can be also applied in other CMOS processes to serve different mixed-voltage I/O interfaces.**

I. INTRODUCTION

With the scaled-down CMOS technology in nanometer generation, the power supply voltage is also decreased to reduce power consumption. Figure 1 shows the voltage levels of power supplies in different technology generations. For example, the VDD voltage levels of core logic and I/O buffers in the typical 0.13-μm CMOS process are 1.2V and 2.5V, respectively. However, some peripheral components or other ICs in a microelectronic system are still operated with the higher voltage levels such as 3.3V or 5V for different system specifications. In other words, the chips with higher output voltage may drive the chips with lower power supply voltage in a system, and vice versa. The conventional CMOS I/O buffer is not suitable in the mixed-voltage system, because several issues may arise, such as gate-oxide reliability [1], hot carrier degradation [2], and undesirable leakage current paths [3].

Several process or circuit design techniques were reported to solve the aforementioned issues in the mixed-voltage applications [4] – [10]. The dual-oxide process [4] and stacked NMOS [5] are widely used in I/O buffer to avoid gate-oxide reliability issue for mixed-voltage applications. The additional N-well bias [6] or tracking circuits for self-biased body and gate terminals of PMOS devices [7] – [10] are used to overcome the leakage current issues. However, there are some drawbacks in using additional N-well bias in the mixed-voltage I/O buffer. First, the layout routing becomes difficult due to the requirement of the additional pad and associated metal connection delivering the bias to the body terminal of PMOS transistors. Second, because the body terminal is coupled to an external voltage source higher than the voltage of the source terminal, the threshold voltage of the pull-up PMOS is increased due to the body effect. Third, the gate voltage of pull-up PMOS also needs to be suitably controlled for reducing leakage current. On the other hand, the self-biased tracking circuit for I/O buffer is a better choice for mixed-voltage application without aforementioned drawbacks. However, when an I/O cell library was built up, the programmable driving capability with modified finger numbers of output buffer must be included. Furthermore, the pull-up or pull-down resistors will be also designed in the I/O cells for different applications. In the previous tracking circuit reported in [8], unexpected leakage current for the I/O cells with low driving capability or with built-in pull-down resistor will occur, which will be discussed in section II.

In this paper, a mixed-voltage I/O buffer with new tracking circuit is proposed to overcome the undesirable leakage issues, especially for the I/O cells with low driving capability or built-in pull-down resistor. The new proposed 2.5V/3.3V tolerant I/O buffer circuit has been implemented in a 0.13-μm salicided CMOS process with a compact layout area.

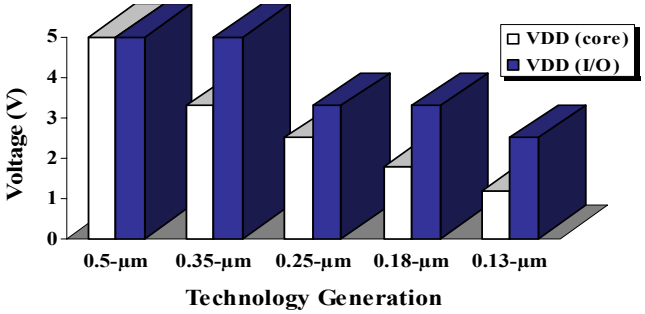

Figure 1. Comparison on power supply voltages in different technology generations.

II. CMOS I/O BUFFERS FOR MIXED-VOLTAGE APPLICATIONS

A. Conventional CMOS I/O Buffer

Figure 2 shows the conventional CMOS I/O buffer using in a mixed-voltage environment. The power supply voltage of VDDIO is 2.5V, but the input signal swing at the I/O pad may rise up to 3.3V in the receiving (input) mode. The gate voltages of NMOS and PMOS of output buffer are controlled

by pre-driver circuit and biased at 0V and 2.5V in the receiving (input) mode to turn off the pull-down NMOS and the pull-up PMOS, respectively. However, when the input voltage at the pad rises as high as 3.3V in the receiving mode, the parasitic drain-to-well diode of PMOS will be forward biased and the channel of PMOS will be also turned on. Therefore, this PMOS conducts incorrectly to cause leakage current path from pad to VDD through its channel and the parasitic diode. Besides, the overstress voltage across gate oxide of the MOS devices is another serious reliability issue to the mixed-voltage I/O interface circuits. As shown in Figure 2, the pull-down NMOS and the transistors in the input buffer suffer overstress voltage across their gate oxides. The gate oxide may become leaky due to tunneling effect or dielectric breakdown. If the electric field across the gate oxide is too large, it may even be permanently damaged. Therefore, the conventional CMOS I/O buffer is not suitable for the mixed-voltage application.

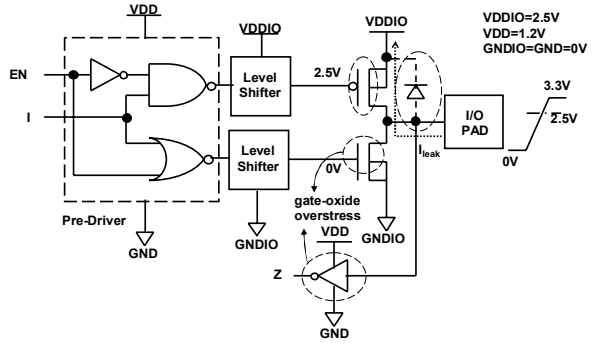

Figure 2. The leakage and gate-oxide overstress issues for the conventional CMOS I/O buffer in the mixed-voltage environment.

B. Mixed-Voltage I/O Buffer

The block diagram of mixed-voltage I/O buffer is shown in Figure 3. The tracking circuits including floating N-well and gate-tracking circuits are used to bias the body and gate of pull-up PMOS for overcoming leakage current from pad to VDDIO through the parasitic drain-to-well junction diode and the channel of pull-up PMOS, respectively. The pre-driver is used to control the tri-state I/O buffer into the receiving (input) mode, the transmitting (output) mode, or the high impedance (high-z) mode by the control signal EN. The ESD protection circuit is used to enhance the ESD robustness of the mixed-voltage I/O buffer.

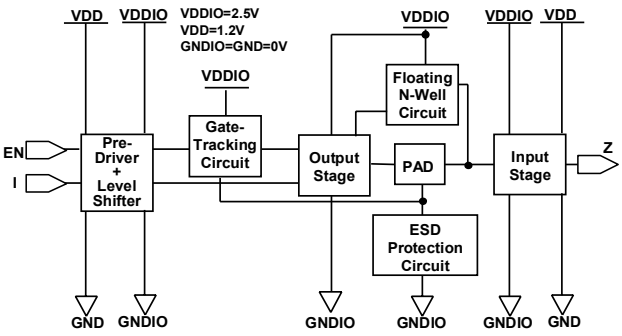

Figure 3. The block diagram of mixed-voltage I/O buffer.

There were several designs reported to realize the tracking circuits [7] – [10]. For a pure I/O buffer without extra functions (such as programmable driving capability or built-in pull-down resistor), the previous tracking circuits are operated well. However, such functions are usually included in the I/O cell library. From both of simulation and measurement results, the previous tracking circuits cause some unexpected leakage currents in the I/O cells which have the functions of programmable driving capability or built-in pull-down resistor.

C. Unexpected Leakage Issues

Figure 4 shows the mixed-voltage I/O buffer with tracking circuit reported in [8]. When the input voltage at the pad rises as high as 3.3V in the receiving mode, the N-well (marked with X in Figure 4) is biased by the input signal through the parasitic drain-well junction diode of pull-up PMOS (MM4). There is no leakage current from pad to VDDIO through the parasitic drain-well diode, but the N-well is biased at 3.3V-$V_{cut\text{-}in}$, where $V_{cut\text{-}in}$ is the cut-in voltage of parasitic drain-well junction diode.

Figure 5 shows the output buffer of I/O cell with the programmable driving capability. In the I/O cell with programmable driving capability, the total channel width of output buffer (MM4/MM9) and ESD protection devices (MM4'/MM9') is fixed. For example, for the I/O cell with driving current of 2mA, the finger number of MM4/MM9 is 1, and the finger number of MM4'/MM9' for ESD protection is 11. On the other hand, for the I/O cell with driving current of 16mA, the finger number of MM4/MM9 is 8, and the finger number of MM4'/MM9' for ESD protection is 4. The driving capability of the I/O cell is programmable by adjusting the finger numbers between MM4/MM9 and MM4'/MM9'. Because MM4' should be turned off during normal circuit operation, the gate terminal of MM4' is connected to its body (N-well). However, when the input voltage at the pad rises as high as 3.3V in the receiving mode, the N-well voltage is biased at 3.3V-$V_{cut\text{-}in}$. The leakage current is conducted from the pad to VDDIO through the weakly turned-on MM4'. Figure 6 shows the measured I-V curves at the pad of the I/O cells with programmable driving capability. The leakage current is increased when the pad voltage is higher than 2.7V. The I/O cell with lower driving capability has higher leakage current because of larger size of MM4'.

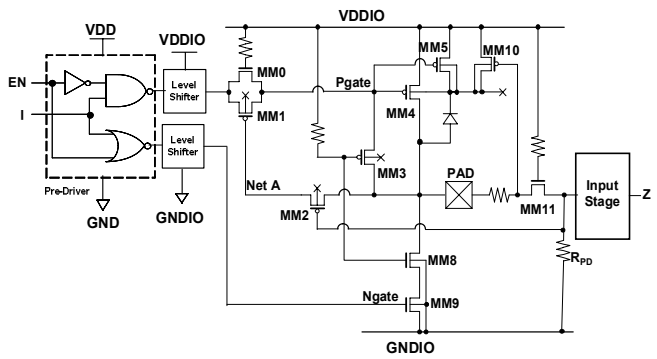

Figure 4. The tracking circuit for mixed-voltage application reported in [8].

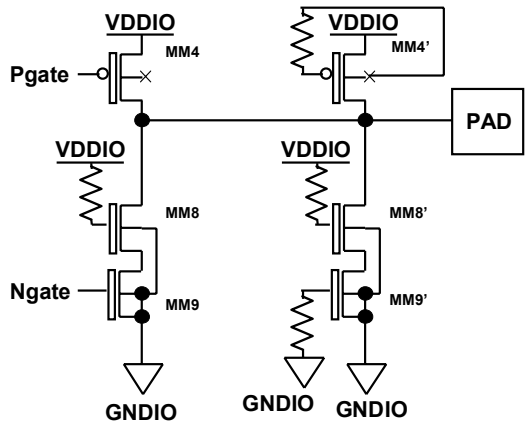

Figure 5. The output stage of the I/O cells with programmable driving capability.

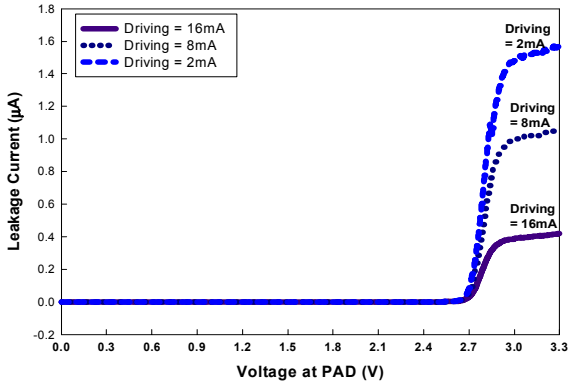

Figure 6. The measured I-V curves at the pad of the I/O cells with different driving capability.

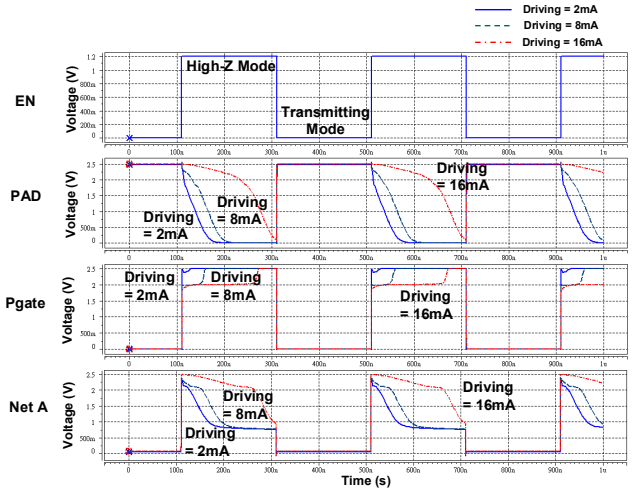

Figure 7. The simulation results of the I/O cells with different driving capability from logic high in the transmitting mode into the high-z mode.

Besides the unexpected leakage current in the I/O cell with low driving capability, the tracking circuit shown in Figure 4 is also not suitable for the I/O cell with built-in pull-down resistor (R_{PD} in Figure 4). Figure 7 shows the simulation results of the I/O cells with different driving capability from the logic high in the transmitting mode into the high-z mode, which is controlled by the control signal EN. During the I/O cells from the logic high in the transmitting mode into the high-z mode, MM4 should be turned off by charging its gate (marked as Pgate in Figure 4) to VDDIO, and the voltage at pad will be discharged to ground through the pull-down resistor R_{PD}. However, MM1 is initially off because its gate (marked as Net A in Figure 4) voltage is quickly charged to VDDIO through the turned-on MM2. Therefore, the Pgate will not be charged to VDDIO for turning MM4 off because MM1 is not turned on. Furthermore, it is more difficult to pull down the Net A for the I/O cell with higher driving capability because MM4 which has larger size is still turned on with stronger driving strength to pull up the pad, and Net A is also still pulled up through the turned-on MM2. For this reason, the propagation delay from logic high in the transmitting mode into the high-z mode for the I/O cell with higher driving capability will be longer, which is shown in Figure 7.

From the above description, a new tracking circuit has to be designed for solving the aforementioned issues in the mixed-voltage I/O buffer.

III. The New Proposed Tracking Circuit

A. Circuit Design

Figure 8 shows the I/O buffer with the new proposed tracking circuit for mixed-voltage application, where the thick-oxide devices (for 2.5V at VDDIO) are used in the I/O buffer excluding the pre-driver with thin-oxide devices (for 1.2V at VDD). In this new proposed tracking circuit, MM12 is added for biasing N-well (marked with X in Figure 8) to the correct 3.3V when the input voltage at the pad rises as high as 3.3V in the receiving mode. Therefore, the gate voltage of MM4' (shown in Figure 5) will be kept at 3.3V without leakage issue in the receiving mode for the I/O cells with programmable driving capability.

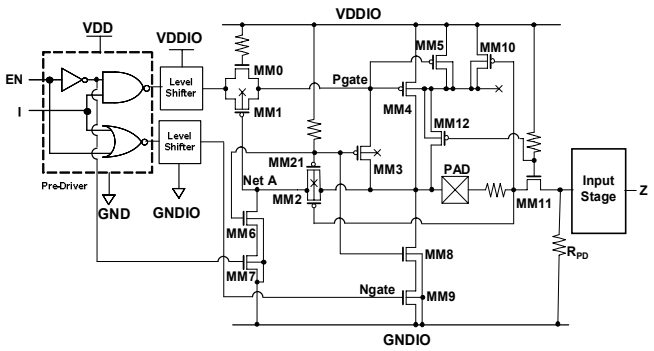

Figure 8. The new proposed tracking circuit for mixed-voltage application.

Comparison between Figures 4 and 8, the MM6, MM7, and MM21 devices are added, and the gate terminal of MM2 is connected to the node after the input resistor in this new proposed design. Figure 9 shows the simulation results of the new proposed I/O cells with different driving capability from the logic high in the transmitting mode into the high-z mode. From the simulation results, Net A is not charged to VDDIO in the new proposed design because MM2 is kept off by its gate connected to the node after the input resistor. Therefore, as shown in Figure 9, the propagation delay of pad from

logic high in the transmitting mode into the high-z mode are the same for all I/O cells with different driving capability. MM21 is used to charge Net A to 3.3V to turn off MM1 when received input signal of 3.3V in the receiving mode. Stacked MM6 and MM7 are used to bias Net A of 0V to keep MM1 turned-on in the transmitting mode and without gate-oxide reliability issue when Net A is charged to 3.3V in the receiving mode.

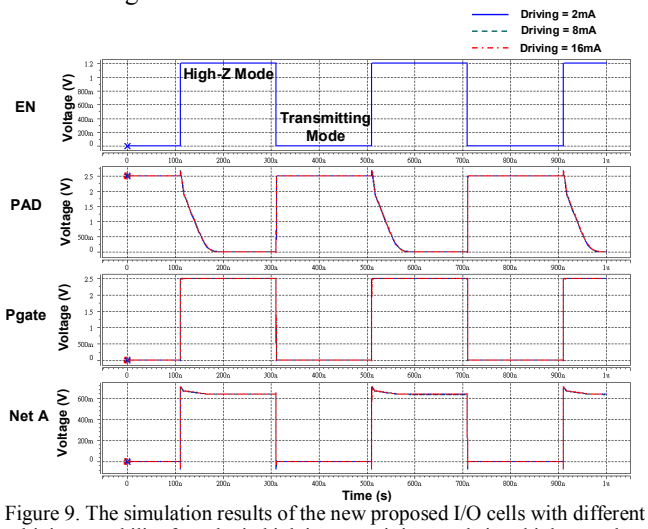

Figure 9. The simulation results of the new proposed I/O cells with different driving capability from logic high in transmitting mode into high-z mode.

B. *Experimental Results*

Figure 10 shows the measured I-V curves at the pad of the new proposed I/O cells with programmable driving capability. When the input voltage at the pad rises as high as 2.6V in the receiving mode, the N-well and gate terminals of MM4' are still at 2.5V because MM12 is not turned on. The leakage current is conducted from the pad to VDDIO through the weakly turned-on MM4'. Therefore, the peak leakage current is observed when the input voltage at the pad is 2.6V. The maximum leakage current is only 6nA of the I/O cell with driving capability of 2mA. However, when the pad voltage passes 2.6V, the leakage current is reduced to only ~1.5nA due to the turned-on MM12. Compared to Figure 6, the leakage current issue for 2.5V/3.3V tolerant I/O buffer (shown in Figure 6) has been solved in this proposed design.

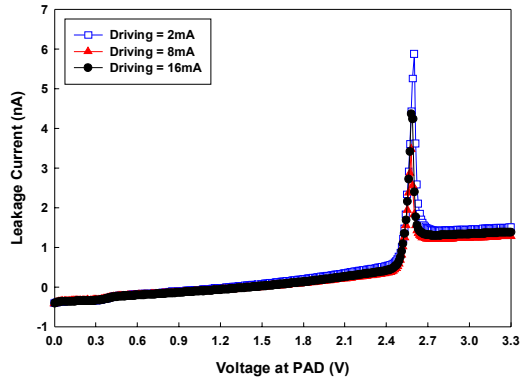

Figure 10. The measured I-V curves at the pad of the new proposed I/O cells with different driving capability.

The measured results of I/O cell with 16mA driving capability from the logic high in the transmitting mode into the high-z mode are shown in Figure 11. During the I/O cells from the logic high in the transmitting mode into the high-z mode, the voltage at pad will be discharged to ground through the pull-down resistor R_{PD} (shown in Figure 8). This new proposed tracking circuit is suitable for the I/O cell with built-in pull-down resistor.

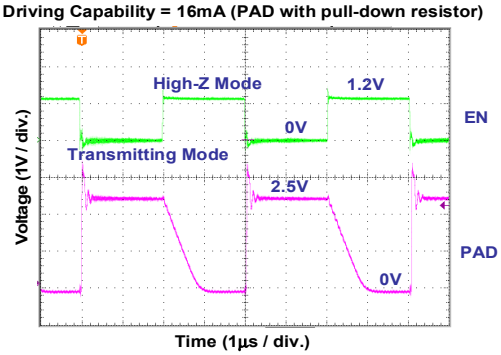

Figure 11. The measured waveform of the new proposed I/O cell with driving capability of 16mA from logic high in transmitting mode into high-z mode.

IV. Conclusion

A new tracking circuit for 2.5V/3.3V mixed-voltage I/O buffer is proposed. This new proposed tracking circuit does not cause the leakage current issue for the I/O cells with programmable driving capability. It can successfully pull down the pad voltage through the pull-down resistor when the pad translating into high-z mode. This tracking circuit can be also applied in other CMOS processes to serve different mixed-voltage applications.

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