Unexpected Failure in Power-Rail ESD Clamp Circuits of CMOS Integrated Circuits in Microelectronics Systems During Electrical Fast Transient (EFT) Test and the Re-Design Solution

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***Abstract* — Four different on-chip power-rail electrostatic discharge (ESD) clamp circuits have been designed to investigate their susceptibility to electrical fast transient (EFT) test. From the experimental results, the feedback loop in two kinds of on-chip power-rail ESD clamp circuits provides the lock function to perform a latchup-like failure after the EFT test. The re-design solution will be developed to overcome this issue to meet the regulation of EFT/EMC test.**

I. Introduction

Whole-chip electrostatic discharge (ESD) protection has become an important task on the reliability of integrated circuits (ICs) in the deep-submicron CMOS technology, because the internal circuits of CMOS IC's with the scaled-down device sizes are more vulnerable to ESD damage. In order to obtain high ESD robustness, a CMOS IC must be designed with on-chip ESD protection circuits at the input/output (I/O) pins and across the power lines. To avoid the unexpected ESD damages located in the internal circuits after pin-to-pin ESD stress or V_{DD}-to-V_{SS} ESD stress, the turn-on-efficient ESD protection circuit is required to clamp the overstress across the gate oxide of internal circuits. The typical on-chip ESD protection design with power-rail ESD clamp circuit in CMOS ICs is shown in Fig. 1 [1]. When the input (or output) pin is zapped under the positive-to-V_{SS} (PS-mode) or negative-to-V_{DD} (ND-mode) ESD stresses, the power-rail ESD clamp circuit can provide a low impedance path between V_{DD} and V_{SS} to efficiently discharge ESD current. In the power-rail ESD clamp circuit, the ESD-transient detection circuit is designed to detect ESD event and sends a control voltage to the gate of ESD-clamping NMOS. The ESD-clamping NMOS can be turned on quickly by a positive gate voltage rather than by the drain snapback breakdown. To enhance the triggering efficiency of the power-rail ESD clamp circuit, some advanced designs on the ESD-transient detection circuit had been reported [2]-[5].

Recently, the electromagnetic compatibility (EMC) of ICs has attracted more attentions than before in the microelectronic products. This tendency results from not only the increased integration density of ICs, but also the strict requirement of reliability regulation, such as the electrical fast transient test (EFT) for electromagnetic compatibility [6]. Therefore, engineers have to deal with the lower immunities to electromagnetic interferences in microelectronic products. Since the susceptibility of a final microelectronic product may only depend on just one single chip, the characterization of EMC susceptibility at IC level is getting more important.

In this work, the malfunction or wrong triggering behavior among different on-chip power-rail ESD clamp circuits under EFT test were investigated. Some ESD-transient detection circuits designed with feedback loop in the power-rail ESD clamp circuits will continually keep the ESD-clamping NMOS in the latch-on state after the EFT test. The latch-on ESD-clamping NMOS between V_{DD} and V_{SS} power lines in the powered-up microelectronic system will in turns cause serious latchup-like failure in CMOS ICs.

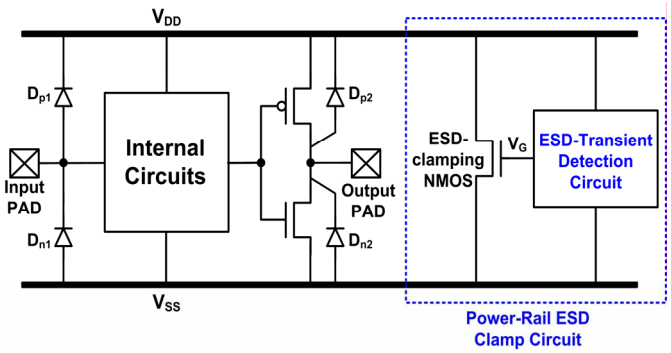

Fig. 1. The typical on-chip ESD protection design with efficient power-rail ESD clamp circuit.

II. Power-Rail ESD Clamp Circuits

To provide effective on-chip ESD protection, four different power-rail ESD clamp circuits had been reported [2]-[5], which are re-drawn in Figs. 2(a)-2(d) with the names of (1) typical RC-based power-rail ESD clamp, (2) power-rail ESD clamp with PMOS feedback, (3) power-rail ESD clamp with NMOS+PMOS feedback, and (4) power-rail ESD clamp with cascaded PMOS feedback.

The typical RC-based power-rail ESD clamp circuit is illustrated in Fig. 2(a) with a three-stage buffer between the

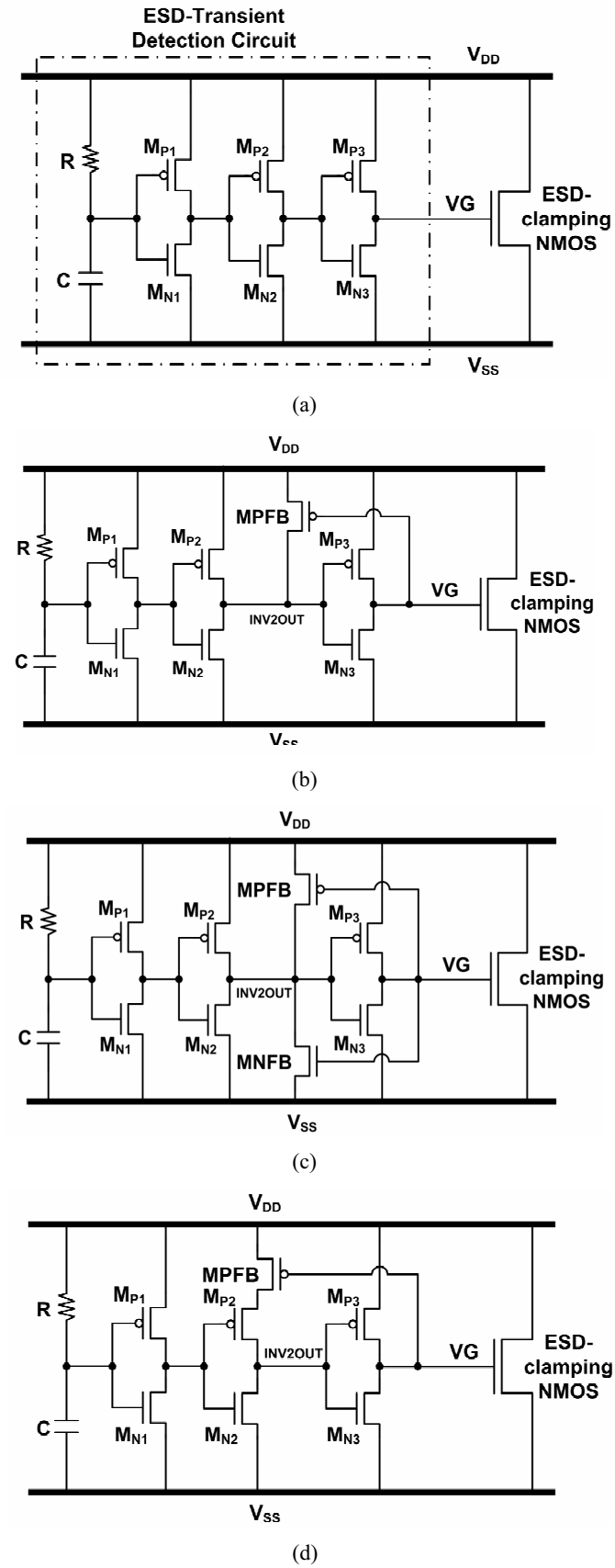

Fig. 2. Four different power-rail ESD clamp circuits designed with (a) typical RC-based detection, (b) PMOS feedback, (c) NMOS+PMOS feedback, and (d) cascaded PMOS feedback.

RC circuit and the ESD-clamping NMOS [2]. The ESD-clamping NMOS is used to provide a low impedance path between the V_{DD} and V_{SS} to discharge ESD current. The RC time constant in the RC-based ESD-transient detection circuit has been typically designed about 0.1 ~1μs to detect the ESD pulses with the rise time of ~10ns and to keep off the power-rail ESD clamp circuit under normal power-on transition with the rise time of ~1ms.

The power-rail ESD clamp circuit incorporated with PMOS feedback [3], as shown in Fig. 2(b), can be used to mitigate false triggering during a fast power-up transition (rise time <10μs). The transistor MPFB can help to keep the gate voltage of ESD-clamping NMOS below the threshold voltage and further reduce the current drawn during the power-up transition.

In the advanced CMOS technology with thinner gate oxide, the large MOS capacitance could suffer large gate-oxide leakage current. It was reported that the power-rail ESD clamp circuit incorporated with a regenerative feedback network can be used to reduce the RC time constant [4], as illustrated in Fig. 2(c). When a fast positive-going ESD transient appears across the power lines, the MNFB can further pull the potential of INV2OUT node towards ground to latch the ESD-clamping NMOS in the conducting state until the voltage on V_{DD} drops below the threshold voltage of ESD-clamping NMOS.

The power-rail ESD clamp circuit with cascaded PMOS feedback has also been proposed to reduce the RC time constant and to solve false trigger issue during fast power-up transition [5], as shown in Fig. 2(d). During the ESD-stress condition, the transistor MPFB is turned off and the voltage on the INV2OUT node can be remained at a low state. If the power-rail ESD clamp circuit is mis-triggered by fast transient, the voltage on the INV2OUT node can be charged up toward V_{DD} by the subthreshold current of MPFB.

Such four power-rail ESD clamp circuits have been fabricated in a 0.18-μm 1.8-V CMOS process for verification in EFT test.

III. Electrical Fast Transient (EFT) Test

A. Measurement Setup

The standard of IEC 61000-4-4 has defined the immunity requirements and test methods for electronic equipment to repetitive electrical fast transients, such as those originating from switching transients (interruption of inductive loads, relay contact bounce, etc.). The repetitive electrical fast transient test is a test with bursts consisting of a number of fast pulses, coupled into power supply or signal ports of electronic equipments. The specified waveforms of these fast transients with the repetition frequency of 5 kHz are shown in Figs. 3(a) and 3(b). In Fig. 3(a), the burst duration is defined with 15ms and repeats every 300 ms. The start value

of the pulse peak is 200V (the minimum voltage provided by EFT generator), and the application time for each voltage level is not less than 1 minute. In Fig. 3(b), the waveform of a single pulse has a rise time of about 5 ns and a pulse duration of 50 ns. The repetition frequency is 5 kHz (period of 0.2 ms).

The measurement setup for EFT test is shown in Fig. 4. A supply voltage of 1.8V is used as V_{DD} and the EFT generator is connected directly to the device under test (DUT) through the cable in this work. The voltage and current waveforms on the DUT (at V_{DD} node) after EFT test are monitored by the digital oscilloscope. After every EFT zapping, the voltage level on V_{DD} of IC is measured again to watch whether latchup-like failure occurs after the test, or not. When the latchup-like failure occurs, the voltage level on VDD node will be pulled down to a lower voltage level due to the latch-on state of ESD-clamping NMOS in the power-rail ESD clamp circuit.

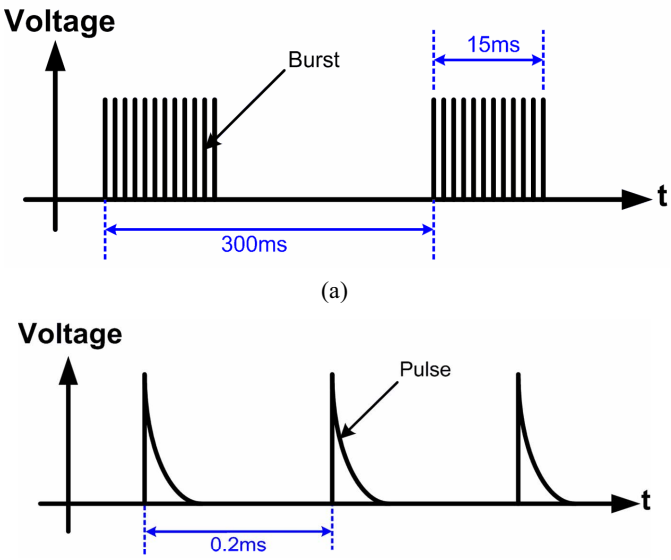

Fig. 3. Specified fast transient waveforms of (a) burst and (b) single pulse with repetition frequency of 5kHz.

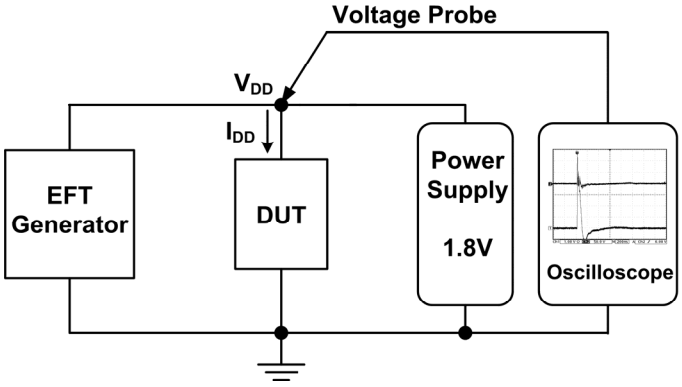

Fig. 4. Measurement setup for Electrical Fast Transient (EFT) test with the IC power supply of 1.8V.

B. Experimental Results

With the EFT measurement setup in Fig. 4, the V_{DD} and I_{DD} transient responses can be recorded by the oscilloscope, which can clearly indicate whether the latchup-like failure occurs (I_{DD} will significantly increase). Figs. 5(a) and 5(b) show the measured V_{DD} and I_{DD} transient response on the power-rail ESD clamp circuit with NMOS+PMOS feedback structure under the test with EFT voltage level of -200V and +200V, respectively. After the EFT test with an initial EFT voltage level of -200V, latchup-like failure can be found in this power-rail ESD clamp circuit, because I_{DD} significantly increases and V_{DD} is pulled down, as shown in Fig. 5(a). After the EFT test with an initial EFT voltage level of +200V, latchup-like failure is also observed in Fig. 5(b). All the PMOS and NMOS devices in the ESD-transient detection circuits are surrounded with double guard rings to guarantee no latchup issue in this region. This implies that the feedback loop in the ESD-transient detection circuit is locking after EFT test and to continually keep the ESD-clamping NMOS in its latch-on state. From the observed voltage and current waveforms, the large I_{DD} current is due to the latch-on state of ESD-clamping NMOS after EFT test.

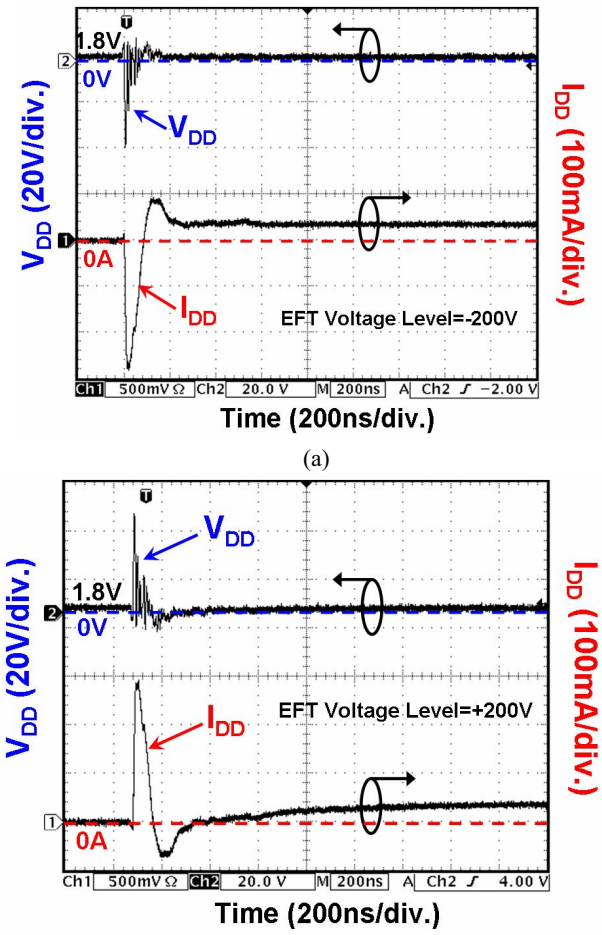

Fig. 5. Measured V_{DD} and I_{DD} waveforms on the power-rail ESD clamp circuit with NMOS+PMOS feedback under EFT test with voltage levels of (a) -200V and (b) +200V.

The EFT levels (the minimum voltage of EFT voltage level to induce the latchup-like failure on V_{DD}) among the aforementioned four different power-rail ESD clamp circuits are listed in Table 1. The power-rail ESD clamp circuits with NMOS+PMOS feedback or with cascaded PMOS feedback have lower EFT levels to cause latchup-like failure after EFT test. From these experimental results, the power-rail ESD clamp circuit designed with NMOS+PMOS feedback is highly sensitive to transient-induced latchup-like failure. The typical power-rail ESD clamp circuit with RC-based detection and without feedback loop has much higher EFT level. The continued latchup-like state will result in malfunction or damage in CMOS IC inside the DUT due to the pulled-down V_{DD} level and the huge I_{DD} current. The failure location after EFT test has been inspected and shown in Fig. 6, which is located along V_{DD} power line (even drawn with a metal width of 30μm) between the power-rail ESD clamp circuit and the V_{DD} bond pad.

Table 1: Comparison on EFT levels among four different power-rail ESD clamp circuits under EFT test.

Power-Rail ESD Clamp Circuits	Positive EFT Level	Negative EFT Level
Typical RC-Based Detection	Over +800V	Over -800V
With PMOS Feedback	Over +800V	Over -800V
With NMOS+PMOS Feedback	Under +200V *	Under -200V *
With Cascaded PMOS Feedback	+500V	Under -200V *

* The start value of the pulse peak is ±200V (the minimum voltage provided by EFT generator).

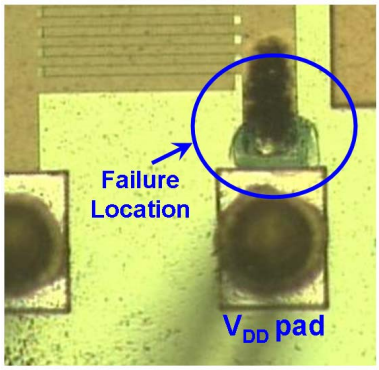

Fig. 6. After EFT test, the failure spot (metal burning out) is located at the power line between power-rail ESD clamp circuit and the V_{DD} bond pad.

IV. Conclusion

Some of advanced on-chip power-rail ESD clamp circuits designed with feedback loop in their ESD-transient detection circuits have been found to suffer the latchup-like failure after the EFT test. The latch-on state in ESD-clamping NMOS is kept by the feedback loop in the ESD-transient detection circuit after electrical fast transients. The huge I_{DD} current in such a latchup-like state will result in malfunction or damage in CMOS ICs. Some modified designs should be developed to overcome such unexpected failure in the on-chip power-rail ESD clamp circuits. *The re-design solution to overcome this issue will be shown in th presentaion.*

References

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