ESD Protection Design for High-Speed Applications in CMOS Technology

Jie-Ting Chen[1], Chun-Yu Lin[2], Rong-Kun Chang[1], Ming-Dou Ker[1], Tzu-Chien Tzeng[3], and Tzu-Chiang Lin[3]

[1]Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan
[2]Department of Electrical Engineering, National Taiwan Normal University, Taipei, Taiwan
[3]Novatek Microelectronics Corp., Hsinchu, Taiwan

***Abstract*—To prevent from electrostatic discharge (ESD) damages, the ESD protection design must be added on chip. The ESD protection design with low parasitic capacitance is needed for high-speed applications. In this work, an ESD protection design realized by stacked diodes with embedded silicon-controlled rectifier was proposed. Verified in silicon chip, the proposed ESD protection design with lower parasitic capacitance and higher ESD robustness was more suitable for high-speed ESD protection in CMOS technology.**

I. Introduction

The high-speed integrated circuits have been designed and fabricated in nanoscale CMOS processes due to the advantages of high integration and potential for mass production [1]. However, the transistors currently used in nanoscale CMOS technologies are sensitive to electrostatic discharge (ESD) events [2], [3]. In order to sustain the required ESD robustness, all integrated circuits need to be equipped with ESD protection designs [4], [5], including the high-speed integrated circuits [6], [7]. However, the parasitic capacitance of the ESD protection circuit at the I/O pad is one of the most important design considerations for the high-speed circuits [8]. As shown in Fig. 1, the parasitic capacitance of ESD protection circuit will cause the signal loss from the pad to ground, and then the circuit performance is deteriorated.

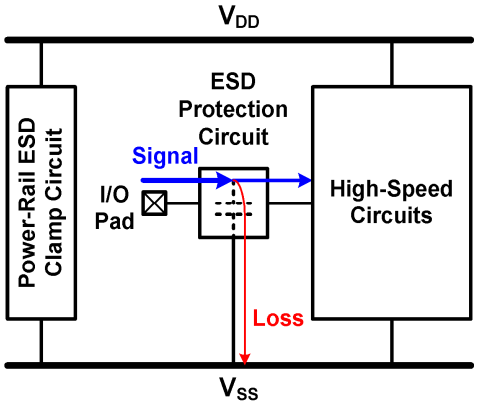


Fig. 1. Signal loss at I/O pad of high-speed circuits with ESD protection circuit.

This work was supported in part by Novatek Microelectronics Corp., Taiwan, and in part by Ministry of Science and Technology (MOST), Taiwan, under Contracts of MOST 105-2221-E-009-166, MOST 103-2221-E-009-197-MY2, and MOST 104-2622-E-009-003.

In order to effectively protect the high-speed circuits and to minimize the parasitic effects of ESD protection circuits, several high-speed ESD protection designs have been reported [6]-[10]. For improved ESD robustness and reduced parasitic capacitance, a novel ESD protection design for high-speed applications is proposed in this work and is verified in a nanoscale CMOS process. The performances of the proposed ESD protection design are compared with those obtained using conventional ESD protection design.

II. Conventional and Proposed ESD Protection Designs

The ESD protection diodes have been widely used for high-speed applications, since they can fit the typical specification on the parasitic capacitance and ESD robustness [10]. A conventional ESD protection circuit for high-speed I/O consists of a pair of primary ESD diodes (D_{P1} and D_{N1}), a pair of secondary ESD diodes (D_{P2} and D_{N2}), and a series resistor (R_{ESD}), as shown in Fig. 2. The device cross-sectional views of P-type diode (D_{P1} and D_{P2}) and N-type diode (D_{N1} and D_{N2}), are shown in Figs. 3(a) and 3(b), respectively.

In the ESD-test standards, there are several ESD-test pin combinations, including positive I/O-to-V_{DD} (PD), positive I/O-to-V_{SS} (PS), negative I/O-to-V_{DD} (ND), and negative I/O-to-V_{SS} (NS) ESD tests. When D_P (D_{P1} and D_{P2}) and D_N (D_{N1} and D_{N2}) in the conventional ESD protection design are under forward-biased condition, they can provide the efficient current-discharging paths from I/O pad to V_{DD} and from V_{SS} to I/O pad, respectively. With the help of power-rail ESD clamp circuit, the conventional ESD protection design provides the whole-chip ESD protection for all ESD-test pin combinations.

In order to reduce the parasitic capacitance from ESD protection diodes without sacrificing ESD robustness, the ESD protection diodes in stacked configuration can be used. The stacked diodes with embedded silicon-controlled rectifier (SDSCR) has been reported to be useful for ESD protection with low parasitic capacitance, fast turn-on speed, and high

978-1-5090-0916-9/16/$31.00 ©2016 IEEE

ESD robustness [11], [12]. In this work, the SDSCR are further applied to the high-speed applications. The proposed ESD protection circuit for high-speed I/O consists of a pair of primary SDSCR (SD_{P1} and SD_{N1}), a pair of secondary SDSCR (SD_{P2} and SD_{N2}), and a series resistor (R_{ESD}), as shown in Fig. 4. This ESD protection design also provides the whole-chip ESD protection for all ESD-test pin combinations.

Figs. 5(a) and 5(b) show the device cross-sectional views of P-type SDSCR (SD_{P1} and SD_{P2}) and N-type SDSCR (SD_{N1} and SD_{N2}), respectively. The terminals which connected to I/O pad are always laid at the center to reduce the parasitic capacitance. Besides, the top metal is used for routing to I/O pad. In the beginning of ESD stress, the stacked diodes will turn on to discharge the initial current, and then the embedded SCR will take over to discharge the primary current, as shown with the dotted lines in Fig. 5.

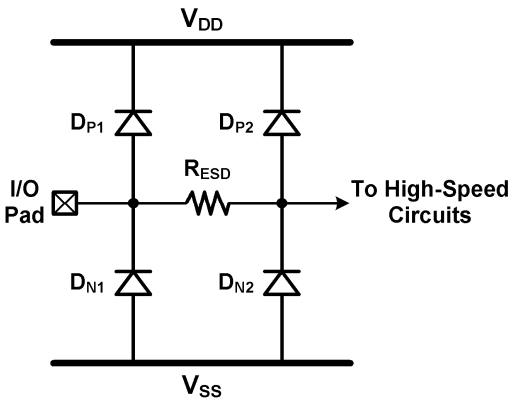


Fig. 2. Conventional ESD protection circuit.

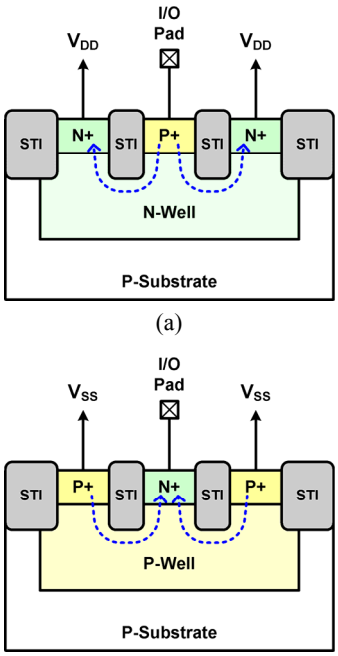


Fig. 3. Device cross-sectional view of (a) P-type diode and (b) N-type diode, used in conventional ESD protection circuit.

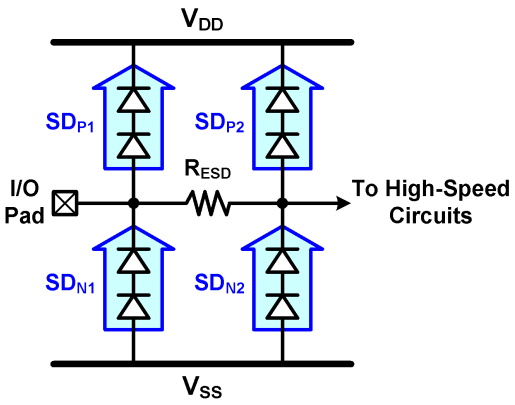


Fig. 4. Proposed ESD protection circuit.

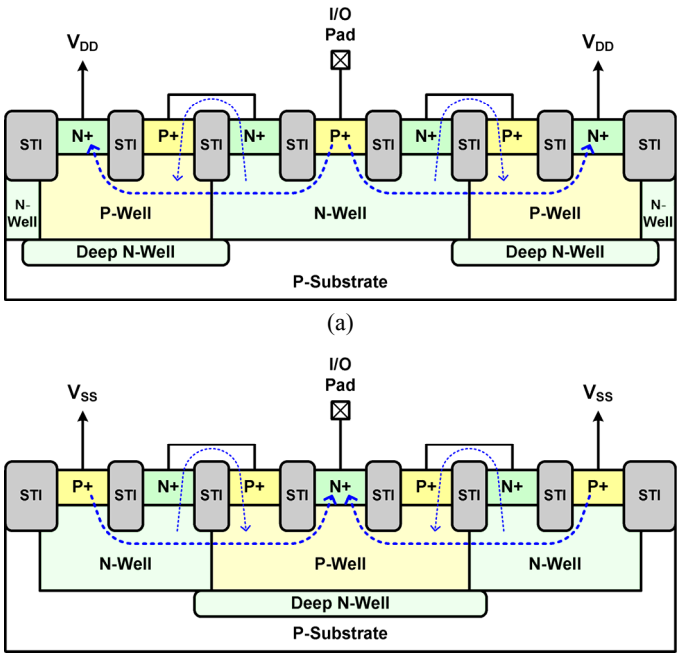


Fig. 5. Device cross-sectional view of (a) P-type SDSCR and (b) N-type SDSCR, used in proposed ESD protection circuit.

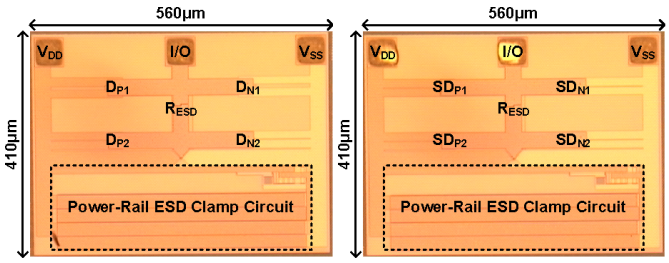
III. Experimental Results

The conventional and proposed ESD protection designs have been fabricated in a nanoscale CMOS process. The width of each ESD device is selected to be 30μm. The R_{ESD} utilizes 50Ω resistor, and the power-rail ESD clamp circuit utilizes the RC-inverter-triggered NMOS. Figs. 6(a) and 6(b) show the chip photographs of the conventional and proposed ESD protection designs, respectively.

A. ESD Robustness

The human-body-model (HBM) ESD robustness of both test circuits are tested. The failure criterion is defined as the I-V characteristics shifting over 30% from its original curve after ESD stressed at every ESD test level. The HBM ESD robustness of both test circuits under all pin combinations are

listed in Table I. The HBM ESD robustness of the conventional ESD protection design is 4.2kV, which is obtained from the lowest level of PD, PS, ND, and NS tests. The HBM ESD robustness of the proposed ESD protection design can be improved to 4.8kV.



(a) (b)

Fig. 6. Chip micrographs of (a) conventional ESD protection design and (b) proposed ESD protection design.

B. TLP I-V Characteristics

To investigate the turn-on behavior and the I-V characteristics of the circuits in the domain of HBM ESD event, the transmission-line-pulsing (TLP) system with a 10ns rise time and a 100ns pulse width is used. The TLP-measured I-V curves of both test circuits under PD, PS, ND, and NS tests are shown in Fig. 7. The secondary breakdown current (I_{t2}), which indicates the current-handling ability, of the test circuit can be obtained from the TLP-measured I-V curve. The TLP-measured I_{t2} of both test circuits under all pin combinations are listed in Table I. The I_{t2} of the proposed ESD protection design is higher than that of the conventional ESD protection design.

C. Parasitic Capacitance

Fig. 8 shows the extracted parasitic capacitance of both test circuits. The parasitic capacitance of the proposed ESD protection design is lower than that of the conventional ESD protection design.

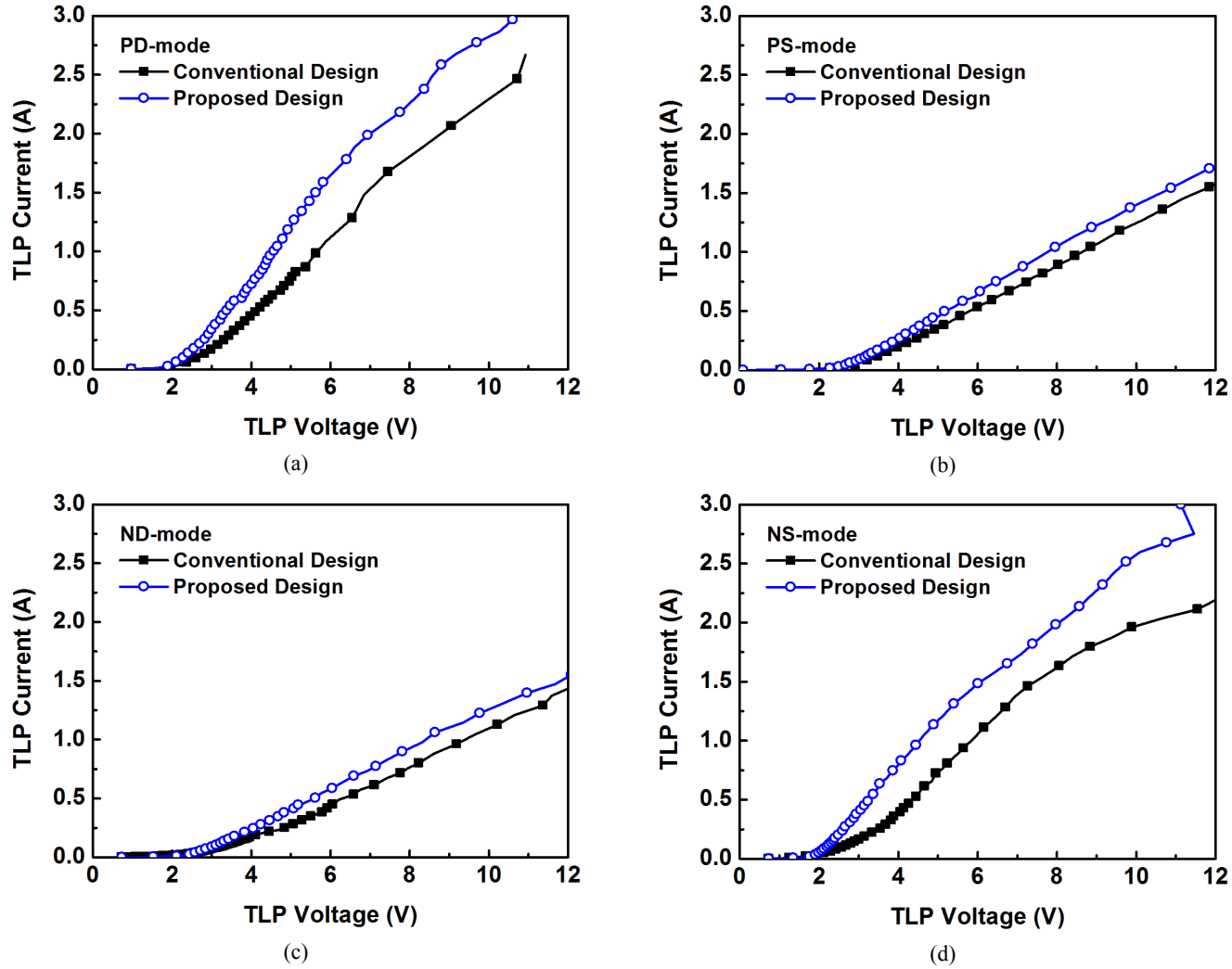


Fig. 7. TLP-measured I-V characteristics of test circuits under (a) PD, (b) PS, (c) ND, and (d) NS tests.

D. Comparison

Since the high ESD robustness and low parasitic capacitance is needed for high-speed applications, the figure of merit (FOM) used in this work is

$$FOM = \frac{HBM}{C_{parasitic}} \quad (1)$$

where HBM denotes the lowest level of PD, PS, ND, and NS tests, and $C_{parasitic}$ is the parasitic capacitance at 5GHz. The FOM of conventional and proposed ESD protection designs are 42.1V/fF and 81.4V/fF, respectively; therefore, the proposed ESD protection design can achieve the better FOM.

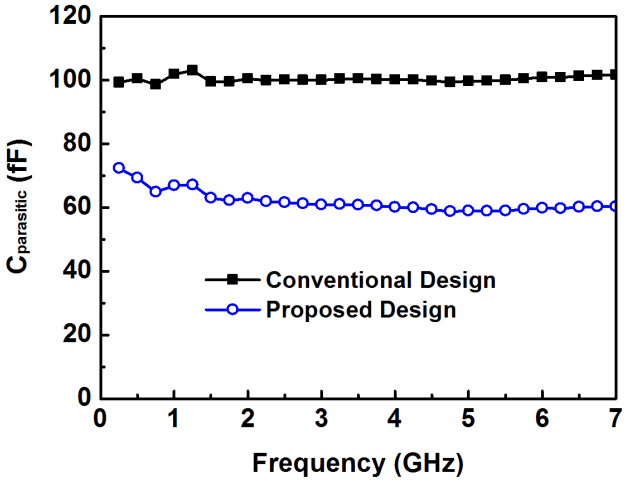


Fig. 8. Measured parasitic capacitances of test circuits.

Table I. Measurement results of test circuits.

	Conventional Design	Proposed Design
PD HBM	4.5kV	5.2kV
PS HBM	4.5kV	5.2kV
ND HBM	4.2kV	4.8kV
NS HBM	4.2kV	5.2kV
PD I_{t2}	2.5A	2.9A
PS I_{t2}	2.4A	2.7A
ND I_{t2}	2.2A	2.8A
NS I_{t2}	2.2A	2.8A
$C_{parasitic}$ (at 5GHz)	99.7fF	59.0fF
FOM	42.1V/fF	81.4V/fF

IV. Conclusion

The proposed ESD protection circuit has been developed in nanoscale CMOS process for high-speed applications. Measurement results verify that the proposed ESD protection circuit has lower parasitic capacitance and higher ESD robustness; therefore, the proposed ESD protection circuit can be a good solution for high-speed applications in CMOS technology.

References

[1] K. Kaviani, A. Amirkhany, C. Huang, P. Le, W. Beyene, C. Madden, K. Saito, K. Sano, V. Murugan, K. Chang, and X. Yuan, "A 0.4-mW/Gb/s near-ground receiver front-end with replica transconductance termination calibration for a 16-Gb/s source-series terminated transceiver," *IEEE J. Solid-State Circuits*, vol. 48, no. 3, pp. 636-648, Mar. 2013.

[2] C. Duvvury, "ESD qualification changes for 45nm and beyond," in *IEDM Tech. Dig.*, 2008, pp. 337-340.

[3] J. Li, K. Chatty, R. Gauthier, R. Mishra, and C. Russ, "Technology scaling of advanced bulk CMOS on-chip ESD protection down to the 32nm node," in *Proc. EOS/ESD Symp.*, 2009, pp. 69-75.

[4] F. Altolaguirre and M.-D. Ker, "Power-rail ESD clamp circuit with embedded-trigger SCR device in a 65-nm CMOS process," in *Proc. Midwest Symp. Circuits and Systems (MWSCAS)*, 2014, pp. 250-253.

[5] R. Salmeh, "Impacts of the pads, ESD diodes and package parasitic on the noise figure and gain of a common source low noise amplifier," in *Proc. Midwest Symp. Circuits and Systems (MWSCAS)*, 2010, pp. 946-952.

[6] S. Cao, J. Chun, S. Beebe, and R. Dutton, "ESD design strategies for high-speed digital and RF circuits in deeply scaled silicon technologies," *IEEE Trans. Circuits and Systems—I: Regular Papers*, vol. 57, no. 9, pp. 2301-2311, Sep. 2010.

[7] Q. Cui, J. Salcedo, S. Parthasarathy, Y. Zhou, J. Liou, and J. Hajjar, "High-robustness and low-capacitance silicon-controlled recti• er for high-speed I/O ESD protection," *IEEE Electron Device Letters*, vol. 34, no. 2, pp. 178-180, Feb. 2013.

[8] R. Wong, R. Fung, and S. Wen, "Networking industry trends in ESD protection for high speed IOs," in *Proc. Int. ASIC Conf.*, 2013.

[9] N. Jack and E. Rosenbaum, "ESD protection for high-speed receiver circuits," in *Proc. Int. Reliability Physics Symp.*, 2010, pp. 835-840.

[10] C.-T. Yeh, M.-D. Ker, and Y.-C. Liang, "Optimization on layout style of ESD protection diode for radio-frequency front-end and high-speed I/O interface circuits," *IEEE Trans. Device and Materials Reliability*, vol. 10, no. 2, pp. 238-246, Jun. 2010.

[11] C.-Y. Lin, M.-L. Fan, M.-D. Ker, L.-W. Chu, J.-C. Tseng, and M.-H. Song, "Improving ESD robustness of stacked diodes with embedded SCR for RF applications in 65-nm CMOS," in *Proc. Int. Reliability Physics Symp.*, 2014.

[12] R. Sun, Z. Wang, M. Klebanov, W. Liang, J. Liou, and D. Liu, "Silicon-controlled rectifier for electrostatic discharge protection solutions with minimal snapback and reduced overshoot voltage," *IEEE Electron Device Letters*, vol. 36, no. 5, pp. 424-426, May 2015.