

Study on the ESD-Induced Gate-Oxide Breakdown and the Protection Solution in 28nm High-K Metal-Gate CMOS Technology

Chun-Yu Lin¹, Ming-Dou Ker², Pin-Hsin Chang², and Wen-Tai Wang³

¹Department of Electrical Engineering, National Taiwan Normal University, Taiwan

²Institute of Electronics, National Chiao Tung University, Taiwan

³Global Unichip Corporation, Taiwan

Abstract—To protect the IC chips against the electrostatic discharge (ESD) damages in 28nm high-k metal-gate (HKMG) CMOS technology, the ESD protection consideration was studied in this work. The ESD design window was found to be within 1V and 5.1V in 28nm HKMG CMOS technology. An ESD protection device of PMOS with embedded silicon-controlled rectifier (SCR) was investigated to be suitable for ESD protection in such narrow ESD design window.

Index Terms—CMOS, electrostatic discharge (ESD), high-k metal-gate (HKMG), silicon-controlled rectifier (SCR).

I. INTRODUCTION

As CMOS technologies keep scaling down, the thin oxide thickness of MOS transistors has made the integrated circuits to be sensitive to the electrostatic discharge (ESD) [1]. A typical specification for IC chips on human-body-model (HBM) ESD robustness is 2kV [2]. In order to protect the IC chips against the ESD damages, on-chip ESD protection devices must be equipped for the pads that may be stressed by ESD. The typical on-chip ESD protection design is shown in Fig. 1, which consists of the ESD protection devices between input/output (I/O) pad and V_{DD}/V_{SS} , and between V_{DD} and V_{SS} [3]. Although the high-k metal-gate has been introduced in sub-50nm CMOS technologies, the MOS transistors are still sensitive to ESD [4]. Moreover, because the average cost of a die in sub-50nm technologies is expensive, it is important to optimize ESD protection devices to have a high ESD robustness within limited cell area.

To discharge the high ESD energy without causing damage to internal circuits, the typical ESD protection devices include the diode, MOS, and silicon-controlled rectifier (SCR) [5]–[7]. The SCR device has been reported to be useful for ESD protection due to its high ESD robustness, small device size, and excellent clamping capabilities (low holding voltage and small turn-on resistance) [7]. Besides, the SCR device can be safely used without latchup danger in advanced CMOS technologies with the low supply voltage [8]. Moreover, a PMOS with embedded SCR device has been presented to have low trigger voltage [9]. In this work, the PMOS with embedded SCR device is further investigated.

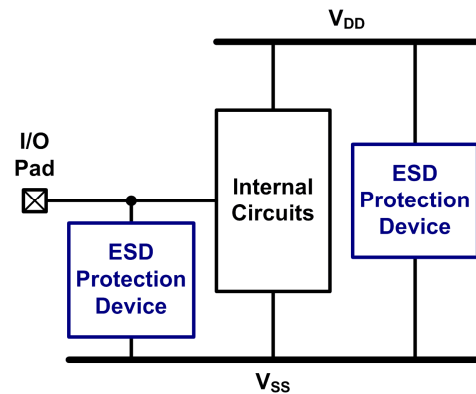


Fig. 1. On-chip ESD protection against ESD damages.

II. ESD-INDUCED GATE-OXIDE BREAKDOWN

To investigate the gate-oxide breakdown voltage, an NMOS was fabricated in the 28nm high-k metal-gate CMOS process. When a metal wire contacted to the transistor gate, it can charge up to a voltage sufficient to zap the thin gate oxide. In order to protect the gate-oxide from damage during the metal wire contacted to the transistor gate, the NMOS with a protection diode was fabricated in the same time, and then the protection diode was removed by using the focused ion beam (FIB). After the protection diode was removed, the breakdown voltage of intrinsic gate oxide can be evaluated, as shown in Fig. 2.

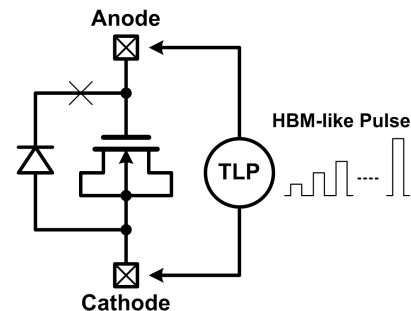


Fig. 2. Test device to evaluate the gate-oxide breakdown voltage of the MOSFET.

A transmission-line-pulsing (TLP) system with a 10ns rise time and a 100ns pulse width is used to evaluate the gate-oxide breakdown voltage in the time domain of HBM ESD event. Fig. 3 shows the measured leakage current under 0.9V bias of the test device after TLP test. As indicated by the leakage-current evolution of the stressed gate oxide, the damage occurs at the breakdown voltage of 5.1V.

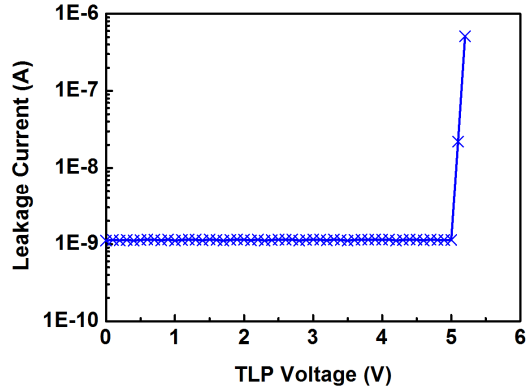


Fig. 3. Measured leakage current under 0.9V bias of test device after TLP test.

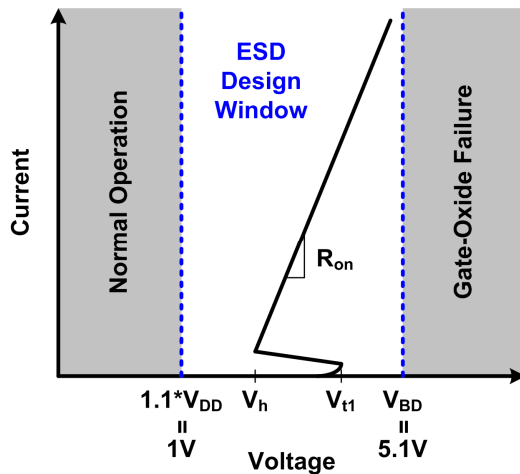


Fig. 4. ESD design window defined by the power-supply voltage with 10% variation ($1.1 \cdot V_{DD}$) and the gate-oxide breakdown voltage (V_{BD}) of the MOSFET.

III. ESD DESIGN WINDOW

To achieve effective ESD protection, the ESD protection device should be carefully designed. Fig. 4 shows the ESD design window of an IC [10], which is defined by the power-supply voltage with 10% variation ($1.1 \cdot V_{DD}$) and the gate-oxide breakdown voltage (V_{BD}) of MOSFET. First, the trigger voltage (V_{t1}) and holding voltage (V_h) of ESD protection device must be lower than the gate-oxide breakdown voltage of MOSFET to prevent the internal circuits from damage before the ESD protection device is turned on during ESD stresses. Second, the trigger voltage and holding voltage of the ESD protection device must be higher than the power-supply voltage of the IC to prevent the ESD protection devices from

being mis-triggered under normal circuit operating conditions. Moreover, the turn-on resistance (R_{on}) of ESD protection device should be minimized to reduce the joule heat generated in the ESD protection device and the clamping voltage of the ESD protection device during ESD stresses. In the given 28nm high-k metal-gate CMOS technology of this work, the ESD design window is within 1V ($V_{DD} = 0.9V$) and 5.1V.

IV. PMOS WITH EMBEDDED SCR DEVICE FOR ESD PROTECTION

The PMOS with embedded SCR is used as ESD protection device. The device cross-sectional view of the PMOS with embedded SCR is shown in Fig. 5, where the P-ESD denotes the p-type ESD implantation [11]. This implantation was typically used to improve the turn-on ability of ESD protection NMOS. The SCR path consists of P+, N-well, P-ESD, and N+. The equivalent circuit of the SCR consists of a PNP BJT and a NPN BJT. The PNP is formed by the P+, N-well, and P-ESD, and the NPN is formed by the N-well, P-ESD, and N+. The P-ESD layer at anode side is used to enlarge the SCR path. At cathode side, the silicide blocking is used between N+ and P+. Beside, the P-ESD layer at cathode side is used to isolate the N-well and N+ region. As ESD zapping from anode to cathode, the positive-feedback regenerative mechanism of PNP and NPN results in the SCR device highly conductive to make SCR very robust against ESD stresses.

To reduce the trigger voltage of an SCR device, the trigger current can be sent into the base terminal of NPN in the SCR device. The trigger current is inversely related to the trigger voltage of the SCR device; therefore, some trigger techniques have been reported [7]. To investigate the relationship between the trigger current and the trigger voltage, the trigger pad is connected to the PMOS device with embedded SCR, as shown in Fig. 5.

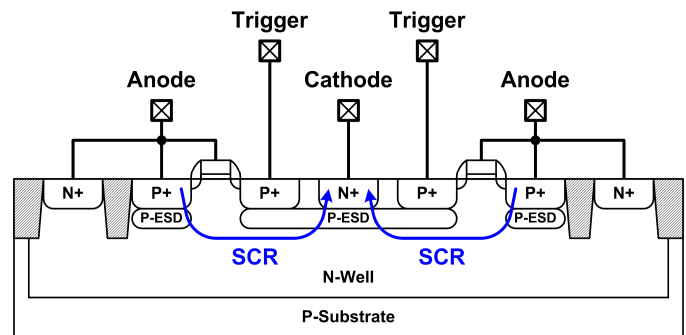


Fig. 5. Cross-sectional view of PMOS with embedded SCR device.

V. VERIFICATION IN SILICON

To verify the PMOS with embedded SCR device in silicon chip, a 28nm high-k metal-gate CMOS process is used in this work. The widths of the test devices are selected to be 120μm and 360μm.

A. ESD Robustness

The HBM ESD robustness is tested according to the ESDA/JEDEC joint standard [12]. The ESD energy is stressed from anode to cathode of the test devices. The trigger pad is kept floating during ESD tests. The failure criterion is defined as the I-V curve seen between test pads shifting over 30% from its original curve after ESD stressed at every ESD test level. According to the measurement results, the PMOS with embedded SCR with 120 μm and 360 μm widths can pass 5kV and 8kV HBM ESD tests, respectively.

B. TLP I-V Characteristics

The TLP system with 10ns rise time and 100ns pulse width is used to evaluate the trigger voltage (V_{ti}), holding voltage (V_h), turn-on resistance (R_{on}), and secondary breakdown current (I_{t2}) of the test devices in the time domain of HBM ESD event. The ratio between HBM ESD robustness and I_{t2} is typically 1.5k Ω , because the peak HBM current is assumed to be equal to the HBM pre-charge voltage divided by 1.5 k Ω [13]. The TLP-measured I-V curves of the test devices without additional trigger current are shown in Fig. 6. The test devices with 120 μm and 360 μm widths can be triggered on at about 4.6V. The trigger voltage is lower than the gate-oxide breakdown voltage. The holding voltages of the test devices are about 1.7V, which is higher than the power-supply voltage and safe from the latchup issue. All measured characteristics of the test devices are listed in Table I.

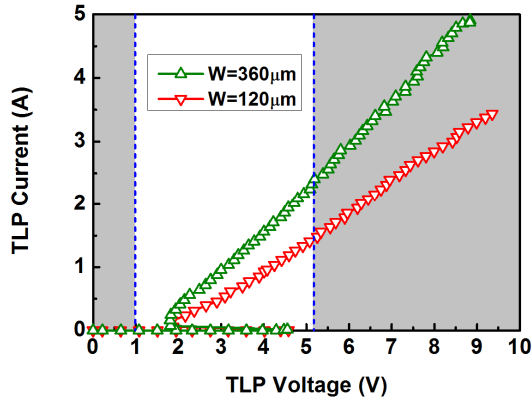


Fig. 6. Measured TLP I-V curves.

Table I
Summary on Measurement Results

Width	PMOS with Embedded SCR	
	120 μm	360 μm
HBM ESD Robustness	5kV	8kV
TLP V_{ti}	4.58V	4.55V
TLP V_h	1.66V	1.74V
TLP R_{on}	4.2 Ω	1.5 Ω

C. Trigger Mechanism

The dc trigger current (I_{trig}) was injected into the trigger pad of the test devices, as measuring the TLP I-V curves. Fig. 7 shows the TLP-measured I-V curves of the test device with 120 μm width under different trigger currents. According to the measurement results, the trigger voltage of the test device can be further reduced with the larger trigger current. If the trigger current is continually increased, the trigger voltage of the proposed device will be reduced to a value close to its holding voltage. Besides, the trigger current will not degrade the holding voltage, and turn-on resistance of the test device.

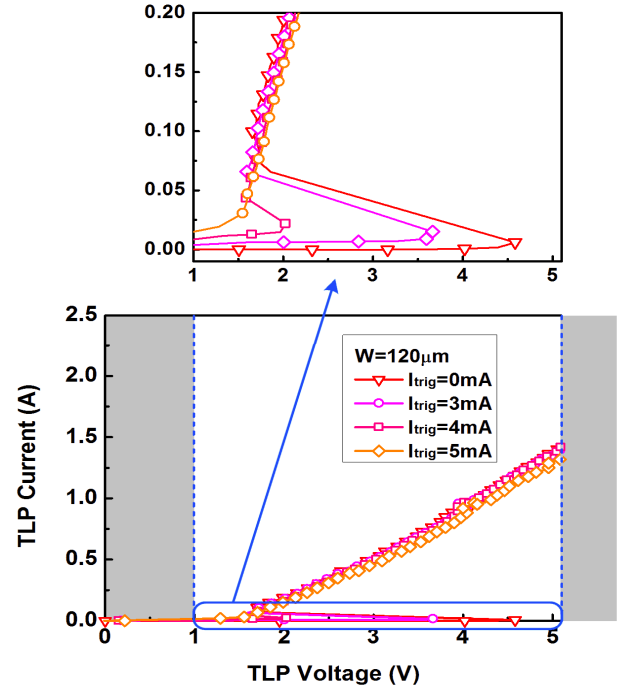


Fig. 7. Measured TLP I-V curves of test device with 120 μm width under different trigger currents.

D. Transient-Induced Latchup (TLU) Test

If the ESD protection device is used between V_{DD} and V_{SS} , the latchup immunity should be considered. To evaluate the latchup immunity of the proposed device, the transient-induced latchup (TLU) was tested [14]. A 200pF charging capacitor is used to store the charges as the TLU-triggering source, and then the stored charges are discharged to the test device through the relay. Figs. 8(a) and 8(b) show the measured transient voltage waveforms of the test device with 120 μm width under the TLU tests with charging voltage of +10V and -10V, respectively. Before the TLU tests, the voltage across the test device was 0.9V, which is the V_{DD} voltage in the given CMOS process. During the TLU tests, the measured voltage waveforms are influenced simultaneously by the underdamped sinusoidal voltage. After the TLU tests, the voltage across the test device was returned to 0.9V. From the TLU test results, the test device can immune to the latchup.

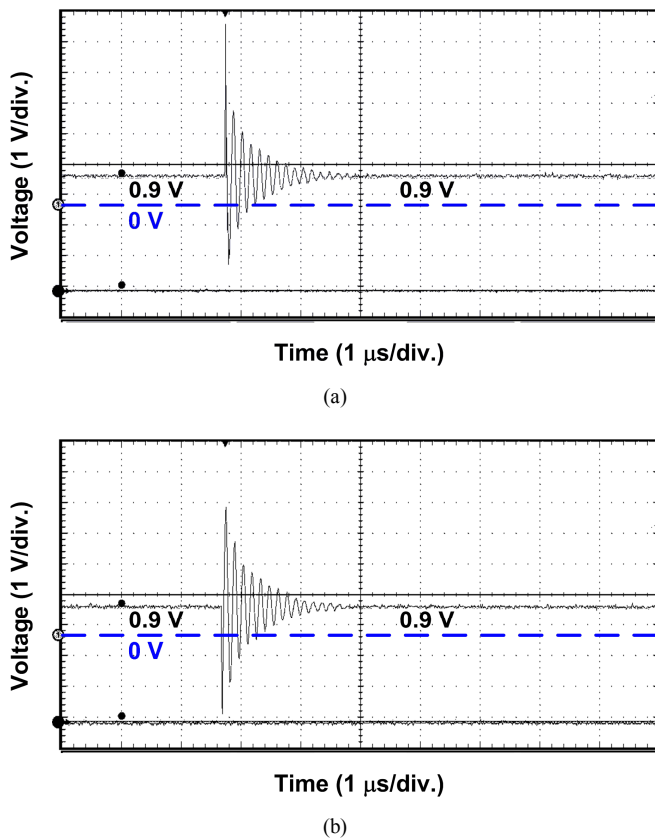


Fig. 8. Measured voltage waveforms on test device with 120 μ m width under TLU tests with charging voltage of (a) +10V and (b) -10V.

VI. CONCLUSION

The ESD protection device of PMOS with embedded SCR has been designed, fabricated, and characterized in a 28nm high-k metal-gate CMOS process. This device combines P+/P-ESD, N-well, P-ESD, and N+ to form the embedded SCR path. Verified in silicon chip, the test device with 120 μ m/360 μ m width has 5kV/8kV HBM ESD robustness, 4.58V/4.55V trigger voltage, 1.66V/1.74V holding voltage, and 4.2 Ω /1.5 Ω turn-on resistance. Besides, the test device has been tested to be free from latchup event. Therefore, the PMOS with embedded SCR can be a better solution for ESD protection in 28nm HKMG CMOS process.

ACKNOWLEDGMENT

This work was supported by Global Unichip Corporation (GUC), Taiwan, by Biomedical Electronics Translational Research Center, National Chiao Tung University, Taiwan, and by Ministry of Science and Technology, Taiwan, under Contract MOST 104-2220-E-009-004, MOST 103-2221-E-009-197-MY2, and MOST 104-2622-E-009-003. The authors would like to thank the employees of GUC for their great help in supporting the joint development project.

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