Whole-Chip ESD Protection Design with SCR for RF Applications in 65-nm CMOS Process

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ABSTRACT

CMOS technology has been used to implement radio-frequency (RF) integrated circuits. On-chip electrostatic discharge (ESD) protection designs must be added at all input/output pads in RF circuits. To minimize the impacts from ESD protection circuit on RF performances, ESD protection circuit at input/output pads must be carefully designed. In this work, a whole-chip ESD protection design with silicon-controlled rectifier (SCR) was proposed. Experimental results in 65-nm CMOS process show that the proposed design can achieve low parasitic capacitance and high ESD robustness.

1. INTRODUCTION

Radio-frequency integrated circuits (RF ICs) have been widely designed and fabricated in CMOS processes due to the advantages of high integration and low cost for mass production. Electrostatic discharge (ESD), which has become one of the most important reliability issues in IC products, must be taken into consideration during the design phase of all ICs, including the RF front-end circuits. In the RF front-end circuits, the RF input/output (I/O) pads are usually connected to the gate terminal or silicided drain/source terminal of the MOSFET, which leads to a very low ESD robustness if no appropriate ESD protection design is applied. Once the RF front-end circuit is damaged by ESD, it can not be recovered and the RF functionality is lost. Therefore, on-chip ESD protection design must be provided for all RF I/O pads [1].

However, ESD protection devices cause RF performance degradation with several undesired effects [2]. Parasitic capacitance is one of the most important design considerations for RF ICs. As shown in Fig. 1, the parasitic capacitance of ESD protection devices causes signal loss from the pad to ground. Moreover, the parasitic capacitance also changes the input/output matching condition. Consequently, RF performance is deteriorated. Therefore, ESD protection circuit must be carefully designed for all RF I/O pads.

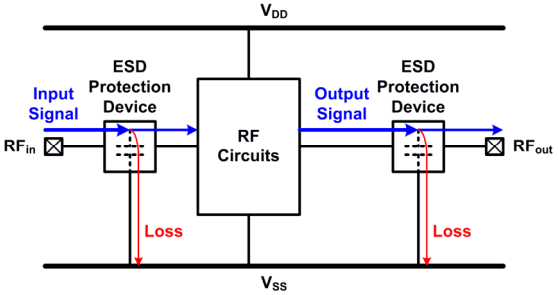

Fig. 1. Signal loss at input and output pads of RF ICs with ESD protection devices.

2. CONVENTIONAL ESD PROTECTION DESIGN

Fig. 2 shows the conventional ESD protection design with dual diodes (D_P and D_N) at RF I/O pad and the power-rail ESD clamp circuit between V_{DD} and V_{SS} [3]. Under positive-to-V_{DD} (PD) or negative-to-V_{SS} (NS) ESD stresses, ESD current is discharged through the forward-biased D_P or D_N. During positive-to-V_{SS} (PS) ESD stress, ESD current is discharged from the RF I/O pad through the forward-biased D_P to V_{DD}, and discharged to the grounded V_{SS} through the power-rail ESD clamp circuit. Similarly, during negative-to-V_{DD} (ND) ESD stress, ESD current is discharged from the V_{DD} through the power-rail ESD clamp circuit and the forward-biased D_N to the RF I/O pad. The parasitic capacitances of the ESD protection diodes are directly contributed at the RF I/O pad, which may be too large to be tolerated for the RF circuits.

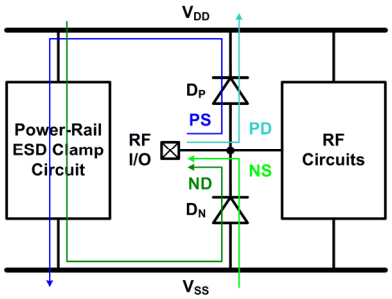

Fig. 2. Conventional ESD protection design.

3. PROPOSED ESD PROTECTION DESIGN

The silicon-controlled rectifier (SCR) device has been reported to be useful for ESD protection with low turn-on resistance, low parasitic effects, and high ESD robustness [4]. A novel design with dual SCR is presented for effective on-chip RF ESD protection, as shown in Fig. 3. Fig. 3 also shows the current discharging paths under PS, PD, NS, and ND ESD stresses.

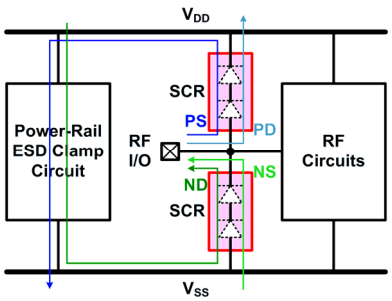

Fig. 3. Proposed ESD protection design.

Fig. 4 shows the cross-sectional view of the SCR device, which consists of P+, N-well, P-well, and N+. The deep N-well structure is used to isolate the P-well region from the common P-substrate. In the beginning of ESD stress, the parasitic diodes (P+/N-well and P-well/N+) in SCR will turn on to discharge the initial current, and then the SCR will take over to discharge the primary current. The parasitic diodes also play the role of trigger circuit of SCR, because the current drawn from N-well (injected into P-well) can also trigger the SCR [4].

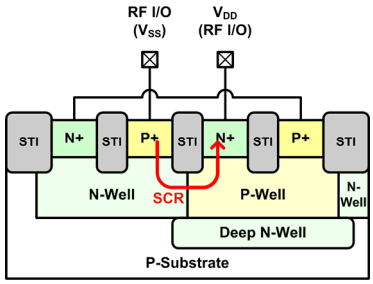

Fig. 4. Cross-sectional view of SCR device.

4. Experimental Results

The test devices of D_P, D_N and SCR have been fabricated in a 65-nm CMOS process. All devices with single finger of W=20μm and W=40μm are implemented for comparison. To facilitate two-port measurement on a probe station, the test devices are arranged with ground-signal-ground (GSG) pads.

4.1 Parasitic Capacitance

The two-port S-parameters of the test devices are measured on wafer. The parasitic effects of the GSG pads and metal routing have been removed by using the de-embedding technique [5]. The parasitic capacitance of each test device was extracted from the S-parameters. Fig. 5 shows the extracted parasitic capacitances of the test devices.

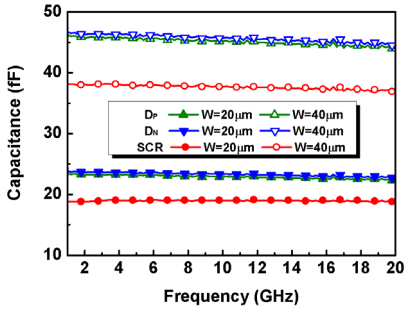

Fig. 5. Measured parasitic capacitances.

4.2 ESD Robustness

The human-body-model (HBM) ESD robustness of the test devices are evaluated by the ESD tester. All these measured ESD robustness are listed in Table I.

To investigate the turn-on behavior and the I-V characteristics in high-current regions of the test devices, the transmission-line-pulsing (TLP) system is used to measure the I-V characteristics, as shown in Fig. 6.

The ratios of HBM ESD robustness and parasitic capacitance (HBM/C) of the test devices are compared, as shown in Table I. The HBM/C ratios of SCR are increased, as compared with those of the diodes. Therefore, the proposed design with SCR is more suitable for ESD protection due to its low parasitic capacitance and high ESD robustness.

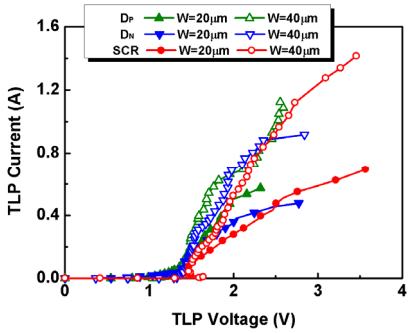

Fig. 6. Measured TLP I-V curves.

5. Conclusion

The novel ESD protection design with SCR has been designed, fabricated, and characterized in a 65-nm CMOS process. Experimental results show that SCR can improve the ESD robustness and reduce the parasitic capacitance. Therefore, the proposed design is more suitable for RF ESD protection.

Table I. Device dimensions and measurement results.

Test Device	W (μm)	C (fF)	HBM (kV)	HBM / C (V/fF)
D_P	20	23.3	0.75	32.2
	40	45.9	1.5	32.7
D_N	20	23.7	0.75	31.6
	40	46.4	1.5	32.3
SCR	20	18.9	1	52.9
	40	38.0	2	52.6

Acknowledgments

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