The Application of Transmission-Line-Pulsing Technique On Electrostatic Discharge Protection Devices

Tung-Yang Chen, Ming-Dou Ker*, and Chung-Yu Wu

Integrated Circuits & System Laboratory
Institute of Electronics
National Chiao-Tung University
Hsinchu, Taiwan, R.O.C.

*VLSI Design Division
Computer &Communicatins Reseach Laboratories
Industrial Technology Research Institute
Hsinchu, Taiwan, R.O.C.

Abstract - In the advanced deep-submicron CMOS technology, it is more difficult to prevent damages from the ESD (*Electrostatic Discharge*) stresses. To understand the physical characteristics and ESD robustness of protection devices, a transmission line pulsing generator (TLPG) system had been set up in several companies to measure the secondary breakdown characteristics of the protection devices. The ESD level of ESD protection devices in CMOS IC's is linearly dependent on the secondary breakdown current (It_2) of the ESD protection devices. The TLPG system is therefore used to measure and analyze the secondary breakdown characteristics of ESD protection devices. Based on the understanding on the secondary breakdown characteristics of the protection devices, some circuit techniques can be developed to improve the protection efficiency of the on-chip ESD protection circuits in the deep-submicron CMOS technologies.

Keywords – ESD, Transmission Line Pulsing Generator, Secondary Breakdown, Human Body Model.

I. INTRODUCTION

In the advanced deep-submicron CMOS technology, some process techniques such as LDD (*Lightly Doped Drain*) and salicide (*Self-Aligned Silicide*) diffusion cause serious degradation on the ESD robustness of CMOS IC's. All IC's should have a reasonable ESD reliability. Some techniques have been developed to improve ESD level of IC's in CMOS technologies, such as the use of silicide blocking mask, ESD implant mask [1], and LVTSCR (*Low-Voltage Trigger SCR*) device [2], [3].

To verify the robustness of ESD protection device, a TLPG (*Transmission Line Pulsing Generator*) system has been set up to measure the secondary breakdown characteristics of those devices. The ESD robustness of the devices is theoretically proportional to the secondary breakdown current (It_2) of the devices.

In this paper, the setup of a TLPG system is explained in more detail, including the generation of a transmission-line pulse.

II. It_2 VERSUS ESD ROBUSTNESS

A. Secondary Breakdown

Even before 1958, some mysterious failures in power transistors were causing considerable concern. These phenomena were often accompanied by collector-emitter short circuits. The use of transistors and other junction devices is often limited by the phenomenon commonly called as "secondary breakdown" [4]. It appears to all junction devices [5]. Secondary breakdown is a transition to a state of higher conductance in a reverse-biased avalanching semiconductor junction device [6], [7]. The secondary breakdown starts when the temperature in the junction locally reaches a critical value [8]. Then, an intrinsic conducting region is established through the space charge region.

The I-V characteristics of a diode and an NMOS device are shown in Fig.1(a) and 1(b), respectively. At the initiation of secondary breakdown, the current constricts the producing high local power dissipation. Therefore, the thermally generated current will produce the necessary voltage decreases.

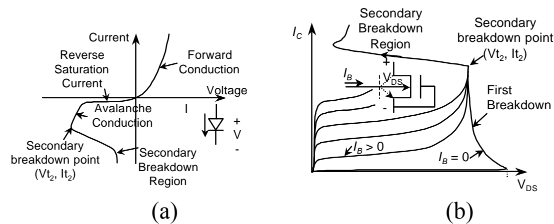


Fig.1 The I-V characteristics of (a) the diode, and (b) the gate-grounded NMOS.

The occurrence of secondary breakdown may cause observable damage to the devices. Junction-heating considerations and heat convection ability of the transistors or diodes usually determine the maximum operating currents. More devices of ESD protection circuits have to be operated below the region of the secondary breakdown. It is possible to utilize their capabilities adequately in this region. The specification of maximum safe operating condition has become increasingly important. The secondary breakdown point (Vt_2, It_2) is defined at the initial point of the maximum operating current region such as that shown in Fig.1. The more maximum current It_2 leads to the higher robustness of ESD protection devices.

B. Human Body Model (HBM)

Human body electrostatic discharge is the most likely cause of ESD events. Walking, scuffing one's shoes on the floor, or shifting around in a chair can build up a charge on the human body, which acts like a capacitor storing energy. The discharge of this energy

through the finger, hand, or through a metal tool held in the hand can zip a device and destroy it. An actual ESD current waveform from the human through a hand-held metallic object is shown in Fig.2 [9].

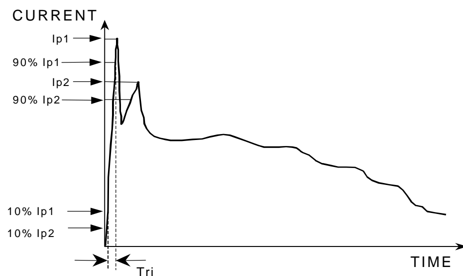
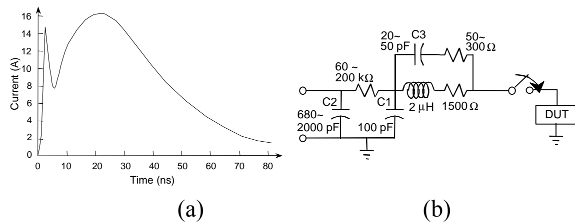


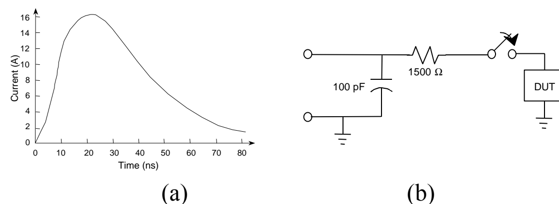
Fig.2 Actual ESD current waveform from the human through a hand-held metallic object.

A model of the human body discharge, which gave a simple double exponential pulse of energy in the discharge, had been defined. The typical current waveform produced by this simulator is shown in Fig.3(a), while the equivalent circuit is shown in Fig.3(b). The inductance and the capacitance C3 represent the components of the arm and hand, and the split capacitance C1 and C2 are those associated with the lower and upper body [10]. This mono-polar pulse and the equivalent circuit are shown in Fig.4(a) and 4(b), respectively.



(a) (b)

Fig.3 (a) Complete ESD current waveform, and (b) the complete human body ESD model.



(a) (b)

Fig.4 (a) Simple ESD current waveform, and (b) the 1st order ESD model.

The HBM is the principal ESD test method used in industry today, which has been specified in the MIL-STD 883C method 3015.7 [11]. The test method attempts to reproduce the ESD waveform generated by the discharge of a human through a low impedance path. A typical waveform of HBM ESD is shown in Fig.5, which has a rise time (*Tri*) of < 10 ns and a decay time (*Tdi*) of about 150 ns. The current pulse is generated by the discharge of a 100-pF capacitor through a 1.5-kΩ resistor into the device under test (DUT). The rise time of the pulse translates from a regulated high voltage supply and the classification test circuit is shown in Fig.6.

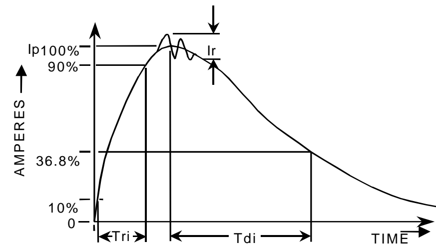


Fig.5 Definition of ESD test circuit current waveform in the human body model.

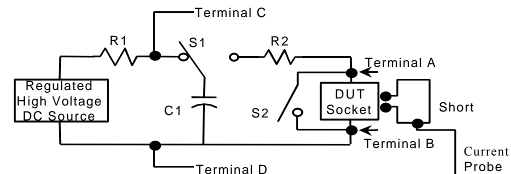


Fig.6 Test circuit for ESD classification in the human body model.

C. The Relationship between It_2 and the HBM ESD Level

The *KeyTek ZapMaster* ESD simulator has been widely used to evaluate the ESD robustness of IC products. On the other hand, we have set up a pulsing generator to simulate the ESD pulse and to measure the It_2. In this paper, a transmission line pulsing generator (TLPG) system [12]-[15] is set up to measure the It_2.

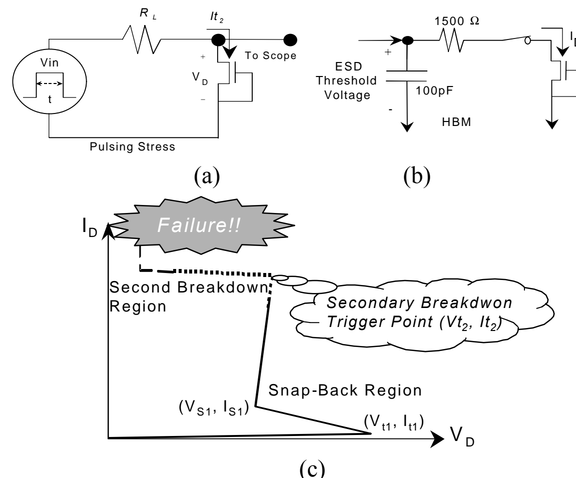


Fig.7 The relation between the It_2 and the ESD level of the device.

In Fig.7(a), it is the equivalent circuit of a TLPG measurement system. The It_2 can be monitored from the scope through a current probe, and it is the same as the I_D in the HBM test of Fig.7(b). The schematic snapback breakdown and secondary breakdown characteristics of the gate-grounded NMOS device is shown in Fig.7(c). Ideally, the HBM ESD threshold

voltage should be related to the pulsed secondary breakdown current (It_2) with the following relation:

$$V_{ESD}=(1500\Omega+R_{device}) \times It_2, \qquad (1)$$

where the 1500 Ω is the series resistance in the HBM ESD model and the R_{device} is the equivalent device resistance under secondary breakdown. Generally, the R_{device} is much smaller than 1500Ω. Some papers had reported that the package-level HBM ESD failure voltage has a rough relationship as the product of 1500Ω and the device It_2 [16].

III. TRANSMISSION LINE PULSING GENERATOR

A. Basic Principle of TLPG Technique

The basic configuration of the wafer-level TLPG is shown in Fig.8. From the illustration, the circuit can be simplified as shown in Fig.9 and divided as two parts of the draw.

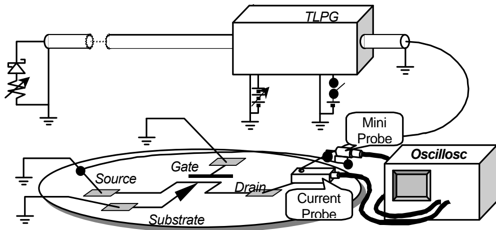


Fig.8 The basic configuration of the wafer-level TLPG.

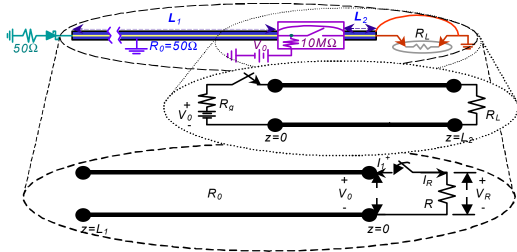


Fig.9 The illustration of basic principle of the wafer-level transmission line pulsing generator.

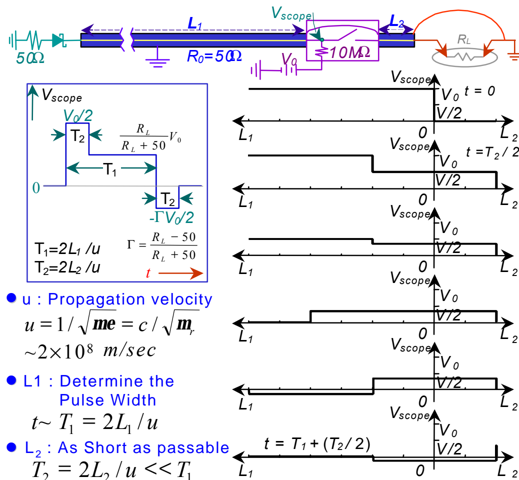


Fig.10 The pulse width calculation of the TLPG.

From the transient principles of transmission line, the pulse of TLPG can be investigated and characterized. The device on the wafer can be contacted by the coaxial probes. The ground returning from the coaxial probe should be shield by a wire loop as short as possible. Only the section of line L_1 in Fig.10 is charged. If the scope probe is located with a reflection from the line L_2 in Fig.10, the waveform is changed by the usual voltage-divider relation which appropriate to device resistance R_L.

In the right hand of Fig.10, it shows the position-voltage diagrams from $t = 0$ to $t = T_1 + (T_2/2)$. The voltage waveform of V_{scope} in the time domain is shown in the left hand of Fig.10.

B. Setup of TLPG

The basic configuration for wafer-level TLPG testing on an NMOS is shown in Fig.8. Four standard 50Ω coaxial probes are used to contact the four terminals of the MOSFET device. The positive TLPG pulse is applied to the drain of the MOSFET, while the other three terminals are held at 0V. The gate, the source, and the substrate probe manipulators don't require any modification. The drain probe manipulator, through which the TLPG pulse is applied, must be modified and dedicated to TLPG testing.

In order to measure the true V_{DUT} and I_{DUT} waveforms as accurate as possible, the sensing units are placed to the DUT as near as possible. For current sensing, a *Tektronix CT1* inductive pickup current transformer is used. The transformer contains a small hole, through which the current carrying conductor is passed. We had very good results by simply passing the probe needle through the hole in this sensing unit. Note that there is a small loop of wire connecting the source probe needle to the coaxial shield on the drain probe cable.

1) Polarized Termination

The series diode-resistor setup used for terminating negative reflections at the back end of the transmission line is easily constructed. A high power Schottky diode and a 50Ω power resistor are assembled in a small box as shown in Fig.11. This box is also used to tie the coaxial cables from the gate, source, and p-substrate probes to ground. A pair of BNC tees is used for this purpose.

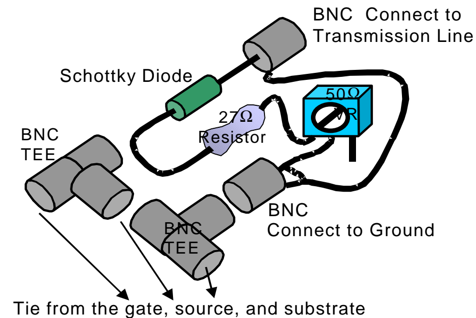


Fig.11 The illustration of the polarized termination for the TLPG.

2) Transmission Line

A charged 50Ω coaxial cable is used to generate a short pulse (3 nanosecond per foot of cable) to a device. Using a charged transmission line is conceptually similar to the more common practice of using a charged capacitor for ESD simulation. But, the charged capacitor and a DUT produce an *R-C* waveform, which is often disturbed by the parasitic elements (notably when device resistance is low). The distributed *L-C* elements of a transmission line produce a pulsed voltage source with impedance equal to the line impedance ($\sqrt{L/C}$), resulting in the simple and easily interpreted waveform. A polarized matched load at the opposite end of the line suppresses the unwanted reflections from the low resistance devices. When the negative reflected pulse from the device reaches the opposite end of the line, the diode forward biases and the 50Ω-terminated resistor absorbs the reflected pulse.

3) TLPG Control Box

As shown in Fig.12, the TLPG control box contains a mercury wetted reed relay, a 10MΩ power resistor, and the required interconnections. The dimensions of this aluminum RFI/EMI shielded box were chosen such that it could be easily mounted on the probe manipulator base.

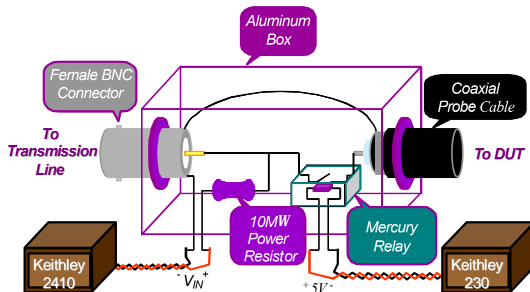


Fig.12 The illustration of the control box in the TLPG.

The transmission line cable of the line L_1 in Fig.9 is attached to the female BNC connector shown on the left side of the Fig.12. The coaxial cable of the line L_2 in Fig.9 from the drain probe is cut as short as possible and hard-wired into the box. Twisted pair wires from external power supplies are also fed into the box to charge the transmission line and to control the switch of mercury relay. The positive lead from the extend supply (*Keithley 2410*) connects to the transmission line through a resistor R of 10MΩ, while the ground lead is tied to a handy shield post on the BNC connector. A mercury wetted reed relay is controlled by another supply (*Keithley 230*) to perform a clean and bounce-free switching. The quality of this relay has the most important factor to affect the rise time of the TLPG pulse. A *CP Clare* 5V, 4-pin, single-pole, normally-open relay is used and connected as shown in Fig.12. The relay is closed by forcing the supply to 5V. A small loop of wire is used to connect the ground shields of the two coaxial cables. When the relay is closed, the limited energy stored in the TLPG is discharged to the DUT.

4) Power Supplies

The *Keithley 230* and *2410* programmable voltage sources are used in the TLPG system. These power supplies are capable of +/- 100V and +/- 1100V DC output and include 100 step programmable memory buffers.

The power supply for charging the transmission line is connected as shown in Fig.12. Before applying a pulse to the DUT, the desired V_{IN} is simply entered on the front keypad of the *Keithley 2410*. In theory, the maximum V_{IN} for the TLPG should be limited by the dielectric strength of the cable and switch, as well as the diode reverse breakdown voltage at the termination end.

The mercury wetted reed relay is controlled by the *Keithley 230* voltage source. As shown in Fig.12, this supply provides the 5V-voltage waveform to close the relay. Once the transmission line power supply is set to the desired level, the relay can be fired to zap the DUT. The relay is handy to control with the following three-step program entered into the 30 memory buffers. This program forces the supply to 0V for 10ms, then 5V for 3ms, and finally back to 0V for 20ms. This program works greatly for controlling the relay. It can be run in the continuous mode to repeatedly zap to DUT.

5) DUT Probe and Measure System

Moving out to a slightly larger scale, Fig.13 shows the configuration of the modified drain probe manipulator. The aluminum TLPG control box, which has been discussed in the ‘TLPG Control Box’ Section, is placed at the base of the manipulator. This box is strapped to the manipulator with rubber bands. The coaxial probe cable exits the TLPG control box and connects as usual to the tungsten probe needle. The *Tektronix CT1* current transformer is strapped beneath the end of the probe support arm. The probe needle is bent slightly and passed through the small hole in this transformer. A BNC cable connects the current sensing transformer to the oscilloscope to monitor the current waveform in the time domain.

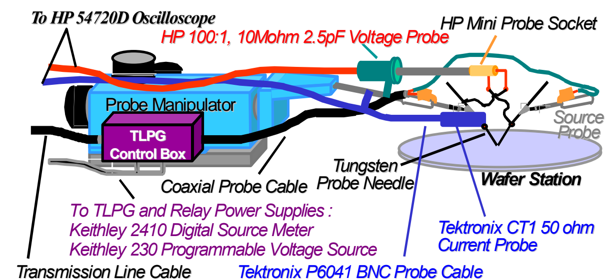


Fig.13 The illustration for the DUT probe and measure system of the wafer-level TLPG.

A *Hewlett Packard (HP) HP10440A* 100:1, 10MΩ, 2.5pF, *miniature voltage probe* is strapped above the support arm of the probe needle. This probe plugs into an *HP mini-probe socket* as shown in Fig.13. Two short wire loops connect this socket to the source and drain probe needles as near as possible to sense the voltage across the DUT. These wires had to be brazed to stick to the tungsten needles.

IV. EXPERIMENTAL RESULTS

To verify the pulse of the TLPG, the 100Ω and 50Ω load resistors are used as the DUT's. A transmission line with a length of 10 meters is charged with 100 V to measure the I-V waveforms from the TLPG. The measured pulses are shown in Fig.14(a) and 14(b). Because of the transmission line length is 10m, the pulse width will be $T_1 = 2L_1/(2X10^8)$ sec = 100 nanosecond. It is clearly shown that there is a reflection waveform after 100ns as shown in Fig.14(a) with a 100Ω DUT. It is owing to the Γ_R is greater than zero. In Fig.14(b) with a 50Ω DUT, there is no reflection waveform after 100ns. So, the phenomenon matches to the theory. This has verified the successful setup of this TLPG system.

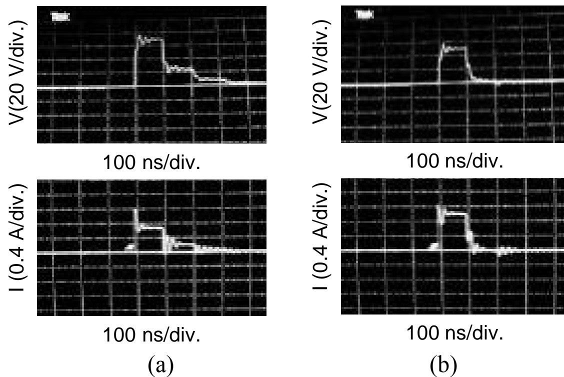


Fig.14 The measured TLPG waveforms for I-V characteristics of (a) 100Ω and (b) 50Ω resistors with 10-meters transmission line and 100V power supply.

By using the TLPG system, the protection devices can be measured by changing the power supply voltage. Using a 15m-length transmission line to measure the ESD protection devices, some measured pulses are shown in Fig.15-Fig.17. Because the *HP10440A* 100:1 miniature voltage probe is used, the actual voltage will be 100 times of the measured voltage on the scope. Because the *Tektronix CT1* current transformer can transform 5 mV per mA, the actual current is the "measured voltage" of current wave divided by 5mV/mA. In Fig.15, the device is under the snapback region. In Fig.16, the current pulse increases abruptly and the voltage curve decreases abruptly at the same time point, where the device enters into the secondary breakdown point. When the device is in the secondary breakdown region, the voltage and current waveforms are shown in Fig.17.

To verify the I-V characteristics of device, the It_2 of a lateral bipolar device in a 0.6-μm CMOS technology is measured by the TLPG. The measured I-V characteristics of the device in the snapback breakdown region is shown in Fig.18.

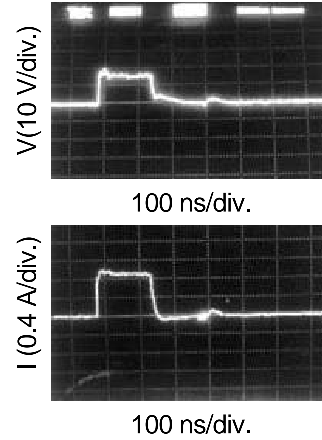


Fig.15 The TLPG-measured voltage waveform and current waveform when the device is in the snapback region.

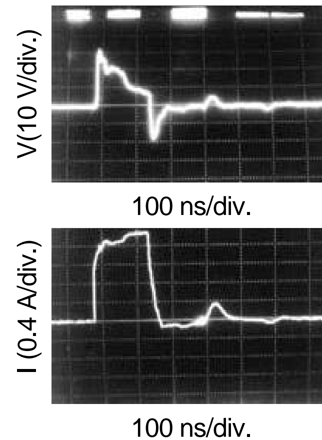


Fig.16 The TLPG-measured voltage waveform and current waveform when the device is just on the secondary breakdown point.

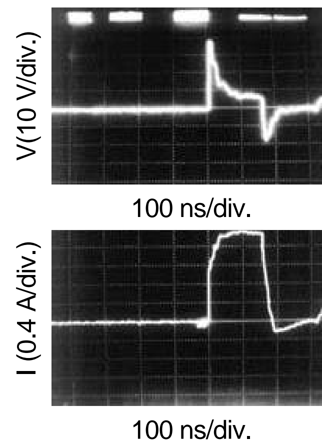


Fig.17 The TLPG-measured voltage waveform and current waveform when the device is in the secondary breakdown region.

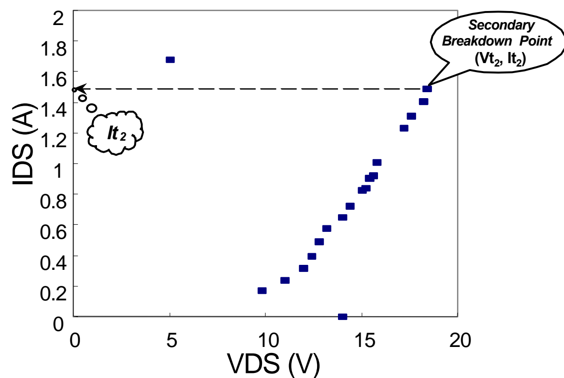


Fig.18 The snapback I-V curve of an ESD protection device, which is measured by using TLPG system.

The secondary breakdown current (It_2) of the protection device is also measured by the TLPG system. When the ESD-stress current on the input pad is greater than the It_2 of the ESD protection device, the input ESD protection device is permanently damaged by the overstress current. Adjusting the device dimension of the protection device, the It_2 can be proportionally increased. Thus, the ESD robustness of ESD protection circuit can be adjusted by the device dimension. The dependence of ESD level on the It_2 of the ESD protection device is shown in Fig.19.

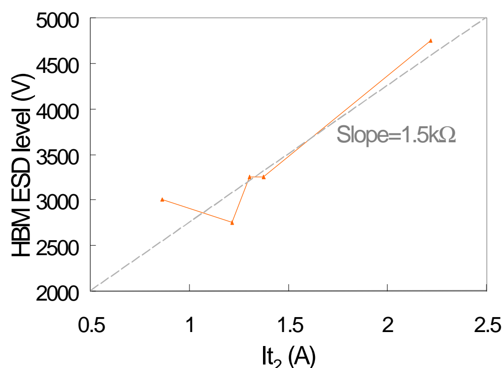


Fig.19 Dependence of the HBM ESD level on the It_2 of the ESD protection device.

V. CONCLUSION

The setup of a TLPG system has been well explained and demonstrated. An energy-limited square pulse can be generated by this TLPG system, and its pulse width can be adjusted by the length of the transmission line. By using the TLPG system, the secondary breakdown characteristics of the ESD protection devices can be clearly analyzed. Dependent on the measure results using the TLPG system, the relation between the It_2 and the ESD level has been proved as a linear function. The secondary-breakdown characteristics of devices are the major reference for the ESD robustness of protection devices. To design high performance ESD protection circuits, the use of the protection devices with high secondary breakdown current is the major key. By the way, the characteristics of the protection devices with new structures can be clearly investigated. The application of using new protection devices can be developed to improve ESD robustness of ESD protection circuits. So, the TLPG system is a good analysis tool for the design of ESD protection circuits.

REFERENCE

[1] S. Daniel and G. Krieger, "Process and design optimization for advanced CMOS I/O ESD protection devices," *EOS/ESD Symposium Proceedings*, EOS-12, pp. 206-213, 1990.

[2] A. Chatterjee, T. Polgreen, "A low-voltage triggering SCR for on-chip ESD protection at output and input pads," *IEEE Electron Device Letters*, Vol. 12, pp. 21-22, 1991.

[3] M.-D. Ker, C.-Y. Wu, H.-H. Chang, T. Cheng, and T.-S. Wu, "Complementary-LVTSCR ESD protection scheme for submicron CMOS IC's," *1995 IEEE symposium on Circuits and Systems*, Vol. 2, pp. 833-836, 1995.

[4] H. A. Schafft, "Second breakdown -- A comprehensive review," *Proceedings of The IEEE*, Vol. 55, No. 8, August 1967.

[5] H. A. Schafft and J. C. French, "Second breakdown in transistors," *IRE Trans, Electron Devices*, Vol. ED-9, pp. 129-136, March 1962.

[6] P. L. Hower and V. Gopala Krishna Reddi, "Avalanche injection and second breakdown in transistors," *IEEE Transactions on Electron Devices*, Vol. ED-17, No. 4, April 1970.

[7] W. B. Smith, D. H. Pontius, and P. P. Budenstein, "Second breakdown and damage in junction devices," *IEEE Transactions on Electron Devices*, Vol. ED-20, No. 8, pp. 731-744, Aug. 1973.

[8] G. M. Ford, "Collector to emitter breakdown related to thermal runaway in homogeneous base germanium power transistors," *Solid State Design*, Vol. 4, pp. 29-36, June 1963.

[9] "American National Standard guide for electrostatic discharge test methodologies and criteria for electronic equipment," *Accredited Standards Committee on Electromagnetic Compatibility*, C63, USA.

[10] L. van Roozendal, A. Amerasekera, P. Bos, W. Baelde, F. Bontekoe, P. Kersten, E. Korma, P. Rommers, P. Krys, U. Weber, and P. Ashby, "Standard ESD testing of integrated circuits," *EOS/ESD Symposium Proceedings*, EOS-12, pp. 119-130, 1990.

[11] MIL-STD-883C method 3015.7, Military Standard Test Methods and Proc. For Microelectronics, Dept. of Defense, Washington, D. C., U.S.A., 1989.

[12] T. J. Maloney and N. Khurana, "Transmission line pulsing techniques for circuit modeling of ESD phenomena," *EOS/ESD Symposium Proceedings*, EOS-7, pp. 49-54, 1985.

[13] J. Blankenagel, "A high voltage pulse generator for ESD simulation," *EOS/ESD Symposium Proceedings*, EOS-11, pp. 50-54, 1989.

[14] N. Khurana, T. Maloney, W. Yeh, "ESD on CHMOS devices - equivalent circuits, physical models and failure mechanisms," *IEEE International Reliability Physics Symposium*, pp.212-223, 1985.

[15] R. A. Ahton, "Modified transmission line pulse system and transistor test structures for the study of ESD," *Proc. IEEE 1995 Int. Conference on Microelectronic Test Structures*, Vol. 8, pp. 127-132, March 1995.

[16] C. H. Dfaz, T. E. Kopley, and P. J. Marcoux, "Building-in ESD/EOS reliability for sub-halfmicron CMOS processes," *IEEE Transactions on Electron Devices*, Vol. 43, No. 6, pp. 991-999, June 1996.