Circuit Performance Degradation of Switched-Capacitor Circuit with Bootstrapped Switch Technique due to Gate-Oxide Overstress in a 130-nm CMOS Process

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ABSTRACT

The effect of MOSFET gate-oxide reliability on MOS switch with bootstrapped technique is investigated with the switched-capacitor circuit in a 130-nm CMOS process. The sample-and-hold amplifier with the open-loop configuration is used to verify the impact of MOS switch gate-oxide reliability on the switched-capacitor circuit. After overstress on the MOS switch of sample-and-hold amplifier, the circuit performances on the time domain and frequency domain have been measured to verify the impact of MOS switch gate-oxide reliability on circuit performance.

1. INTRODUCTION

The switched-capacitor circuit is an important building block in analog integrated circuits, such as analog-to-digital data converter (ADC). The high-speed and high-resolution analog-to-digital data converter needs a high performance switched-capacitor circuit. The low-supply voltage will degrade the performance of the switched-capacitor circuit due to the nonlinear effect of the MOSFET switch such as body effect, turn-on resistance variation, charge injection, and clock feedthrough. The bootstrapped switch [1]-[3] and switched-opamp (switched operational amplifier) techniques [4]-[6] are widely used in low-voltage switched-capacitor circuit. The switched-opamp technique is not suitable for high-speed switched-capacitor circuit, because turning opamp on/off needs much more time than turning switch on/off. The bootstrapped switch technique provided a constant voltage between the gate and source nodes of the MOS switch is used to improve the performances of low-voltage and high-speed switched-capacitor circuit. However, the bootstrapped switch technique induces the gate-oxide overstress on MOS switch [1] to degrade the lifetime of switch device. The suitable device size design of the bootstrapped switch circuit [1] and the thick-oxide MOSFET device [2] can be used to avoid the gate-oxide overstress on the switch device. Therefore, the gate-oxide reliability of MOS switch in the low-voltage and high-speed switched-capacitor circuit with the bootstrapped switch technique is a very important reliability issue.

In this work, the impact of gate-oxide reliability on MOS switch in the switched-capacitor circuit with the bootstrapped technique is investigated with the sample-and-hold amplifier (SHA) in a 130-nm CMOS process [7]. The time-domain and frequency-domain circuit performances of the sample-and-hold amplifier with the open-loop configuration are measured after the gate-oxide overstress on MOS switch.

2. BOOTSTRAPPED SWITCH TECHNIQUE

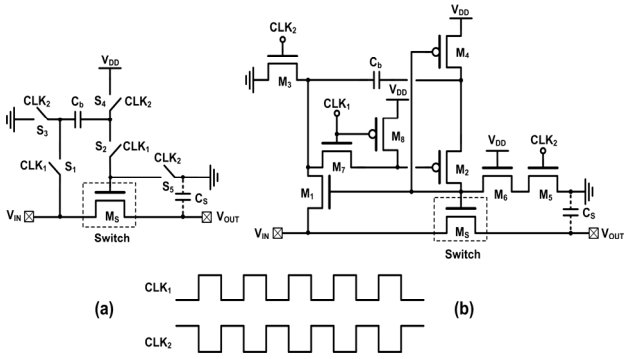


Fig. 1. (a) Conceptual schematic, and (b) detail circuit implementation, of bootstrapped switch technique for switched-capacitor circuit.

The conceptual schematic of the bootstrapped switch technique for switched-capacitor circuit is shown in Fig. 1(a). The basic schematic includes the signal MOS switch M_S, five ideal switches S_1-S_5, and a capacitance C_b. The CLK_1 and CLK_2 clock signals are the out-of-phase signals. When CLK_1 is low and CLK_2 is high, the S_3 and S_4 switches charge the capacitance C_b to the supply voltage V_{DD}, and the S_5 switch is used to turn off the switch device M_S. Then when CLK_1 is high and CLK_2 is low, the S_1 and S_2 switches change the capacitance C_b in series with the input signal V_{IN} and connect to the gate of switch device M_S, such that the gate-to-source voltage across the switch device M_S is equal to the supply voltage V_{DD}. The gate voltage on the switch device M_S will be charged to $V_{IN}+V_{DD}$, which is larger than the supply voltage. The detailed circuit implementation is shown in Fig. 1(b) [8]. The M_1, M_2, M_3, M_4 and M_5 correspond to the five ideal switches S_1-S_5 shown in Fig. 1(a). The M_6 transistor is added to reduce the maximum drain-to-source voltage (V_{DS}) of M_5 transistor to avoid the gate-oxide overstress. The capacitance C_b must be lager to supply charge to the gate of switch device in addition to all parasitic capacitances in the charge path. Otherwise, charge sharing will significantly reduce the boosted voltage. The boosted voltage on the gate of switch device can be expressed as

$$V_g = V_{IN} + \frac{C_b}{C_b + C_p} V_{DD}, \quad (1)$$

where C_p is total parasitic capacitance connected to the top plate of C_b while it is across the main switch device M_S.

The sampling capacitance C_S in the switched-capacitor circuit with the bootstrapped switch technique is usually designed with several pF to improve the circuit performance. The different RC delay times between the sampling network (M_S and C_S) and the bootstrapped network (M_1-M_8 and C_b) will induce the gate-oxide transient overstress across the gate-to-drain nodes of the switch M_S to cause the long-term reliability issue in the switched-capacitor circuit with the bootstrapped switch technique. In order to explain the gate-oxide transient overstress event in switched-capacitor circuit with bootstrapped technique, the sub-sampling switched-capacitor circuit with bootstrapped switch technique can be used to introduce and understand this phenomenon. If the input voltage V_{IN} of bootstrapped switch circuit is biased from ground to supply voltage V_{DD}, the gate voltage of the switch device with the bootstrapped technique is charged to near two times supply voltage to keep the constant voltage, V_{DD}, between the gate and source nodes of switch device. Simultaneously, the drain voltage of switch device will be charged from ground to supply voltage V_{DD}. The simulated waveform of the bootstrapped switch circuit under sub-sampling configuration is shown in Fig. 2. The rise and fall times of the CLK_1 and CLK_2 clock signals are set to 1 nsec, respectively. The rise time of the input signal V_{IN} is also set to 1 nsec, too. The V_G is the gate voltage of switch device M_S. When the input voltage V_{IN} is biased from ground to supply voltage, the equivalent RC delay time from source to drain nodes of switch device is larger than that from source to gate nodes of switch device in the bootstrapped switch circuit. The voltage across the gate-to-drain nodes of switch device is overstressed to degrade the switch device lifetime and the circuit performance of the switched-capacitor circuit with the bootstrapped switch technique during a very short time in sampling mode. Therefore, the long-term gate-oxide reliability in the low-voltage switched-capacitor circuit with the bootstrapped switch technique is a very important reliability issue in the nano-scale CMOS process.

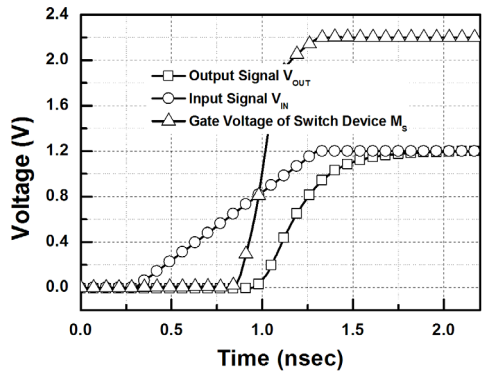


Fig. 2. Simulated waveforms of bootstrapped switch circuit with the gate-oxide transient overstress under sub-sampling configuration.

3. Sample-and-Hold Amplifier with Gate-Oxide Reliability Test Circuit

The switched-capacitor circuit with the bootstrapped technique has a long-term reliability problem, which causes the circuit performance degradation. The overstress voltage on the gate oxide of the switch device depends on the voltages of input and clock signals. The obvious degradation of circuit performance in the switched capacitor circuit with bootstrapped technique needs a long-term operation, which may need many years, to measure the change under the gate-oxide degradation of switch device. In order to accelerate the degradation of circuit performance, the switched-capacitor circuit with the gate-oxide reliability test circuit is proposed in Fig. 3. The sample-and-hold amplifier with the open-loop configuration is used to verify the gate-oxide reliability of the bootstrapped MOS switch. In Fig. 3, the operational amplifier with the folded-cascode structure is used to realize the buffer.

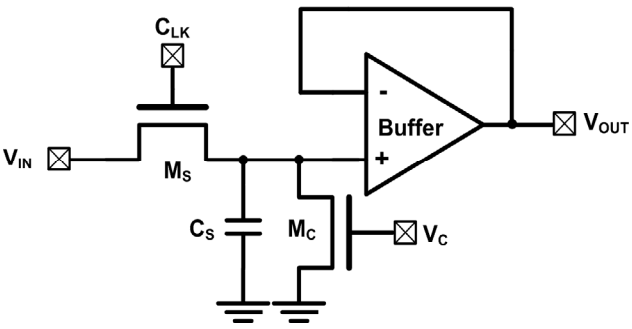


Fig. 3. Complete circuit with the gate-oxide reliability test circuit for switched-capacitor circuit.

The normal operating voltage (V_{DD}) and the gate-oxide thickness (t_{ox}) of all MOSFET devices in the sample-and-hold amplifier with the gate-oxide reliability test circuit are 1.2 V and 2.63 nm, respectively, in a 130-nm CMOS process. The control device M_C is used to control the drain voltage of the switch M_S. The device ratio of the switch M_S is determined by the sampling frequency of the sample-and-hold amplifier. Therefore, the device ratio of the control device M_C should be designed larger than that of the switch M_S. If the device ratio of the control device M_C is smaller than that of the switch M_S, the drain voltage of control device M_C will not be kept at ground. In normal operation, the control voltage V_C is biased to ground, so the control device M_C is turned off. The sample-and-hold amplifier can be successfully operated under the sample and hold modes, respectively. In the gate-oxide overstress test, the control voltage V_C is biased to supply voltage, and the input signal V_{IN} is kept to the supply voltage V_{DD}. The voltage at C_{LK} node can be applied with any voltage level higher than the supply voltage to overstress the gate oxide of switch device. The voltage across the gate-to-drain terminals of the switch M_S is controlled by the C_{LK} voltage. This test circuit can be used to simulate the overstress across the gate-to-drain terminals of switch

M_S in the switched-capacitor circuit with bootstrapped switch technique.

Simulated by HSPICE, signal-to-(noise+distortion) ratio (SNDR) of the sample-and-hold amplifier with the gate-oxide reliability test circuit is 40.1 dB under the 25 MHz square signal (sampling frequency) at C_{LK} node and 2 MHz sinusoid signal at V_{IN} node as shown in Fig. 4. The switched-capacitor circuit with the gate-oxide reliability test circuit has 6 bits resolution under the 25 MHz sampling frequency. The test chip has been fabricated in a 130-nm CMOS process. The normal operating voltage is 1.2 V. The chip micrograph and layout view of the sample-and-hold amplifier with the gate-oxide reliability test circuit is shown in Fig. 5. The occupied silicon area of this test circuit including the two test circuits and ESD (Electrostatic Discharge) protection devices is 390 μm × 390 μm. The ESD protection devices realize with N+ P-well diode to avoid the ESD inducing the gate-oxide damage.

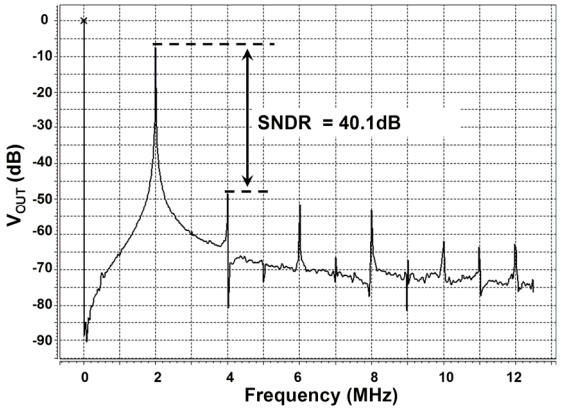


Fig. 4. The simulated SNDR of the sample-and-hold amplifier with the gate-oxide reliability test circuit.

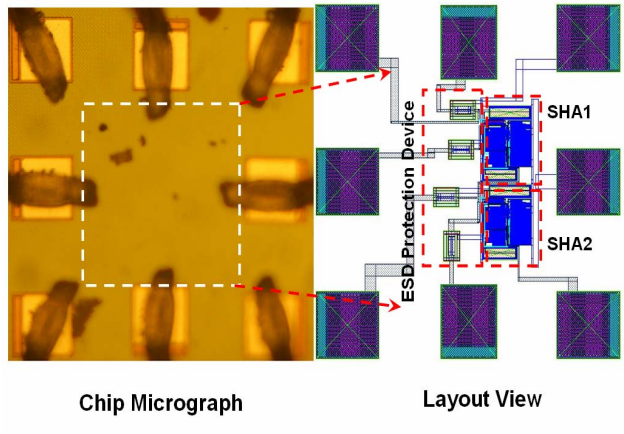


Fig. 5. The chip micrograph and layout view of the sample-and-hold amplifier with the gate-oxide reliability test circuit.

4. Overstress Test Results

When the sample-and-hold amplifier with the gate-oxide test circuit operates in the overstress mode, the input signal, V_{IN}, is biased to supply voltage, the control voltage, V_C, is set to supply voltage, and the C_{LK} node is set to 1.8 V, as shown in Fig. 3. Because the normal operating voltage (supply voltage) is of 1.2 V, the voltage across the gate-to-drain terminal of the witch device will be overstress of 1.8 V. Only the gate-to-drain terminal of the switch device will be overstress to simulate the switched-capacitor circuit with the bootstrap switch technique under the transient gate-oxide stress. The time-domain and frequency-domain waveforms of sample-and-hold amplifier with the gate-oxide test circuit are re-evaluated under this overstress condition.

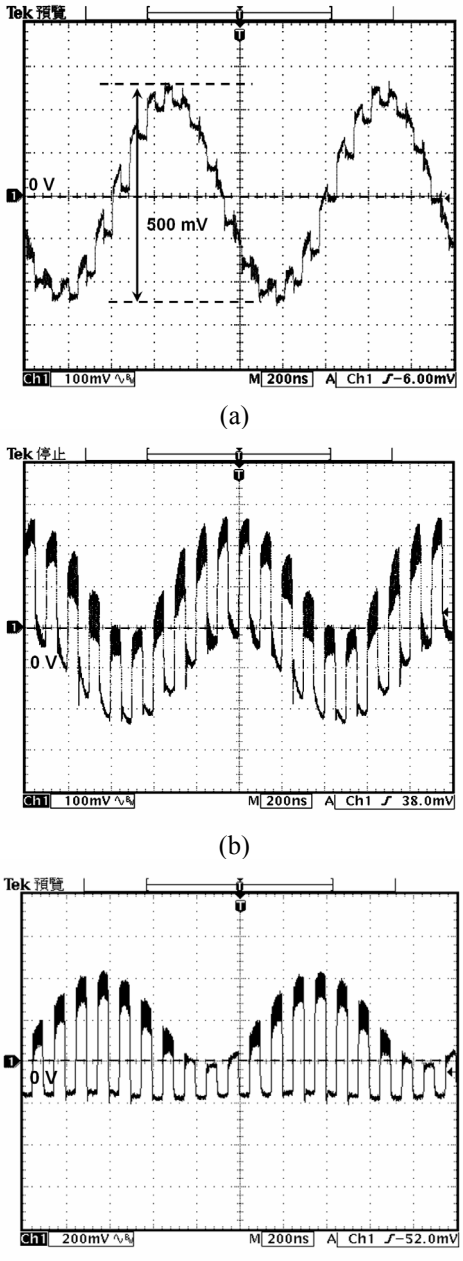
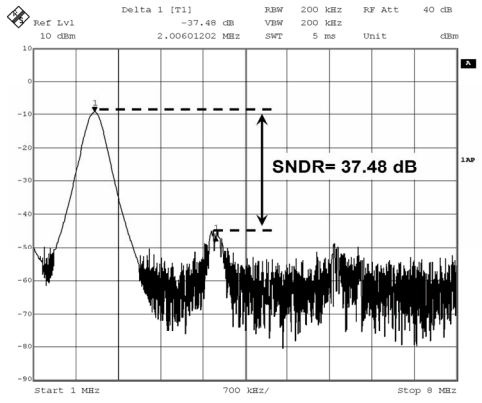
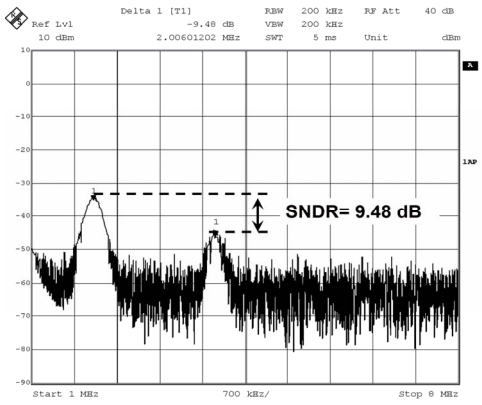


Fig. 6. The measured time-domain waveform of the sample-and-hold amplifier with the gate-oxide reliability test circuit under the different overstress time. (a) overstress time = 0 hour, (b) overstress time = 3 hour, and (c) overstress time = 6 hour.

Figs. 6(a), 6(b), and 6(c) show the time-domain waveform at V_{OUT} node, as shown in Fig. 3, under the different stress time. The gate-oxide breakdown on the gate-to-drain terminal of the switch device degrades the performance of the sample-and-hold amplifier. Because the gate-oxide degradation will induce the leakage current from the drain to gate terminal (gate to drain terminal), the leakage current of the switch device induces that the output voltage on the hold mode is degraded, as shown in Figs. 6(b) and 6(c), under the different stress time. If the gate oxide (gate-to-drain) of the switch device is fully breakdown, the output waveform at V_{OUT} of switched-capacitor circuit will be changed to square waveform due to the large leakage current. Finally, the sample-and-hold amplifier will not be functional work.



(a)



(b)

Fig. 7. The measured frequency-domain waveform of the sample-and-hold amplifier with the gate-oxide reliability test circuit under the different overstress time. (a) overstress time = 0 hour, and (b) overstress time = 6 hour.

Figs. 7(a) and 7(b) show the measured frequency spectrum at output node V_{OUT} of the sample-and-hold amplifier with the gate-oxide reliability test circuit, as shown in Fig. 3, under the different stress time. The SNDR of the sample-and-hold amplifier is degraded with the gate-oxide breakdown of the switch device from 37.48 dB to 9.48 dB. The effective number bits of the sample-and-hold amplifier are reduced by gate-oxide breakdown of the switch device.

5. CONCLUSION

The impact of gate-oxide reliability on switch device in the bootstrapped circuit has been investigated and analyzed with the sample-and-hold amplifier. The time-domain and frequency-domain waveforms of the sample-and-hold amplifier after different tress times have been measured. The gate-oxide overstress across the gate-to-drain terminals of the switch device induces the leakage current to degrade the voltage at V_{OUT} in the hold mode. After the gate-oxide overstress, the performance of the sample-and-hold amplifier is seriously degraded by gate-oxide degradation of MOS switch. The effective number bit of the sample-and-hold amplifier is decreased by gate-oxide degradation of the switch device. The gate-oxide reliability of MOS switch in the switched-capacitor circuit with the bootstrapped technique has been a very important application concern for analog circuits in the nano-scale CMOS processes. The bootstrapped technique designed with thick gate-oxide MOSFET device can overcome this problem. How to design the switched-capacitor circuit with only thin gate-oxide devices is still a challenge to analog circuit designers.

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