(12) UK Patent Application (19) GB (11) 2 304 994 (13) A

(43) Date of A Publication 26.03.1997

(21) Application No 9518233.3

(22) Date of Filing 07.09.1995

(51) INT CL[6]
H01L 27/02

(52) UK CL (Edition O)
H1K KGPE K1BC K1CA K1FL

(56) Documents Cited
EP 0575062 A US 5289334 A US 4139880 A

(58) Field of Search
UK CL (Edition N) H1K KGPE
INT CL[6] H01L 27/02
ONLINE: EDOC WPI JAPIO

(71) Applicant(s)
Winbond Electronics Corporation

(Incorporated in Taiwan)

No 4 Creation Rd 3rd, Science Based Industrial Park, Hsinchu, Taiwan

(72) Inventor(s)
Ming-Dou Ker
Chung-Yu Wu
Tao Cheng
Chau-Neng Wu
Ta-Lee Yu

(74) Agent and/or Address for Service
Urquhart-Dykes & Lord
8th Floor, Tower House, Merrion Way, LEEDS, LS2 8PA, United Kingdom

(54) Capacitor couple electrostatic discharge protection circuit

(57) The present invention is related to a capacitor-couple electrostatic discharge (ESD) protection circuit for protecting an internal circuit and/or an output buffer of an IC from being damaged by an ESD current. The capacitor-couple ESD protection circuit includes an ESD bypass device 223 for bypassing the ESD current, a capacitor-couple circuit 222 for coupling a portion of voltage to the ESD bypass device, and a potential leveling device 224 for keeping an ESD voltage transmitted for the internal circuit at a low potential level. By using the present ESD protection circuit, the snapback breakdown voltage can be lowered to protect the thinner gate oxide of the internal circuit especially in the submicron CMOS technologies.

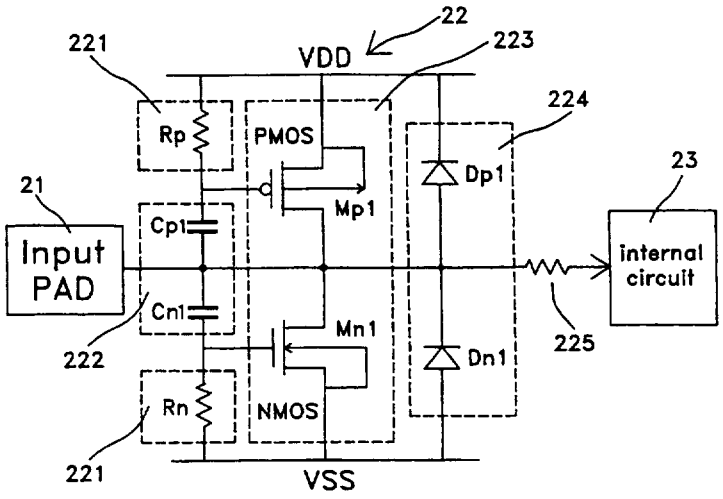

Fig. 2

GB 2 304 994 A