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(58) Field of Search
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(54) MOS transistor

(57) In an electronic device, and more particularly in an MOS transistor, a square-type layout style is used to improve the output driving/sinking capability of output buffers as well as the ESD protection capability of NMOS and PMOS devices in output buffers or input ESD protection circuits within smaller layout area. Both gate (42) and source diffusion (43) are in square loop form. Drain diffusion (41) area and drain-to-bulk parasitic capacitance at the output node are reduced by this square-type layout. Devices using the present layout style can be assembled to form larger, rectangular (or square) and similarly functioning devices. Thus, the present square-type layout style is very attractive to submicron CMOS VLSI/ULSI in high-density and high-speed applications.

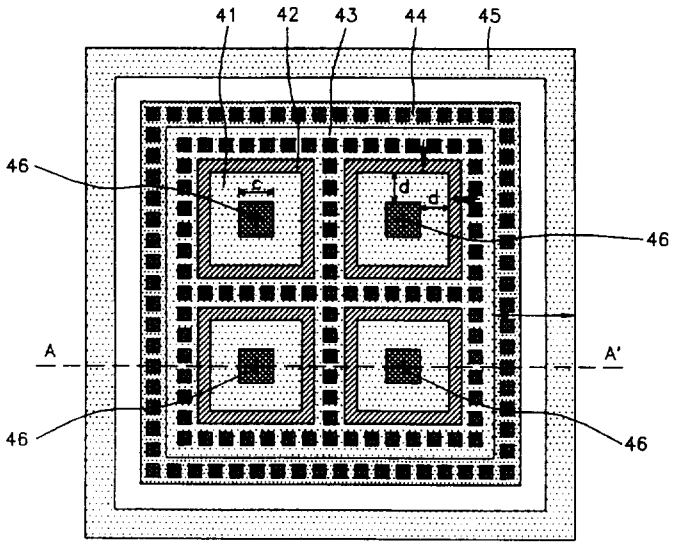

Fig. 4

GB 2 306 770 A