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(54) Abstract Title  
**Substrate-triggering electrostatic discharge protection circuit for deep-submicron integrated circuits**

(57) A substrate-triggering electrostatic discharge (ESD) protection circuit is provided for use on a deep-submicron integrated circuit for ESD protection. The ESD protection circuit is incorporated between an input pad IP and the input stage 10 of the internal circuit 40 of an integrated circuit formed on a substrate, and comprises an NMOS transistor N1 and resistor R1 coupled to ground. The substrate of the transistor N1 is coupled to the substrate of a field oxide device (FOD) F1 also connected between the input pad 10 and ground. The FOD F1 includes a lateral parasitic bipolar junction transistor (LBJT) the base of which is formed from the FOD substrate. ESD stress causes snapback breakdown in transistor N1 which generates substrate current which triggers LBJT and turns on FOD F1 to bypass ESD current to ground, so protecting the gate oxide in the input stage. The FOD F1 may be replaced by a second NMOS transistor. A further embodiment includes two PMOS transistors in addition.

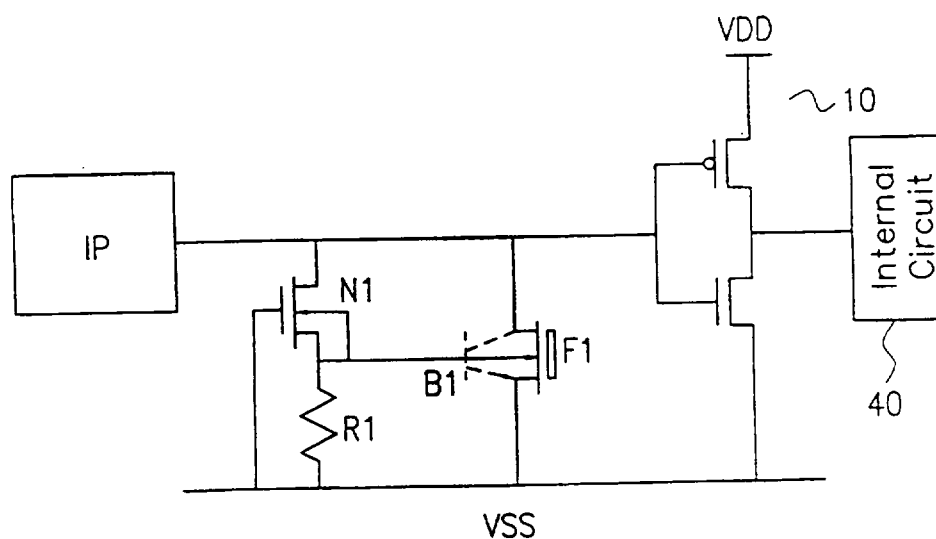


FIG. 4

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