Response to the Comments of Reviewer #1

Manuscript: JSSC #7753

Paper Title: The Impact of Low-Holding-Voltage Issue in High-Voltage CMOS Technology and the Design of Latchup-Free Power-Rail ESD Clamp Circuit for LCD Driver ICs

---

The manuscript "The Impact of Low-Holding-Voltage Issue in High-Voltage CMOS Technology and the Design of Latchup-Free Power-Rail ESD Clamp Circuit for LCD Driver ICs", presented an ESD protection design for the LCDs' drivers operated at Vdd=40V and fabricated in a 0.25μm technology. The authors shown an ESD protection design based on FOD devices which complied with an ESD protection level close to the equivalent given by 1.5A TLP. TLP and TLU tests accomplished on the stand-alone ESD protections showed that a FOD devices stack can provide ESD protection with no latchup problem at 40V operating voltage. Authors summarized the progress of the ESD protection design and a sequence of test results for assessing the affectivity of the ESD protection. The information provided in the manuscript is especially useful for design engineers dealing with ESD protection problems for LCD drivers fabricated in similar CMOS technologies.

Suggestions/Recommendations:

■Q1: Fig. 2a does not provide useful information.

Ans: Fig. 2a is revised by adding the picture of the driver ICs with tape carrier package (TCP). Please refer to the Fig. 2a in the revised manuscript.
Fig. 2 gives the readers the information of system-level EMC/ESD test on LCD panel by an ESD gun and the impact on the driver ICs in the LCD panel.

■Q2: Section II A second paragraph. Explanations given on the double-snapback behavior are very brief. Please elaborate.

Ans: Because the double-snapback characteristic in high-voltage nMOSFET is not the major topic in this manuscript, an extra reference to the explanations of the double-snapback behavior is added in section II in the revised manuscript.
Please refer to the reference [16] listed in the revised manuscript.

[16] M.-D. Ker and K.-H. Lin, "Double snapback characteristics in high-voltage nMOFETs and the impact to on-chip ESD protection design," *IEEE Electron Device Letters*, vol. 25, no. 9, pp. 640-642, 2004.

■Q3: Section II A, third paragraph, last sentence. The conjecture about the change in the trigger voltage by using the TLP should be carefully revised and discussed.

Ans: The discussion on the change in the trigger voltage by using the TLP is revised.

Please refer to the revised manuscript on section II A for detail.

"The difference on trigger voltages of the device measured by DC (HP4155) and TLP is caused by the transient-coupling effect (dV/dt transient) through the parasitic capacitance in the drain/bulk junction of the device. The TLP is designed with a rise time of 10ns to simulate the human-body-model (HBM) ESD event [17]. The dV/dt transient voltage at the zapping node can generate the displacement current to turn on the parasitic bipolar transistor of the device without involving the avalanche breakdown. Therefore, the trigger voltage of the device is lower by TLP measurement."

■Q4: Section III, last paragraph. The operating voltage is 40V and the TLP trigger/holding measured for the stack of two FOD devices showed in the manuscript that it may comply with this requirement. This is the case if the voltage overshoot does not damage the internal circuit's devices or if the core circuit load does not further delay the activation of the ESD protection (this can be properly verified once the ESD protection is integrated on the LCD circuit). What is the motivation of pushing the trigger down and show the FOD stack can be triggered and operated much below 40V? It may confuse the readers and does not provide additional information for the described ESD protection.

Ans: In this work, the stack of FOD devices is proposed to increase the total holding voltage to solve the latchup or latchup-like danger during normal circuit operating condition. But, during ESD stress condition, the stack FOD devices should turn on quickly to provide effective ESD protection to the internal circuits. The trigger voltage of stack FOD devices should be effectively reduced before the internal circuits are damaged by ESD energy. Therefore, the ESD detection circuit is designed to provide the trigger current to further decrease the trigger voltage of stack FOD devices during ESD stress condition. During normal circuit operating condition, the ESD detection circuit is inactive, and the common node of stack FOD devices is biased at VSS (0V).

Please refer to the revised manuscript on section III A for detail. The following sentence has been added in the revised manuscript.

"During ESD stress condition, the ESD clamp device should turn on quickly to bypass the ESD current, before the internal circuits are damaged by the ESD energy."

Please refer to the revised manuscript on section III C for detail. The section III C is revised in the revised manuscript.

".... With the total holding voltage of the stacked structure higher than the supply voltage,

the latchup or latchup-like issue will not occur even though the stacked structure is mis-triggered by the noise transient or glitch on the power lines during normal circuit operating condition. Therefore, the transient-induced latchup issue can be successfully overcome without modifying the high-voltage CMOS process. To provide effective ESD protection to the internal circuits during ESD stress, the substrate-triggered technique is achieved by the RC-based ESD detection circuit [18]. The RC-based ESD detection circuit can detect the ESD pulse to provide trigger current into the stacked structure, and then the stacked structure can turn on quickly to discharge the ESD current."

■Q5: Section III C. This section should be expanded to include the implementation of the ESD protection. What is the area required for the ESD protection, and what is the max ESD protection level?

Ans: The layout view of the stacked-field-oxide structure with two cascaded FOD devices is added in the revised manuscript. Please refer to the Fig. 11 in revised manuscript. The layout area of the stacked-field-oxide structure with a device width of 200μm for each FOD device is 150μm × 60μm. From the measured results, the It2 current of stacked-field-oxide structure is linearly increased while the device channel width increases. Therefore, the specified ESD level of driver ICs can be achieved by adjusting the device width of the stacked-field-oxide devices.

■Q6: Section III C. Fig 15 showed two protection clamps, one with two and the other with three FOD devices. Previous figures have showed the results of up to two FOD devices, and based on those results, the stack of two FOD devices seem to meet the ESD protection requirements. Is the scheme of three FOD necessary?

Ans: The latchup immunity of power clamp with two cascaded FOD devices to the noise transient on the power lines has been significantly improved. With three cascaded FOD devices, the total holding voltage of power clamp can be designed higher than the supply voltage to avoid the latchup or latchup-like issue. By adjusting different numbers or even different types of stacked ESD devices (NMOS, SCR, or FOD) in the power clamp, the total holding voltage of the stacked structure can be designed higher than the supply voltage.

Please refer to the revised manuscript on section III C for detail.

".... With two cascaded FOD devices in Fig. 17(a), the latchup immunity of power-rail ESD clamp circuit to the noise transient during normal circuit operating condition can be highly increased. With three cascaded FOD devices in Fig. 17(b), the total holding voltage of the stacked-field-oxide structure can be designed higher than the supply voltage. .... by

adjusting different numbers or even different types of stacked ESD devices (NMOS, SCR, or FOD) in the power-rail ESD clamp circuits, the total holding voltage of the stacked structure can be designed higher than the supply voltage. With the total holding voltage of the stacked structure higher than the supply voltage, the latchup or latchup-like issue will not occur even though the stacked structure is mis-triggered by the noise transient or glitch on the power lines during normal circuit operating condition. Therefore, the transient-induced latchup issue can be successfully overcome without modifying the high-voltage CMOS process....

■Q7: The detection circuit can be damaged by an ESD event. Authors should discuss why this circuit was not damaged during the ESD stress and show supporting evidence. In addition, gate oxides of MOS-based detection circuit can break down at the normal operating voltage of 40V. The authors need to address these issues carefully.

Ans: The RC-based ESD detection circuit shown in this manuscript has been widely used in the ESD protection design. It is useful to improve the turn-on efficiency of the ESD clamp. The ESD detection circuit can detect the ESD pulse to provide trigger current into the ESD clamp, and then ESD clamp can turn on quickly to discharge the ESD current. Because the ESD detection is not the ESD discharging path, it will not be damaged by the ESD pulse. For the detailed design and verification of ESD detection circuit, please refer the reference [18] listed in the revised manuscript.

[18] M.-D. Ker, "Area-efficient VDD-to-VSS ESD clamp circuit by using substrate-triggering field-oxide device (STFOD) for whole-chip ESD protection," in *Proc. of Int. Symp. on VLSI Technology, Systems, and Applications*, 1997, pp. 69-73.

In addition, the gate oxides of lateral diffused MOS (LDMOS) devices can sustain the normal operating voltage of 40V in this 40-V CMOS process. Therefore, the gate oxides of MOS-based detection circuit will not break down at the normal operating voltage of 40V.

Thank you very much for your valuable comments and suggestions to improve this manuscript.

Response to the Comments of Reviewer #2

Manuscript: JSSC #7753

Paper Title: The Impact of Low-Holding-Voltage Issue in High-Voltage CMOS Technology and the Design of Latchup-Free Power-Rail ESD Clamp Circuit for LCD Driver ICs

---

This paper includes some interesting results, which may be beneficial to designers and device engineers. I would recommend publishing this paper with some revisions. Some comments are given in the following for author's consideration.

■Q1: In order to avoid latch-up damage to power clamp in 40V power supply, authors used 2-stacked FODs to achieve a high holding voltage. It is a feasible approach to the high voltage (40V as in the paper) ESD protection without latch-up concern. But the 2-stacked FODs has a transient trigger voltage of only ~40.5V (see Fig. 13), which is very close to power supply of 40V. As a result, the device (2-stacked FODs) may be triggered on by the noise on power bus during normal operation, as authors stated in paragraph 3 on page 6. So, should the trigger voltage of 2-stacked FODs be increased by some volts (e.g. stacked 2 P+/Nwell diodes in series to the FODs) ? The increased voltage put some margin for 2-stacked FODs immune to Vdd bus noise, thus keep FOD-based power clamps away from mis-triggering by Vdd bus noise or glitch.

Ans: Thanks for your suggestion. The transient trigger voltage can be increased by the extra ESD protection device in series to the 2-stacked FODs. But, the power lines of driver ICs can be coupled with an overshooting/undershooting voltage up to several hundred volts during the system-level ESD stress, as mentioned in the introduction of this manuscript. Therefore, the power clamp could be triggered on by the transient pulse during the system-level ESD stress. In this work, we focused on increasing the total holding voltage of the power clamp by stacked structure to avoid the latchup or latchup-like issue, even though the power clamp could be mis-triggered by the noise transient or glitch on the power lines. With the extra ESD protection device in series to the 2-stacked FODs, the total holding voltage of the stacked structure can be designed higher than the supply voltage.

Please refer to the revised manuscript on section III C for detail. The section III C is revised in the revised manuscript.

".... With two cascaded FOD devices in Fig. 17(a), the latchup immunity of power-rail ESD clamp circuit to the noise transient during normal circuit operating condition can be highly increased. With three cascaded FOD devices in Fig. 17(b), the total holding voltage of the stacked-field-oxide structure can be designed higher than the supply voltage.... In addition, if the total holding voltage of the stacked structure can be designed higher than

the supply voltage, the FOD3 in Fig. 17(b) can be even replaced by other type of ESD device. So, by adjusting different numbers or even different types of stacked ESD devices (NMOS, SCR, or FOD) in the power-rail ESD clamp circuits, the total holding voltage of the stacked structure can be designed higher than the supply voltage. With the total holding voltage of the stacked structure higher than the supply voltage, the latchup or latchup-like issue will not occur even though the stacked structure is mis-triggered by the noise transient or glitch on the power lines during normal circuit operating condition. Therefore, the transient-induced latchup issue can be successfully overcome without modifying the high-voltage CMOS process....”

■Q2: ESD device performance (conduction uniformity, trigger voltage, It2, etc.) may vary with different layout architectures. The paper focuses on 200μm FOD and stacked FODs with collector-to-emitter of 6.0μm, but authors did not mention the device layout configuration (e.g. are the FODs multi-finger or multi-stripe?) It is more instructive to readers if authors could supplement following contents: (1) Configuration of tested samples, especially FOD (stacked FOD) which the paper focuses. (2) Have authors observed major difference in FOD ESD performance by changing N+-to-P+ (emitter-to-base, base-to-collector) spacing? (see in Fig. 5(a)); (3) How about the affect of process variation on FOD performance (e.g. trigger voltage, holding voltage)?

Ans: (1) The layout view of the stacked-field-oxide structure with two cascaded FOD devices is added in the revised manuscript. Please refer to the Fig. 11 in revised manuscript.

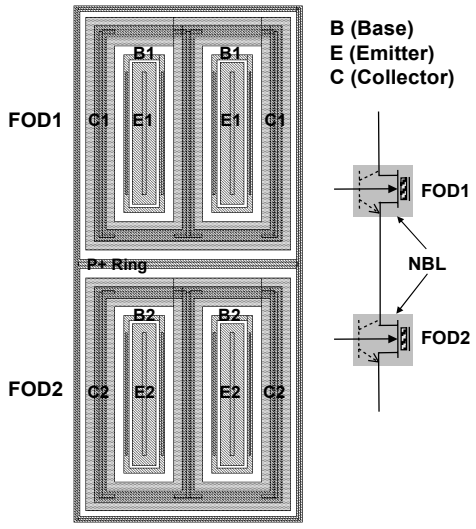


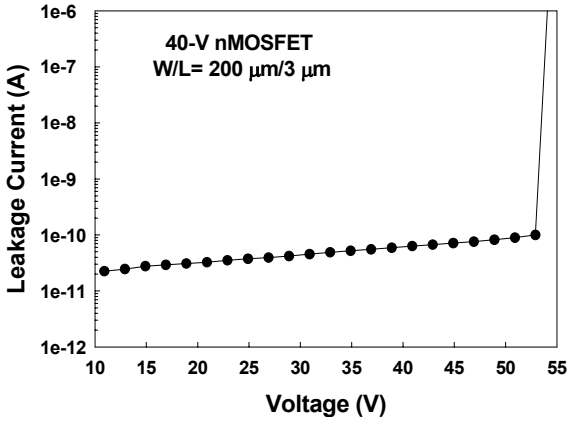
Fig. 11 The layout view and schematic diagram of the stacked-field-oxide structure with two cascaded FOD devices. Each FOD device in stacked-field-oxide structure is isolated by the n+ buried layer (NBL) from the common p-type substrate. The metal connections between FOD devices are not shown.

(2) In our testchips, the holding voltage of FOD device is not significantly increased as the spacing from collector diffusion to emitter diffusion increases (6μm -> 12μm). How to increase the holding voltage of high-voltage ESD protection device to avoid the latchup-like failure will be an important challenge to on-chip ESD protection design for high-voltage CMOS IC products. (3) As the experience of measurement, the process variation on FOD performance can be ignored.

■Q3: Fig. 3 provides cross-section of N-type LDMOS and its TLP response at Vgs=0V. The transient trigger voltage is only ~27.5V. Is it dangerous for the LDMOS to be used as output driver in 40V power supply (VDD_HV) as shown in Fig. 1 (the Mn)? When the pre-driver (Level-shifter circuits) outputs '0' state, Mp will be 'on', and Mn drain-to-source will see 40V drop (VDD_HV). In the status, any noise/glitch in VDD_HV or from substrate may trigger Mn into bipolar conduction. Have authors considered the possibility? Any related test data to clear the concern?

Ans: The DC characteristic of 40-V nMOSFET measured by HP4155 is shown in below. From the measured result, the breakdown voltage of 40-V nMOSFET is ~52 V. The difference on trigger voltage of the 40-V nMOSFET measured by DC (HP4155) and TLP is caused by transient-coupling effect. Please refer to the revised manuscript on section II A for detail.

"The difference on trigger voltages of the device measured by DC (HP4155) and TLP is caused by the transient-coupling effect (dV/dt transient) through the parasitic capacitance in the drain/bulk junction of the device. The TLP is designed with a rise time of 10ns to simulate the human-body-model (HBM) ESD event [17]. The dV/dt transient voltage at the zapping node can generate the displacement current to turn on the parasitic bipolar transistor of the device without involving the avalanche breakdown. Therefore, the trigger voltage of the device is lower by TLP measurement."



Thank you very much for your valuable comments and suggestions to improve this manuscript.

Response to the Comments of Reviewer #3

Manuscript: JSSC #7753

Paper Title: The Impact of Low-Holding-Voltage Issue in High-Voltage CMOS Technology and the Design of Latchup-Free Power-Rail ESD Clamp Circuit for LCD Driver ICs

---

■Q1: This paper outlines a way to design power rail ESD clamps for 40V circuits that may be useful, but it gives an incomplete view of the actual use conditions of these devices in a proposed application. For example, there is no indication of any temperature-dependent behavior of the stacked FOD structures. Is that all captured in a referenced publication? How do we know the burn-in and field use conditions for these devices? If these are to be latchup free as claimed, they must be subjected to a full complement of latchup tests, not just those favored by the authors.

Ans: Thanks for your suggestion. In this work, the stack of FOD devices is proposed to increase the total holding voltage to solve the latchup or latchup-like danger during normal circuit operating condition. With two cascaded FOD devices, the latchup immunity of power-rail ESD clamp circuit to the noise transient during normal circuit operating condition has been highly increased from the TLU test. Basically, the temperature of the system should not be too high for LCD panel applications. The temperature-dependent behavior of the stacked FOD structures is measured and discussed in the revised manuscript. Please refer to the revised manuscript on Fig. 14 and section III A for detail.

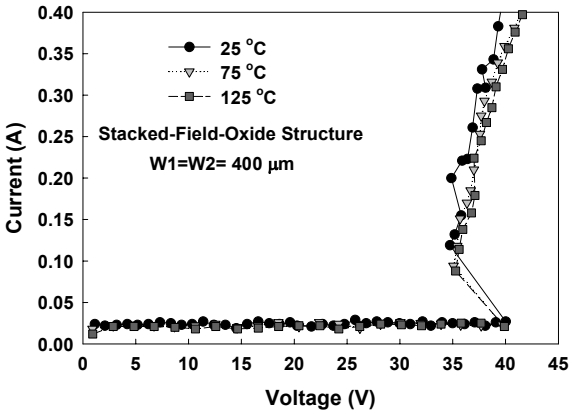


Fig. 14 The holding voltage of the stacked-field-oxide structure (two cascaded FOD devices) under different temperatures measured by TLP.

"To investigate the temperature-dependent behavior of the stacked-field-oxide structure, the TLP-measured I-V characteristics of stacked-field-oxide structure under different temperatures (25°C, 75°C, and 125°C) are compared in Fig. 14. The measured result shows no significant difference on the holding voltage of the stacked-field-oxide structure when the

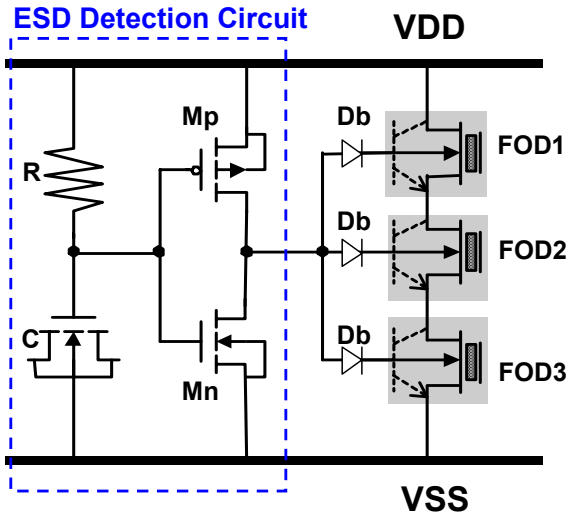
temperature increases. Therefore, the holding voltage of the stacked-field-oxide structure can be successfully controlled by the cascaded FOD devices even at high temperature."

■Q2: An even more obvious example of incomplete data is that the pulsed I-V curves in Fig. 11 are for grounded p-epi, and only Fig. 13 gives us a hint of how the proposed circuits in Fig. 15 would behave. Is Fig. 11 sufficient for the proposed application? If so, argue for that, but it looks like the holding voltage is too high. If not, wait until Fig. 15 devices are proven. Also, with the multiple common p-epi nodes as in Figs 13 and Fig 15, it's hard to know what single potential they are held at. It is quite possible that much current flows from FOD1 to FOD2 or FOD3 through the connection, bypassing FOD2 almost completely in the case of the 3-stack. Is this why no experimental 3-stack results appeared? Is the 3-stack known to behavior differently from the 2-stack when these common nodes are wired together? These things ought to be completed and discussed, not just "proposed", if a timed stacked device is the real solution. The strength of the inverter in Fig. 15 also interacts with the npn behavior of FOD1-3, and the reader wants to know more about that.

Ans: In this work, the stack of FOD devices is proposed to increase the total holding voltage to solve the latchup or latchup-like danger during normal circuit operating condition. From the measured results, the holding voltage of stacked-field-oxide structure with two cascaded FOD devices in snapback region is double of that of single FOD device. From the measured result of TLU test, the latchup immunity of power-rail ESD clamp circuit to the noise transient during normal circuit operating condition has been highly increased.

During ESD stress condition, the stack FOD devices should turn on quickly to provide effective ESD protection to the internal circuits. The RC-based ESD detection circuit shown in this manuscript has been widely used in the ESD protection design. It is useful to improve the turn-on efficiency of the ESD clamp. The ESD detection circuit can detect the ESD pulse to provide trigger current into the ESD clamp, and then ESD clamp can turn on quickly to discharge the ESD current.

Currently, we didn't have the testchip to verify the total holding voltage of the stacked structure with three cascaded FOD devices as shown in below. However, it's important to note that the each FOD device is isolated by the n+ buried layer (NBL) from the common p-type substrate. In addition, the blocking diodes Db are used to block the current flowing through the metals connected among the trigger nodes (base nodes) of the stacked FOD devices (Please refer to reference [22] added in the revised manuscript). Therefore, the unexpected current path can be avoided and the accumulation property in holding voltage for the three cascaded FOD devices can be achieved.



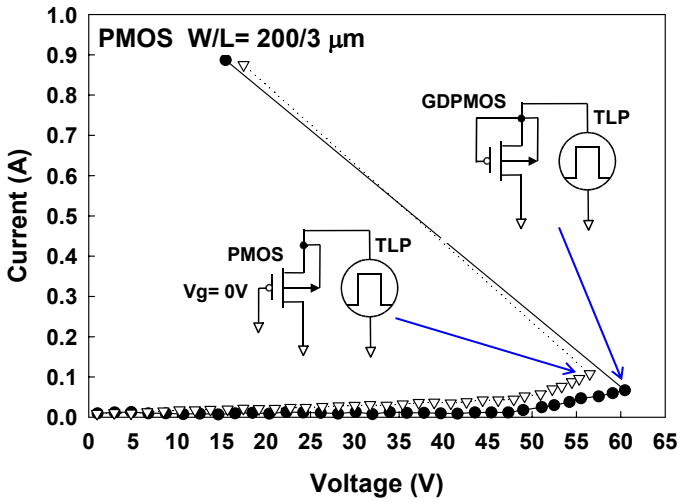
Please refer to the revised manuscript on section III C for detail. The section III C is revised in the revised manuscript.

"The proposed power-rail ESD clamp circuits with two cascaded FOD devices and three cascaded FOD devices in high-voltage CMOS ICs are shown in Figs. 17(a) and (b), respectively. Each FOD device in stacked-field-oxide structure is isolated by the n+ buried layer (NBL) from the common p-type substrate. With two cascaded FOD devices in Fig. 17(a), the latchup immunity of power-rail ESD clamp circuit to the noise transient during normal circuit operating condition can be highly increased. With three cascaded FOD devices in Fig. 17(b), the total holding voltage of the stacked-field-oxide structure can be designed higher than the supply voltage. The blocking diodes Db are used to block the current flowing through the metals connected among the trigger nodes (base nodes) of the stacked FOD devices [22]. Therefore, the unexpected current path can be avoided and the accumulation property in holding voltage for the three cascaded FOD devices can be achieved. In addition, if the total holding voltage of the stacked structure can be designed higher than the supply voltage, the FOD3 in Fig. 17(b) can be even replaced by other type of ESD device. So, by adjusting different numbers or even different types of stacked ESD devices (NMOS, SCR, or FOD) in the power-rail ESD clamp circuits, the total holding voltage of the stacked structure can be designed higher than the supply voltage. With the total holding voltage of the stacked structure higher than the supply voltage, the latchup or latchup-like issue will not occur even though the stacked structure is mis-triggered by the noise transient or glitch on the power lines during normal circuit operating condition. Therefore, the transient-induced latchup issue can be successfully overcome without modifying the high-voltage CMOS process. To provide effective ESD protection to the internal circuits during ESD stress, the substrate-triggered technique is achieved by the

RC-based ESD detection circuit [18]. The RC-based ESD detection circuit can detect the ESD pulse to provide trigger current into the stacked structure, and then the stacked structure can turn on quickly to discharge the ESD current."

■Q3: Also the argument surrounding Fig. 6 that dismisses the GDPMOS device is unconvincing as stated, because the authors missed their opportunity to try it with a timed circuit as in Fig. 15, only complementary to it, temporarily grounding the n-well. Fig. 6 shows that a single GDPMOS device stands of the 40V quite well, but the TLP experiment expected self-triggering of the pnp. What if it were given as much help with a triggering circuit as the stacked FOD in Fig. 15? As there is no evident need to stack the GDPMOS, this avoids all the stacking issues as mentioned above.

Ans: Thanks for your suggestion. The TLP-measured I-V curve of 40-V PMOS device with its gate connected to the ground is shown in below. With the gate connected to the ground, the parasitic pnp BJT of PMOS device can be triggered on without involving the avalanche breakdown during ESD stress. From the measured result, the It2 of PMOS device with the gate connected to the ground can be only slightly improved as compared to that with the gate connected to the VDD (GDPMOS). Without snapback characteristic, the non-uniform turn-on issue of multiple fingers in PMOS device is not obvious, therefore the ESD level of PMOS device can't be efficiently improved even with a trigger circuit (timed circuit) to control the gate or n-well of PMOS device.



Thank you very much for your valuable comments and suggestions to improve this manuscript.