## Nanoelectronics and Gigascale Systems Laboratory Institute of Electronics, National Chiao-Tung University

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Mar. 7, 2005

To

Dr. Ali Niknejad Associate Editor, JSSC

Email: niknejad@eecs.berkeley.edu

Paper Title: The Impact of Low-Holding-Voltage Issue in High-Voltage CMOS Technology and the Design of Latchup-Free Power-Rail ESD Clamp Circuit for LCD Driver ICs (M 7753)

Author(s): Ming-Dou Ker and Kun-Hsien Lin

Dear Prof. Niknejad:

Enclosed please find my revised manuscript entitled as "The Impact of Low-Holding-Voltage Issue in High-Voltage CMOS Technology and the Design of Latchup-Free Power-Rail ESD Clamp Circuit for LCD Driver ICs," which is returned to you for possible publication in *Journal of Solid-State Circuits*. The revision in the revised manuscript has been shown with blue-color words to indicate the changes in this paper. The response to all reviewers' comments is also attached. Please feel free to contact me, if there is any correspondence on this revision.

Thank you very much.

Ming-Don Ker

Sincerely,

Ming-Dou Ker

Professor, National Chiao-Tung University