Modeling the Positive-Feedback Regenerative Process of CMOS Latchup by a Positive Transient Pole Method—Part I: Theoretical Derivation

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***Abstract*— A novel method to characterize the mechanism of positive-feedback regeneration in a p-n-p-n structure during CMOS latchup transition is developed. It is based on the derived time-varying transient poles in large-signal base-emitter voltages of the lumped equivalent circuit of a p-n-p-n structure. Through calculating the time-varying transient poles during CMOS latchup transition, it is found that there exists a transient pole to change from negative to positive and then this pole changes to negative again. A p-n-p-n structure, which has a stronger positive-feedback regeneration during turn-on transition, will lead to a larger positive transient pole. The time when the positive transient pole occurs during CMOS latchup transition is the time when the positive-feedback regeneration starts. By this positive transient pole, the positive-feedback regenerative process of CMOS latchup can be quantitatively characterized.**

NOMENCLATURE

$Q_1(Q_2)$	Parasitic lateral (vertical) p-n-p (n-p-n) BJT in a p-n-p-n structure of CMOS latchup.
$Rs(Rw)$	Equivalent substrate (well) resistances in CMOS IC's.
$C_{jbe1}(C_{jbe2})$	Base-emitter junction depletion capacitance of BJT $Q_1(Q_2)$.
$C_{jbc1}(C_{jbc2})$	Base-collector junction depletion capacitance of BJT $Q_1(Q_2)$.
$C_{\tau be1}(C_{\tau be2})$	Base-emitter junction diffusion capacitance of BJT $Q_1(Q_2)$.
$C_{\tau bc1}(C_{\tau bc2})$	Base-collector junction diffusion capacitance of BJT $Q_1(Q_2)$.
$C_{e1}(C_{e2})$	Base-emitter junction capacitance of BJT $Q_1(Q_2)$ including depletion and diffusion capacitances as defined in (8) or (10).
$C_{c1}(C_{c2})$	Base-collector junction capacitance of BJT $Q_1(Q_2)$ including depletion and diffusion capacitances as defined in (9) or (11).
$I_1(I_2)$	Transient-induced trigger current generated in substrate (well) to cause CMOS latchup.
$I_{B1}(I_{B2})$	Voltage-dependent intrinsic base current of BJT $Q_1(Q_2)$ without the displacement current of capacitances.
$I_{C1}(I_{C2})$	Voltage-dependent intrinsic collector current of BJT $Q_1(Q_2)$ without the displacement current of capacitances.
$i_{B1}(i_{B2})$	Large-signal base current of BJT $Q_1(Q_2)$ including the displacement current of capacitances as defined in (4) or (6).
$i_{C1}(i_{C2})$	Large-signal collector current of BJT $Q_1(Q_2)$ including the displacement current of capacitances as defined in (5) or (7).
$v_{EB1}(v_{BE2})$	Large-signal base-emitter voltage of BJT $Q_1(Q_2)$.
$v_{CB1}(v_{BC2})$	Large-signal base-collector voltage of BJT $Q_1(Q_2)$.
V_{DD}	Power supply of CMOS IC's.
$g_{B1}(g_{B2})$	Piecewise-linearized large-signal transconductance of base current with respect to its base-emitter voltage of BJT $Q_1(Q_2)$.
$g_{C1}(g_{C2})$	Piecewise-linearized large-signal transconductance of collector current with respect to its base-emitter voltage of BJT $Q_1(Q_2)$.
τ_k	A certain time interval during CMOS latchup transition.
p_1, p_2	Poles of the solved time-dependent $v_{EB1}(t)$ and $v_{BE2}(t)$ as defined in (21) and (22).
$p_{1(\max)}$	Maximum peak value of the positive p_1 pole during latchup transition.
t_r	The time required for p_1 pole to become positive after trigger currents are applied.

I. INTRODUCTION

As CMOS technology is scaled down to submicron regime to achieve higher integration density and faster operation speed in VLSI/ULSI applications, the reduced spacings of the inherently embedded parasitic p-n-p-n structure further increase the latchup susceptibility of CMOS IC's. Latchup, which creates a low impedance path from the power supply V_{DD} to ground, is one of major failure mechanisms in the reliability of bulk CMOS IC's. The dc switching voltage of a parasitic p-n-p-n structure designed according to the design rules and fabricated by the submicron bulk CMOS technology is as high as 30–50 V, which is much greater than 5 volt of V_{DD} power supply in CMOS IC's. Thus, latchup in CMOS IC's is initially triggered by sharp voltage/current transitions

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or by voltage/current overshooting and undershooting at the power supplies or at the output nodes, rather than by direct overstress of dc voltage. This transient-induced latchup is especially acute in CMOS IC's because short-circuit currents only during logic switching transitions, which usually cause voltage overshooting or undershooting at the clock transition edges.

Due to the complex phenomena of nonlinear cross-coupled regenerative I-V characteristics in a p-n-p-n structure, it is more difficult to model latchup in the transient case with the additional variable of time than in the dc case. Latchup firing is in itself a transient phenomenon, so it has to be discussed in time domain. The latchup transition and its mechanisms have attracted much attention, and some efforts have been contributed to characterize it [1]–[19]. In the early past, the transient behaviors of turn-on process in the thyristor or the semiconductor-controlled-rectifier (SCR) had also been characterized [20]–[30].

In the previous works, there are two main approaches to model latchup behavior in a p-n-p-n structure. One is the development of analytical models based on the lumped equivalent circuits [1]–[13], [20]–[23], [31]–[38]. The other is the application of numerical simulation based on the solutions of a full set of semiconductor device equations with process parameters [14]–[19], [26]–[30], [39]–[41]. The lumped equivalent model is often used to study the switching behaviors of latchup transition. Some criteria had been developed to judge the occurrence of latchup in a p-n-p-n structure [9]–[13], [20], [21], [31]–[37]. Numerical simulation approach may offer more accurate representation of 2-D or 3-D p-n-p-n structure and the detailed dynamics of charge distribution during latchup transition. But, numerical simulation demands much computing resource and often offers little analytical understanding on latchup transition. The restriction to finite representation of a p-n-p-n structure and the lack of general latchup criterion also make the numerical simulation approach somewhat inefficient. Analytical model with a general latchup criterion is still quite helpful in understanding and controlling latchup for practical and efficient applications. It can provide us with good design guidelines and quick initial characterization. Then numerical simulation can be used as a refining treatment.

In the literatures describing latchup transition, the switching mechanism of a p-n-p-n structure from the OFF (high-impedance) state to its ON (low-impedance) state are all described qualitatively. No any method is developed to quantitatively investigate the mechanism of turn-on process in a p-n-p-n structure and used to characterize the positive-feedback regeneration of latchup transition in terms of device parameters.

In this paper, a time-varying positive transient pole is derived from the large-signal behaviors of a p-n-p-n structure and used to analyze the positive-feedback regenerative process of CMOS latchup transition. By using this time-varying positive transient pole, the switching mechanism of a p-n-p-n structure can be well explained and fully characterized. Especially, the influences of device parameters on the positive-feedback regeneration of CMOS latchup transition can be quantitatively investigated. Therefore some guidelines can be obtained to improve the immunity against transient-induced latchup in CMOS IC's.

II. Dynamic Behaviors of CMOS Latchup Transition

The classical two-transistor model of a p-n-p-n structure with device parameters extracted from the fabricated p-n-p-n structure in CMOS IC's is adopted to analyze the dynamic behaviors of CMOS latchup transition. With extracted device parameters including current-dependent beta gain, voltage-dependent junction capacitance, and transit time, it can offer a reasonable accuracy in modeling the turn-on process of a p-n-p-n structure.

Fig. 1(a) shows the schematic cross-sectional view of a CMOS inverter and the parasitic p-n-p-n latching path in the p-well n-substrate bulk CMOS technology. The corresponding lumped equivalent circuit of the p-n-p-n structure is shown in Fig. 1(b), where $Q_1(Q_2)$ is the parasitic lateral (vertical) p-n-p (n-p-n) bipolar junction transistor (BJT). Q_1 transistor is composed of p+ diffusion as emitter, n-substrate as base, and p-well as its collector. Q_2 transistor is composed of n-substrate as collector, p-well as base, and n+ diffusion in p-well as its emitter. Resistor $Rs(Rw)$ is the equivalent substrate (well) resistance. The voltage-dependent base-emitter and base-collector junction capacitances (C_{e1}, C_{e2}, C_{c1}, and C_{c2}) are also shown in Fig. 1(a) and (b). The transient-induced trigger currents generated in n-substrate and p-well by internal voltage/current transitions due to circuit operations or by external voltage/current transitions due to unexpected events to cause CMOS latchup are marked as the I_1 and I_2 currents, respectively.

Through the circuit connection in Fig. 1(b), the relations among the large-signal branch currents and node voltages are

$$i_{C2}(t) + I_1(t) - i_{B1}(t) - \frac{v_{EB1}(t)}{Rs} = 0 \tag{1}$$

$$i_{C1}(t) + I_2(t) - i_{B2}(t) - \frac{v_{BE2}(t)}{Rw} = 0 \tag{2}$$

$$v_{CB1}(t) = v_{BC2}(t) = -[V_{DD} - v_{EB1}(t) - v_{BE2}(t)]. \tag{3}$$

Taking the effects of junction depletion and diffusion capacitances into considerations and using the modified Gummel-Poon model of BJT [42]–[44], the large-signal base and collector currents of BJT's Q_1 and Q_2 in Fig. 1(b) can be written as

$$i_{B1}(t) = I_{B1}(t) + \frac{\partial(C_{e1}\cdot v_{EB1})}{\partial t} + \frac{\partial(C_{c1}\cdot v_{CB1})}{\partial t} \tag{4}$$

$$i_{C1}(t) = I_{C1}(t) - \frac{\partial(C_{c1}\cdot v_{CB1})}{\partial t} \tag{5}$$

$$i_{B2}(t) = I_{B2}(t) + \frac{\partial(C_{e2}\cdot v_{BE2})}{\partial t} + \frac{\partial(C_{c2}\cdot v_{BC2})}{\partial t} \tag{6}$$

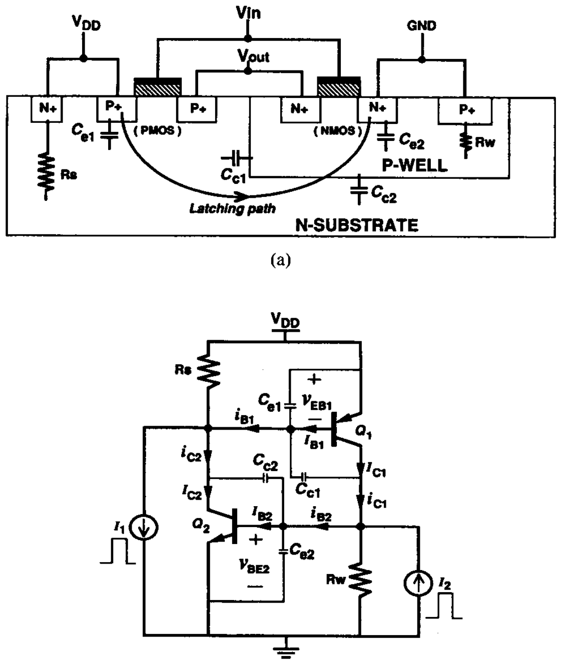
$$i_{C2}(t) = I_{C2}(t) - \frac{\partial(C_{c2}\cdot v_{BC2})}{\partial t} \tag{7}$$

where

$$C_{e1} = C_{jbe1} + C_{\tau be1} \tag{8}$$

$$C_{c1} = C_{jbc1} + C_{\tau bc1} \tag{9}$$

$$C_{e2} = C_{jbe2} + C_{\tau be2} \tag{10}$$



(a)

(b)

Fig. 1. (a) A schematic cross-sectional view of a CMOS inverter and the parasitic resistances and capacitances in a p-n-p-n structure; (b) The lumped equivalent circuit of the p-n-p-n structure in (a).

$$C_{c2} = C_{jbc2} + C_{\tau bc2}. \tag{11}$$

From the above equations, it is obviously indicated that the turn-on mechanisms of a p-n-p-n structure are heavily dependent on its junction capacitances.

The intrinsic base and collector currents of BJT's are exponential functions of their base-emitter and base-collector voltages. The junction capacitances are also related to their base-emitter and base-collector voltages [42]–[44]. In (3), the base-collector voltages of BJT's Q_1 and Q_2 in the lumped equivalent circuit of Fig. 1(b) can be expressed in terms of their base-emitter voltages. Thus, the time-varying large-signal base-emitter voltages, $v_{EB1}(t)$ and $v_{BE2}(t)$, are the most fundamental factors in the lumped equivalent circuit of a p-n-p-n structure during its turn-on transition. If these $v_{EB1}(t)$ and $v_{BE2}(t)$ are solved, all branch currents and node voltages of the lumped equivalent circuit in Fig. 1(b) can be found out from them.

In order to observe the time dependence of latchup transition, the popular circuit simulator *HSPICE* [44] is adopted to accurately solve these $v_{EB1}(t)$ and $v_{BE2}(t)$. With extracted device parameters of parasitic lateral and vertical BJT's in a p-n-p-n structure as listed in Table I, $v_{EB1}(t)$ and $v_{BE2}(t)$ in both latchup and nonlatchup cases triggered by a pulse-type 5-mA substrate current I_1 with two different pulse widths of 10 nS and 3.5 nS are simulated by *HSPICE* and the results are drawn in Fig. 2. The equivalent substrate and well resistances (Rs and Rw) used in the simulation are 800 Ω and 5.6 KΩ, respectively. The 5-mA I_1 pulse is applied at the time interval of $t = 0$. Before $t = 0$, $v_{EB1}(t)$ and $v_{BE2}(t)$ are set to zero because the p-n-p-n structure is initially *off*. As the 5-mA I_1 is applied with 10-nS pulse width, $v_{EB1}(t)$ raises up quickly in several nanosecond (nS) and then holds on a stable value about 0.827 V, while $v_{BE2}(t)$ first drops to −0.345 V and then raises up and holds on about 0.897 V. After I_1 trigger current changes from 5 mA to 0 mA at the time interval of 10 nS, $v_{EB1}(t)$ and $v_{BE2}(t)$ still remain in their stable values, and this condition is the latchup case. On the contrary, if the 5-mA I_1 trigger current only with 3.5-nS pulse width, $v_{EB1}(t)$ and $v_{BE2}(t)$ are first raising as those in the latchup case but then they drop to zero volt after I_1 triggering. Since $v_{EB1}(t)$ and $v_{BE2}(t)$ cannot hold on their stable turn-on voltages after triggering, this is a nonlatchup case. If the pulse width of the 5-mA I_1 trigger current is reduced from 10 nS to 3.5 nS, it can be found that there is a minimum value of pulse width to sustain the occurrence of latchup. Similarly, variations of $v_{EB1}(t)$ and $v_{BE2}(t)$ due to well current I_2 triggering can be also observed by this method. Generally, a trigger current with higher pulse amplitude requires a shorter minimum pulse width to initiate the occurrence of CMOS latchup [13].

Through observation on $v_{EB1}(t)$ and $v_{BE2}(t)$, the dynamic behaviors of CMOS latchup transition due to transient-induced substrate or well currents triggering can be clearly understood.

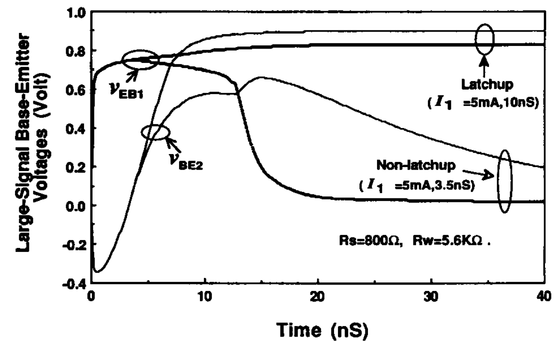


Fig. 2. The typical *HSPICE* simulated $v_{EB1}(t)$ and $v_{BE2}(t)$ waveforms of a p-n-p-n structure with $Rs = 800\Omega$ and $Rw = 5.6\,\mathrm{K}\Omega$ in both latchup and nonlatchup cases.

TABLE I
THE EXTRACTED DEVICE PARAMETERS OF THE PARASITIC LATERAL AND VERTICAL BJT'S IN A p-n-p-n STRUCTURE OF CMOS IC'S

parameter	Q_1(p-n-p) (lateral)	Q_2(n-p-n) (vertical)
β_F	1.104	277.2
β_R	0.2	2.0
I_S(A)	2.833E–16	8.112E–16
I_{KF}(A)	6.909E–5	4.867E–4
I_{SE}(A)	4.250E–14	1.217E–13
τ_F(nS)	20	0.25
τ_R(nS)	10	2.0
C_{jc0}(pF)	2.0	0.6
C_{je0}(pF)	0.6	1.3
MJE	0.5	0.5
MJC	0.33	0.33

In this work, the efforts are emphasized to quantitatively model the positive-feedback regenerative process of CMOS latchup and to investigate the influence of device parameters on this positive-feedback regeneration in a p-n-p-n structure.

III. The Time-Varying Positive Transient Pole and Its Effect on CMOS Latchup Transition

Traditionally, the positive-feedback regenerative process during latchup transition in a p-n-p-n structure is qualitatively explained as the regeneration in cross-coupled base and collector currents of BJT's Q_1 and Q_2 with the sum of their alpha gains or the product of their beta gains greater than unity [45], [46]. In Section II, $v_{EB1}(t)$ and $v_{BE2}(t)$ have been explored as the most fundamental factors in a p-n-p-n structure during the turn-on transition. Thus, the positive-feedback regenerative process can be more physically understood through detailed insight in the voltage waveforms of $v_{EB1}(t)$ and $v_{BE2}(t)$.

A. The Time-Varying Large-Signal Base-Emitter Voltages

If junction capacitances are piecewisely estimated as their averaged values between two adjacent time intervals, the $\partial(C_j \cdot v_j)/\partial t$ terms in (4)–(7) can be approximated as $C_j \cdot (\partial v_j/\partial t)$ in each time interval, where the C_j and v_j represent the junction capacitance and its voltage bias, respectively, in each junction of the p-n-p-n structure. The detailed derivation of piecewise-averaged approximation on the base-emitter and base-collector junction capacitances is given in Appendix A. With averaged approximation on junction capacitances in each time interval, $v_{EB1}(t)$ and $v_{BE2}(t)$ through (1)–(7) can be rearranged and further expressed as

$$\frac{\partial v_{EB1}(t)}{\partial t} = \frac{I_{F1}(t) \cdot (C_{c1} + C_{c2} + C_{e2}) - I_{F2}(t) \cdot (C_{c1} + C_{c2})}{\Delta_C} \quad (12)$$

$$\frac{\partial v_{BE2}(t)}{\partial t} = \frac{I_{F2}(t) \cdot (C_{c1} + C_{c2} + C_{e1}) - I_{F1}(t) \cdot (C_{c1} + C_{c2})}{\Delta_C} \quad (13)$$

where

$$I_{F1}(t) \equiv I_{C2}(t) - I_{B1}(t) - \frac{v_{EB1}(t)}{Rs} + I_1(t) \quad (14)$$

$$I_{F2}(t) \equiv I_{C1}(t) - I_{B2}(t) - \frac{v_{BE2}(t)}{Rw} + I_2(t) \quad (15)$$

$$\Delta_C \equiv (C_{c1} + C_{c2}) \cdot (C_{e1} + C_{e2}) + C_{e1} \cdot C_{e2}. \quad (16)$$

These equations still can not be directly solved by hand derivation because $I_{B1}(t), I_{B2}(t), I_{C1}(t)$, and $I_{C2}(t)$ are exponential functions of $v_{EB1}(t)$ and $v_{BE2}(t)$. If these intrinsic base and collector currents are further approximated as linear functions of their base-emitter voltages in each time interval, the apparent solutions of $v_{EB1}(t)$ and $v_{BE2}(t)$ in (12)–(15) can be directly found out.

Even due to pulse-type substrate or well currents triggering, $v_{EB1}(t)$ and $v_{BE2}(t)$ do not abruptly change in time domain because of *RC* charging or discharging delay in device junction capacitances and parasitic substrate or well resistances. With $v_{EB1}(t)$ and $v_{BE2}(t)$ gradually changing, the intrinsic base and collector currents can be further piecewisely linearized from their exponential relations to become as the first-order approximated linear relations in each time interval. The first-order piecewise-linearized base and collector current equations in each time interval are derived in Appendix B.

Using reasonably linearized approximation in the intrinsic base and collector currents as well as averaged estimation in each junction capacitance of a p-n-p-n structure in each time interval during latchup transition, $v_{EB1}(t)$ and $v_{BE2}(t)$ can be directly solved and expressed as functions of time, trigger signals, and device parameters. At a time interval τ_k, the Laplace-form solutions of $v_{EB1}(t)$ and $v_{BE2}(t)$ can be obtained from (12)–(16), (A.1)–(A.6), and (B.1)–(B.8) as (17) and (18) shown at the bottom of the page. The corresponding time-domain solutions around the time interval τ_k are two-pole functions of time t. They are

$$v_{EB1}(t)|_{\tau_k+t} = A_0 + A_1 \cdot e^{(p_1 \cdot t)} + A_2 \cdot e^{(p_2 \cdot t)} \quad (19)$$

$$v_{BE2}(t)|_{\tau_k+t} = B_0 + B_1 \cdot e^{(p_1 \cdot t)} + B_2 \cdot e^{(p_2 \cdot t)} \quad (20)$$

where the poles p_1 and p_2 at the time interval τ_k are derived as

$$p_1 = \frac{-(a_1 + b_1) + \sqrt{(a_1 + b_1)^2 - 4 \cdot (a_1 \cdot b_1 - a_2 \cdot b_2)}}{2} \quad (21)$$

$$p_2 = \frac{-(a_1 + b_1) - \sqrt{(a_1 + b_1)^2 - 4 \cdot (a_1 \cdot b_1 - a_2 \cdot b_2)}}{2} \quad (22)$$

The a_j, b_j, A_j, and B_j ($j = 0, 1, 2$) coefficients in (17)–(22) are functions of device parameters and trigger currents at the time interval τ_k, and they are summarized in Table II. The time interval τ_k is the kth time interval in *HSPICE* simulation of transient analysis with a given time step. The large-signal base-emitter voltage waveforms in Fig. 2 due to a 5-mA I_1 triggering with pulse widths of 10 nS or 3.5 nS are simulated with a time step of 0.01 nS. Thus, the time period from $t = 0$ to time interval τ_k is $0.01 \times k$ nS. If a shorter time step is used in *HSPICE* simulation, a better accuracy on the transient-analysis simulated results can be obtained but it consumes more CPU time.

$$V_{EB1}(S) = \frac{S^2 \cdot v_{EB1}(\tau_k) + S \cdot [b_1 \cdot v_{EB1}(\tau_k) + a_2 \cdot v_{BE2}(\tau_k) + a_0] + (a_0 \cdot b_1 + a_2 \cdot b_0)}{S \cdot [S^2 + S \cdot (a_1 + b_1) + (a_1 \cdot b_1 - a_2 \cdot b_2)]} \quad (17)$$

$$V_{BE2}(S) = \frac{S^2 \cdot v_{BE2}(\tau_k) + S \cdot [a_1 \cdot v_{BE2}(\tau_k) + b_2 \cdot v_{EB1}(\tau_k) + b_0] + (b_0 \cdot a_1 + b_2 \cdot a_0)}{S \cdot [S^2 + S \cdot (a_1 + b_1) + (a_1 \cdot b_1 - a_2 \cdot b_2)]} \quad (18)$$

TABLE II
THE COEFFICIENTS IN THE EQUATIONS OF (17)–(22)

$$A_0 = \frac{a_0 \cdot b_1 + b_0 \cdot a_2}{a_1 \cdot b_1 - a_2 \cdot b_2}$$

$$A_1 = \frac{1}{p_1 \cdot (p_1 - p_2)} \cdot \Big\{ (p_1)^2 \cdot v_{EB1}(\tau_k) + p_1 \cdot [b_1 \cdot v_{EB1}(\tau_k) + a_2 \cdot v_{BE2}(\tau_k) + a_0] + (a_0 \cdot b_1 + b_0 \cdot a_2) \Big\}$$

$$A_2 = \frac{1}{p_2 \cdot (p_2 - p_1)} \cdot \Big\{ (p_2)^2 \cdot v_{EB1}(\tau_k) + p_2 \cdot [b_1 \cdot v_{EB1}(\tau_k) + a_2 \cdot v_{BE2}(\tau_k) + a_0] + (a_0 \cdot b_1 + b_0 \cdot a_2) \Big\}$$

$$B_0 = \frac{b_0 \cdot a_1 + a_0 \cdot b_2}{a_1 \cdot b_1 - a_2 \cdot b_2}$$

$$B_1 = \frac{1}{p_1 \cdot (p_1 - p_2)} \cdot \Big\{ (p_1)^2 \cdot v_{BE2}(\tau_k) + p_1 \cdot [a_1 \cdot v_{BE2}(\tau_k) + b_2 \cdot v_{EB1}(\tau_k) + b_0] + (b_0 \cdot a_1 + a_0 \cdot b_2) \Big\}$$

$$B_2 = \frac{1}{p_2 \cdot (p_2 - p_1)} \cdot \Big\{ (p_2)^2 \cdot v_{BE2}(\tau_k) + p_2 \cdot [a_1 \cdot v_{BE2}(\tau_k) + b_2 \cdot v_{EB1}(\tau_k) + b_0] + (b_0 \cdot a_1 + a_0 \cdot b_2) \Big\}$$

where

$$a_2 = \frac{1}{\Delta_C} \cdot [(C_{c1} + C_{c2} + C_{e2}) \cdot g_{C2} + (C_{c1} + C_{c2}) \cdot (g_{B2} + 1/R_w)]$$

$$a_1 = \frac{1}{\Delta_C} \cdot [(C_{c1} + C_{c2} + C_{e2}) \cdot (g_{B1} + 1/R_s) + (C_{c1} + C_{c2}) \cdot g_{C1}]$$

$$a_0 = \frac{1}{\Delta_C} \cdot [(C_{c1} + C_{c2} + C_{e2}) \cdot (I_1 + I_{C20} - I_{B10}) - (C_{c1} + C_{c2}) \cdot (I_2 + I_{C10} - I_{B20})]$$

$$b_2 = \frac{1}{\Delta_C} \cdot [(C_{c1} + C_{c2} + C_{e1}) \cdot g_{C1} + (C_{c1} + C_{c2}) \cdot (g_{B1} + 1/R_s)]$$

$$b_1 = \frac{1}{\Delta_C} \cdot [(C_{c1} + C_{c2} + C_{e1}) \cdot (g_{B2} + 1/R_w) + (C_{c1} + C_{c2}) \cdot g_{C2}]$$

$$b_0 = \frac{1}{\Delta_C} \cdot [(C_{c1} + C_{c2} + C_{e1}) \cdot (I_2 + I_{C10} - I_{B20}) - (C_{c1} + C_{c2}) \cdot (I_1 + I_{C20} - I_{B10})]$$

B. The Positive Transient Pole and Its Effects on the Positive-Feedback Regenerative Process

Taking a deeper insight into the derived pole equations, these two time-varying transient poles are heavily dependent on junction capacitances of a p-n-p-n structure. The p_2 pole is always negative as expressed in (22), but p_1 pole is dependent on the term of $(a_1 \cdot b_1 - a_2 \cdot b_2)$ in the numerator of (21). This term can be further derived with the coefficients in Table II as

$$a_1 \cdot b_1 - a_2 \cdot b_2 = \frac{1}{\Delta_C} \cdot \left[\left(g_{B1} + \frac{1}{Rs} \right) \cdot \left(g_{B2} + \frac{1}{Rw} \right) - g_{C1} \cdot g_{C2} \right] \quad (23)$$

where Δ_C is only a function of junction capacitances in (16), and the value of Δ_C is always positive. The another term in the right-hand side of (23) is "$\{[g_{B1} + (1/Rs)] \cdot [g_{B2} + (1/Rw)] - g_{C1} \cdot g_{C2}\}$." If this term is greater than zero, p_1 pole is negative. But, p_1 pole becomes positive if this term is less than zero. During latchup transition, this term varies from positive to negative and then becomes positive again. Thus p_1 pole varies from negative to positive and then becomes negative again. The variation of p_1 pole and the corresponding positive-feedback regenerative process during latchup transition can be clearly explained as following:

1) First, the p-n-p-n structure is initially off as the transient-induced substrate or well currents just start to trigger, while $g_{B1(2)}$ and $g_{C1(2)}$ are nearly zero. The term in (23) is positive due to the presence of substrate and well resistances Rs and Rw, and thus p_1 pole is initially negative.
2) As time increases and trigger currents are applied, the base and collector currents in the parasitic BJT's Q_1 and Q_2 increase and lead to the increase of $g_{B1(2)}$ and $g_{C1(2)}$. But, the term in (23) is still positive and p_1 pole is negative.
3) With continuous supporting from trigger currents, $g_{B1(2)}$ and $g_{C1(2)}$ apparently grow up. Especially, g_{C2} increases much faster than g_{B2} because the maximum beta gain of vertical BJT Q_2 is much greater than unity. At one critical time, the term in (23) will change from positive to negative due to the continuous increase of g_{C1} and g_{C2}. This leads p_1 pole to become positive. As listed in Table II, the A_1 and B_1 coefficients in (19) and (20) are positive if the p_1 pole is positive. These positive A_1, B_1, and p_1 cause $v_{EB1}(t)$ and $v_{BE2}(t)$ to raise up fast with an exponential increasing rate. Moreover, the base and collector currents of BJT's Q_1 and Q_2 are basically exponential functions of $v_{EB1}(t)$ and $v_{BE2}(t)$, respectively. So the base and collector currents change quite quickly in a double exponential functions of time. These quickly increasing base and collector currents in turns lead to sharp increase of g_{C1} and g_{C2}. Thus the positive-feedback regeneration occurs with a double exponential increasing rate to push the p-n-p-n structure into its latching state. The p_1 pole becomes more and more positive.
4) As latchup is under exponential regeneration, the faster increasing collector currents of Q_1 and Q_2 will cause the high-level injection effect modeled by the I_{KF} parameter in *HSPICE* [44]. The high-level injection effect induces the degradation in current gain of BJT device [42]–[44], [47]. The I_{KF} parameter of parasitic vertical BJT Q_2 in CMOS technology is only about 0.4867 mA which is much smaller than that of a normal BJT device. This means that the high-level injection effect in a parasitic p-n-p-n structure of CMOS IC's will happen very early during latchup transition. The beginning of high-level injection effect in BJT's Q_1 and Q_2 not only stops the increase of g_{C1} and g_{C2} but also further decreases the ratios of g_{C1}/g_{B1} and g_{C2}/g_{B2}. This effect stops the increase of p_1 pole and then it gradually decreases.
5) With gradually decrease of p_1 pole, it will change from positive to negative at a certain time dependent on the strength of high-level injection effect in the p-n-p-n structure. After then, the negative p_1 and p_2 poles make $v_{EB1}(t)$ and $v_{BE2}(t)$ stop to increase but stay at their final stable values. Finally, the p-n-p-n structure will hold in its stable latching state and a low-impedance path is formed from V_{DD} supply to ground.

Corresponding to the *HSPICE* simulated $v_{EB1}(t)$ and $v_{BE2}(t)$ in Fig. 2, the time-varying transient poles can be calculated from (21) and (22) at each time interval. The calculated results are shown in Fig. 3 in both latchup and nonlatchup cases. As above descriptions, p_2 pole varies in time and is always negative in both latchup and nonlatchup cases, but p_1 pole in the latchup case indeed changes from negative to positive and then becomes negative again during latchup transition. Under the triggering of 5-mA I_1 with only 3.5-nS pulse width, p_1 pole increases a little but does not further becomes positive. Thus, a necessary condition to initiate the occurrence of latchup is that trigger signals must sustain long enough in time to push p_1 pole to become positive.

Through (19)–(23), the positive-feedback regenerative process in a p-n-p-n structure can be modeled by this time-varying positive transient pole. The beginning of positive-feedback regeneration is on the time when p_1 pole changes from negative to positive. The intensity of positive-feedback regeneration can be characterized by the value of positive pole during latchup transition. The maximum peak value of positive p_1 pole and the time required to initiate this positive pole can be adopted as two important parameters to quantitatively model the positive-feedback regeneration in a p-n-p-n structure. They are marked as the $p_{1(\max)}$ and t_r in Fig. 3, respectively. Using these two parameters, the influence of device parameters in a p-n-p-n structure on its positive-feedback regeneration during latchup transition can be quantitatively investigated in details.

Besides, a p-n-p-n structure can be latchup-free if the term in (23) is always positive. There are two ways to get a positive value of (23). One is to reduce the ratio of $(g_{C1} \cdot g_{C2})/(g_{B1} \cdot g_{B2})$ which is corresponding to the product of beta gains in BJT's Q_1 and Q_2. The other is to reduce the parasitic substrate and well resistances. As Rs and Rw are small enough, the term in (23) can be positive even if the ratio of $(g_{C1} \cdot g_{C2})/(g_{B1} \cdot g_{B2})$ is large in a p-n-p-n structure. This provides us with a way to prevent CMOS latchup.

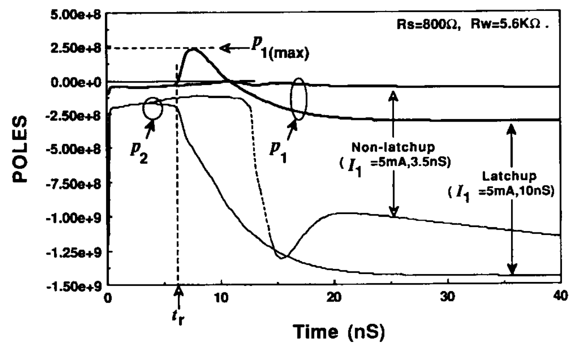


Fig. 3. The calculated time-varying transient poles in both latchup and nonlatchup cases with the corresponding base-emitter voltages of Fig. 2.

Appendix A

To simplify model calculation, the bias-dependent capacitances can be estimated as bias-independent averaged values in each operating voltage range [12].

The averaged diffusion capacitance of a forward-biased base-emitter junction over its voltage range from v_{BEa} to v_{BEb} can be derived as

$$\begin{aligned}\overline{C_{\tau be}} &= \frac{1}{v_{BEb} - v_{BEa}} \cdot \int_{v_{BEa}}^{v_{BEb}} C_{\tau be} \cdot dv_{BE} \\ &= \frac{\tau_F \cdot I_S}{v_{BEb} - v_{BEa}} \\ &\quad \cdot \left[\frac{e^{v_{BEb}/V_T \cdot N_F} - 1}{q_b(v_{BEb})} - \frac{e^{v_{BEa}/V_T \cdot N_F} - 1}{q_b(v_{BEa})}\right]. \end{aligned} \tag{A.1}$$

Similarly, the averaged diffusion capacitance of a reverse-biased base-collector junction with its operating voltage range from v_{BCa} to v_{BCb} is

$$\overline{C_{\tau bc}} = \frac{\tau_R \cdot I_S}{v_{BCb} - v_{BCa}} \cdot \left[e^{v_{BCb}/V_T \cdot N_R} - e^{v_{BCa}/V_T \cdot N_R}\right]. \tag{A.2}$$

In CMOS technology, the base-emitter junctions of the parasitic lateral p-n-p BJT Q_1 and the parasitic vertical n-p-n BJT Q_2 are nearly abrupt junctions whereas the base-collector junctions of these BJT's are nearly grading junctions. The averaged depletion capacitance of an abrupt base-emitter junction over its biasing voltage range from v_{BEa} to v_{BEb} can be derived as

$$\begin{aligned}\overline{C_{jbe}} &= \frac{2 \cdot \Phi_E \cdot C_{je0}}{v_{BEb} - v_{BEa}} \\ &\quad \cdot \left[\left(1 - \frac{v_{BEa}}{\Phi_E}\right)^{(1/2)} - \left(1 - \frac{v_{BEb}}{\Phi_E}\right)^{(1/2)}\right] \end{aligned} \tag{A.3}$$

when $v_{BEa} < v_{BEb} < (\Phi_E/2)$,

$$\begin{aligned}\overline{C_{jbe}} &= \frac{C_{je0}}{v_{BEb} - v_{BEa}} \\ &\quad \cdot \left\{ 2 \cdot \Phi_E \cdot \left[\left(1 - \frac{v_{BEa}}{\Phi_E}\right)^{(1/2)} - \left(\frac{1}{2}\right)^{(1/2)}\right] \right. \\ &\quad \left. + \frac{\left(v_{BEb} - \frac{\Phi_E}{2}\right)}{4 \cdot (0.5)^{3/2}} \cdot \left[1 + \frac{\left(v_{BEb} + \frac{\Phi_E}{2}\right)}{\Phi_E}\right] \right\} \end{aligned} \tag{A.4}$$

when $v_{BEa} < (\Phi_E/2) < v_{BEb}$,

$$\overline{C_{jbe}} = \frac{C_{je0}}{4 \cdot (0.5)^{3/2}} \cdot \left[1 + \frac{(v_{BEb} + v_{BEa})}{\Phi_E}\right] \tag{A.5}$$

when $v_{BEb} > v_{BEa} > (\Phi_E/2)$.

The averaged depletion capacitance of a reverse-biased grading base-collector junction over its operating voltage range from v_{BCa} to v_{BCb} is

$$\begin{aligned}\overline{C_{jbc}} &= \frac{\frac{3}{2} \cdot \Phi_C \cdot C_{jc0}}{v_{BCb} - v_{BCa}} \\ &\quad \cdot \left[\left(1 - \frac{v_{BCa}}{\Phi_C}\right)^{2/3} - \left(1 - \frac{v_{BCb}}{\Phi_C}\right)^{2/3}\right] \end{aligned} \tag{A.6}$$

when $v_{BCb} < v_{BCa} < 0$.

Substituting the proper operating voltage ranges of the transistors Q_1 and Q_2 into the above equations, the bias-independent piecewise-averaged junction diffusion and depletion capacitances can be obtained.

APPENDIX B

The first-order piecewise-linearized base and collector current equations of BJT's Q_1 and Q_2 can be approximated at each time interval as

$$I_{B1} \cong I_{B10} + g_{B1} \cdot v_{EB1} \tag{B.1}$$

$$I_{C1} \cong I_{C10} + g_{C1} \cdot v_{EB1} \tag{B.2}$$

$$I_{B2} \cong I_{B20} + g_{B2} \cdot v_{BE2} \tag{B.3}$$

$$I_{C2} \cong I_{C20} + g_{C2} \cdot v_{BE2} \tag{B.4}$$

From the *HSPICE* step-by-step simulated results, the base-emitter and base-collector voltages during latchup transition can be obtained. At the certain time interval τ_k, the simulated base-emitter and base-collector voltages of BJT Q_1 are denoted as V_{EB1a} and V_{CB1a}, respectively. While at the next time interval τ_{k+1}, those voltages are denoted as V_{EB1b} and V_{CB1b}. The large-signal transconductances of base and collector currents in (B.1) and (B.2) with respect to its base-emitter voltage of BJT Q_1 are defined as

$$\begin{aligned} g_{B1} &\equiv \frac{\Delta I_{B1}}{\Delta v_{EB1}} \\ &= \frac{I_{B1}(V_{EB1b}, V_{CB1b}) - I_{B1}(V_{EB1a}, V_{CB1a})}{V_{EB1b} - V_{EB1a}} \end{aligned} \tag{B.5}$$

$$\begin{aligned} g_{C1} &\equiv \frac{\Delta I_{C1}}{\Delta v_{EB1}} \\ &= \frac{I_{C1}(V_{EB1b}, V_{CB1b}) - I_{C1}(V_{EB1a}, V_{CB1a})}{V_{EB1b} - V_{EB1a}} \end{aligned} \tag{B.6}$$

and the piecewise-linearized initial currents are

$$I_{B10} \equiv I_{B1}(V_{EB1b}, V_{CB1b}) - g_{B1} \cdot V_{EB1b} \tag{B.7}$$

$$I_{C10} \equiv I_{C1}(V_{EB1b}, V_{CB1b}) - g_{C1} \cdot V_{EB1b}. \tag{B.8}$$

Similar technique is also applied to I_{B2} and I_{C2} of BJT Q_2 to determine the piecewise-linearized parameters of g_{B2}, g_{C2}, I_{B20}, and I_{C20} in (B.3) and (B.4).

VI. CONCLUSION

A new method to characterize the positive-feedback regeneration of CMOS latchup transition has been developed. Based on conventional two-transistor lumped equivalent circuit with extracted device parameters in the p-n-p-n structure, the large-signal base-emitter voltages of the parasitic vertical and lateral BJT's can be represented as two-pole functions of time at each time interval. One of the poles is found to change from negative to positive during the turn-on process of CMOS latchup. The occurrence of the positive pole means the happening of the positive-feedback regeneration in the p-n-p-n structure. The positive-feedback regeneration is found to have a double exponential increase rate of time. This very fast and complex regenerative process has been clearly explained and quantitatively characterized by the time-varying positive transient pole. The maximum positive pole and the time required to initiate the positive pole can be adopted as two important parameters to quantitatively investigate the influence of device parameters on the positive-feedback regeneration of CMOS latchup.

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REFERENCES

[1] D. A. Suda, R. E. Hayes, and A. S. Rohlev, "Transient analysis of p-n-p-n optoelectronic devices," *IEEE Trans. Electron Devices,* vol. 39, no. 8, pp. 1858–1864, 1992.

[2] D. B. Estreich and R. W. Dutton, "Modeling latch-up in CMOS integrated circuits," *IEEE Trans. Computer-Aided Design of Integrated Circuits Syst.,* vol. CAD-1, no. 4, pp. 157–162, 1982.

[3] R. D. Rung and H. Momose, "DC holding and dynamic triggering characteristics of bulk CMOS latchup," *IEEE Trans. Electron Devices,* vol. ED-30, no. 12, pp. 1647–1655, 1983.

[4] R. C.-Y. Fang and J. L. Moll, "Latchup model for the parasitic p-n-p-n path in bulk CMOS," *IEEE Trans. Electron Devices,* vol. ED-31, no. 1, pp. 113–120, 1984.

[5] R. R. Troutman and H. P. Zappe, "Layout and bias considerations for preventing transiently triggered latchup in CMOS," *IEEE Trans. Electron Devices,* vol. ED-31, no. 3, pp. 315–321, 1984.

[6] K. Y. Fu, "Transient latchup in bulk CMOS with a voltage-dependent well-substrate junction capacitance," *IEEE Trans. Electron Devices,* vol. ED-32, no. 3, pp. 717–720, 1985.

[7] L. Chang and J. Berg, "Substrate bias effects on transiently triggered latchup in bulk CMOS," *IEEE Trans. Electron Devices,* vol. ED-33, no. 1, pp. 165–167, 1986.

[8] G. Goto, H. Takahashi, and T. Nakamura, "Modeling and analysis of transient latchup in double-well bulk CMOS," *IEEE Trans. Electron Devices,* vol. ED-33, no. 9, pp. 1341–1347, 1986.

[9] R. R. Troutman and H. P. Zappe, "A transient analysis of latchup in bulk CMOS," *IEEE Trans. Electron Devices,* vol. ED-30, no. 2, pp. 170–179, 1983.

[10] G. J. Hu, "A better understanding of CMOS latch-up," *IEEE Trans. Electron Devices,* vol. ED-31, no. 1, pp. 62–67, 1984.

[11] W. Li and M. E. Nokali, "Transient analysis for a new CMOS latchup model," *Solid-State Electronics,* vol. ED-30, no. 12, pp. 1331–1339, 1987.

[12] Y.-H. Yang and C.-Y. Wu, "A new criterion for transient latchup analysis in bulk CMOS," *IEEE Trans. Electron Devices,* vol. ED-36, no. 7, pp. 1336–1347, 1989.

[13] M.-D. Ker and C.-Y. Wu, "Transient analysis of submicron CMOS latchup with a physical criterion," *Solid-State Electron.,* vol. 37, no. 2, pp. 255–273, Feb. 1994.

[14] M. R. Pinto and R. W. Dutton, "Accurate trigger condition analysis for CMOS latchup," *IEEE Electron Device Lett.,* vol. EDL-6, no. 2, pp. 100–102, 1985.

[15] S. Odanaka, M. Wakabayashi, and T. Ohzone, "The dynamics of latchup turned-on behavior in scaled CMOS," *IEEE Trans. Electron Devices,* vol. ED-32, no. 7, pp. 1334–1340, 1985.

[16] J. Harter, H. Jacobs, M. Zwar, and H. Skapa, "Quasi-two-dimensional simulation of transient latchup effect in VLSI CMOS circuits," *IEEE Trans. Electron Devices,* vol. ED-32, no. 9, pp. 1665–1669, 1985.

[17] W.-H. Chang and M. D. Rodriguez, "Transient switching of the parasitic bipolar device of an epitaxial CMOS transistor," *IEEE Electron Device Lett.,* vol. EDL-8, no. 6, pp. 275–276, 1987.

[18] M. Strzempa-Depre, J. Harter, C. Werner, H. Skapa, and R. Kassing, "Static and transient latchup simulation of VLSI-CMOS with an improved physical design model," *IEEE Trans. Electron Devices,* vol. ED-34, no. 6, pp. 1290–1296, 1987.

[19] T. Ohzone and H. Iwata, "Transient latchup characteristics in n-well CMOS," *IEEE Trans. Electron Devices,* vol. 39, no. 8, pp. 1870–1875, 1992.

[20] T. Misawa, "Turn-on transient of p-n-p-n triode," *J. Electron. Contr.,* vol. 7, no. 6, pp. 523–533, 1959.

[21] G. D. Bergman, "The gate-triggered turn-on process in thyristors," *Solid-State Electron.,* vol. 8, pp. 757–765, 1965.

[22] J. McGhee, "A transient model for a three terminal p-n-p-n switch and its use in predicting the gate turn-on process," *Int. J. Electron.,* vol. 35, no. 1, pp. 73–79, 1973.

[23] A. A. Jaecklin, "Turn-on phenomena in optically and electrically fired thyristors," *IEEE Trans. Electron Devices,* vol. ED-29, no. 10, pp. 1552–1560, 1982.

[24] P. Voss, "Observation of the initial phases of thyristor turn-on," *Solid-State Electron.*, vol. 17, pp. 879–880, 1974.
[25] I. V. Grekhov, M. E. Levinshtein, and V. G. Sergeev, "Investigation of the propagation of the turned-on state along a p-n-p-n structure," *Soviet Physics—Semiconductors*, vol. 4, no. 11, pp. 1844–1849, 1971.
[26] R. L. Davies and J. Petruzella, "P-n-p-n charge dynamics," *IEEE Proceedings*, vol. 55, no. 8, pp. 1318–1330, 1967.
[27] J. Cornu and A. A. Jaecklin, "Processes at turn-on of thyristors," *Solid-State Electron.*, vol. 18, pp. 683–689, 1975.
[28] F. Dannhauser and P. Voss, "A quasi-stationary treatment of the turn-on delay phase of one-dimensional thyristor: Part I—Theory," *IEEE Trans. Electron Devices*, vol. ED-23, no. 8, pp. 928–939, 1976.
[29] A. A. Jaecklin, "The first dynamic phase at turn-on of a thyristor," *IEEE Trans. Electron Devices*, vol. ED-23, no. 8, pp. 940–944, 1976.
[30] M. S. Adler and V. A. K. Temple, "The dynamics of the thyristor turn-on process," *IEEE Trans. Electron Devices*, vol. ED-27, no. 2, pp. 483–494, 1980.
[31] C.-Y. Wu, Y.-H. Yang, C. Chang, and C.-C. Chang, "A new approach to model CMOS latchup," *IEEE Trans. Electron Devices*, vol. ED-32, no. 9, pp. 1642–1653, 1985.
[32] J. L. Moll, M. Tanenbaum, J. M. Goldey, and N. Holonyak, "p-n-p-n transistor switches," *IRE Proceedings*, vol. 44, pp. 1174–1182, 1956.
[33] I. M. Mackintosh, "The electrical characteristics of silicon p-n-p-n triodes," *IRE Proceedings*, vol. 46, pp. 1229–1235, 1958.
[34] W. Fulop, "Three terminal measurements of current amplification factors of controlled rectifiers," *IEEE Trans. Electron Devices*, vol. ED-10, pp. 120–135, 1963.
[35] F. E. Gentry, "Turn-on criterion for p-n-p-n devices," *IEEE Trans. Electron Devices*, vol. ED-11, p. 74, 1964.
[36] J. F. Gibbons, "A critique of the theory of p-n-p-n devices," *IEEE Trans. Electron Devices*, vol. ED-11, pp. 406–413, 1964.
[37] M. Klein, "A four-terminal p-n-p-n switching device," *IEEE Trans. Electron Devices*, vol. ED-7, pp. 214–217, 1960.
[38] J. J. Ebers, "Four-terminal p-n-p-n transistors," *IRE Proceedings*, vol. 40, pp. 1361–1364, 1952.
[39] E. C. Sangiorgi, M. R. Pinto, S. E. Swirhun, and R. W. Dutton, "Two-dimensional numerical analysis of latchup in a VLSI CMOS technology," *IEEE Trans. Electron Devices*, vol. ED-32, no. 10, pp. 2117–2130, 1985.
[40] E. Sangiorgi, B. Ricco, and L. Selmi, "Three-Dimensional distribution of CMOS latch-up current," *IEEE Electron Device Lett.*, vol. EDL-8, no. 4, pp. 154–156, 1987.
[41] D. J. Sleeter and E. W. Enlow, "The relationship of holding points and a general solution for CMOS latchup," *IEEE Trans. Electron Devices*, vol. 39, no. 11, pp. 2592–2599, 1992.
[42] I. E. Getreu, *Modeling the Bipolar Transistor.* OR: Tektronix, 1976.
[43] P. Antognetti and G. Massobrio, *Semiconductor Device Modeling with SPICE.* New York: McGraw-Hill, 1988.
[44] *HSPICE User's Manual.* CA: Meta-Software, Inc., 1990.
[45] R. R. Troutman, *Latchup in CMOS Technology: The Problem and Its Cure.* Norwell, MA: Kluwer Academic, 1986.
[46] A. Blicher, *Thyristor Physics.* New York: Springer-Verlag, 1976.
[47] G. Krieger, "The effect of emitter current crowding on CMOS latchup characteristics," *IEEE Trans. Electron Devices*, vol. ED-34, no. 7, pp. 1525–1532, 1987.

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