

# Capacitor-Couple ESD Protection Circuit for Deep-Submicron Low-Voltage CMOS ASIC

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**Abstract**—Capacitor-couple technique used to lower snapback-trigger voltage and to ensure uniform ESD current distribution in deep-submicron CMOS on-chip ESD protection circuit is proposed. The coupling capacitor is realized by a poly layer right under the wire-bonding metal pad without increasing extra layout area to the pad. A timing-original design model has been derived to calculate the capacitor-couple efficiency of this proposed ESD protection circuit. Using this capacitor-couple ESD protection circuit, the thinner gate oxide of CMOS devices in deep-submicron low-voltage CMOS ASIC can be effectively protected.

## I. INTRODUCTION

AS CMOS technology is scaled down into deep-submicron regime, the advanced processes, such as thinner gate oxide, shorter channel length, shallower source/drain junction, LDD structure, and silicided diffusion, much degrade ESD robustness of CMOS IC's [1]–[2]. To achieve the required ESD robustness, the protection devices in submicron CMOS ESD protection circuits are often designed with much larger dimensions than those in traditional long-channel CMOS technologies. But from the practical viewpoint of high-integration applications, the pin counts of CMOS VLSI/ULSI are often more than 200. In such high-pin-count CMOS IC, especially in the pad-limited ASIC design, layout area available for each pad with input ESD protection circuit or output buffer including latchup guard rings is seriously limited. Hence, an ESD protection circuit of high ESD robustness with smaller layout area becomes more difficult to be designed in deep-submicron CMOS technology.

Recently, there are three approaches to improve ESD robustness of submicron CMOS IC's. One is in process level to add an extra mask of "ESD implant" into the process flow to make a stronger structure for input/output devices [3]–[4]. But, the cost of chip fabrication is increased. Another approach is in device level to use low-voltage-trigger lateral SCR (LVTSCR) devices to protect submicron CMOS IC's [5]–[7]. Lateral SCR device can perform very high ESD robustness, but the turn-on mechanism is difficult to simulate and needs more experience to control it [8]. The third approach is in circuit level to adopt "gate-couple" technique to achieve uniform power distribution among the multiple fingers of output NMOS device with large

dimension [9]–[11]. A "GCNMOS (gate-coupled NMOS)" structure [9]–[10], in which an  $N$ -type field-oxide device was used to couple ESD-transient voltage to the gate of output NMOS, was reported to uniformly turn on the multiple fingers of large-dimension output NMOS during ESD transition. In [11], an extra thin-oxide NMOS was used as a capacitor to enhance gate-couple effect, where its drain and source were both connected to the gate of ESD-discharging NMOS but its gate was connected to the pad. Coupled voltage on the gate of ESD-discharging NMOS was sustained by a  $10\text{ K}\Omega$   $N$ -well resistor. Although these reports [9]–[11] can improve ESD reliability, they need other auxiliary devices (such as field-oxide device, thin-oxide NMOS, or  $N$ -well resistor) to perform the gate-couple function. These auxiliary devices occupy extra layout area to the pad. This somewhat limits their applications in the high-pin-count CMOS ASIC without increasing total layout area of the chip.

Besides, since ESD voltages may have positive or negative polarities to both  $V_{DD}$  and  $V_{SS}$  (ground), there are four ESD-stress conditions at each input (or output) pin as shown in Fig. 1.

- 1) *PS Mode*: ESD stress on a pin with positive voltage polarity to  $V_{SS}(\text{GND})$  pin when  $V_{DD}$  pin and other input/output pins are floating.
- 2) *NS Mode*: ESD stress on a pin with negative voltage polarity to  $V_{SS}(\text{GND})$  pin when  $V_{DD}$  pin and other input/output pins are floating.
- 3) *PD Mode*: ESD stress on a pin with positive voltage polarity to  $V_{DD}$  pin when  $V_{SS}(\text{GND})$  pin and other input/output pins are floating.
- 4) *ND Mode*: ESD stress on a pin with negative voltage polarity to  $V_{DD}$  pin when  $V_{SS}(\text{GND})$  pin and other input/output pins are floating.

These ESD voltages could damage both NMOS and PMOS devices in the input stage or output buffer of CMOS IC's. In [9]–[11], GCNMOS device is only arranged between the pad and  $V_{SS}(\text{GND})$ . There is no ESD protection element arranged between the pad and  $V_{DD}$ . In the ND-mode or PD-mode ESD stress, the internal circuits are dangerous to ESD damage. Fig. 2 shows a schematic diagram to explain the unexpected discharging paths in the internal part of a CMOS IC under the ND-mode ESD-stress condition, in which it only has an input-to- $V_{SS}$  ESD protection circuit at the input pad. The ND-mode ESD voltage between input pad and  $V_{DD}$  pad is first transferred to the  $V_{SS}$  power line through the input-to- $V_{SS}$  ESD protection circuit. This causes

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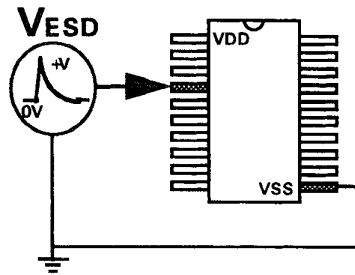
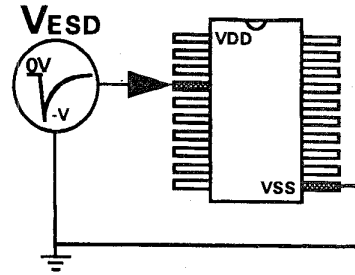
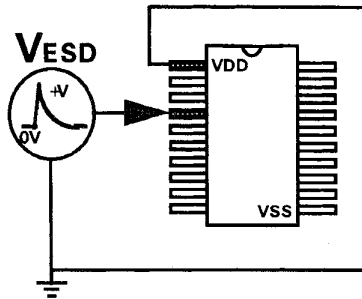
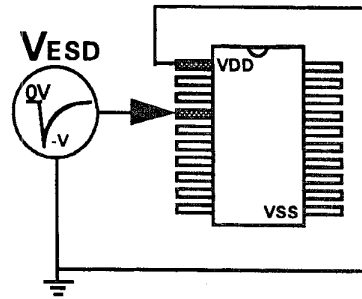
**(1) PS-mode****(2) NS-mode****(3) PD-mode****(4) ND-mode**

Fig. 1. The four modes of ESD stress on an input (or output) pin of CMOS IC.

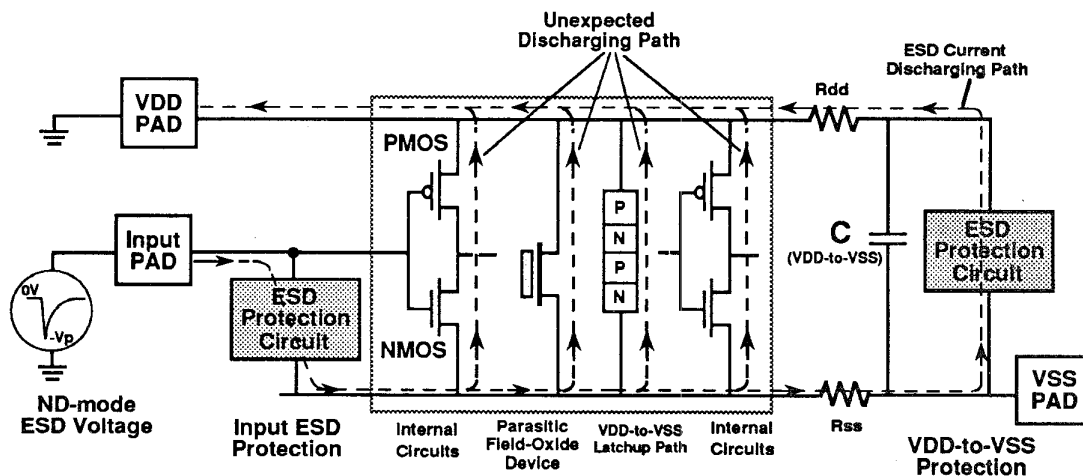


Fig. 2. Unexpected ESD discharging paths along the internal circuits beyond input-to- $V_{SS}$  and  $V_{DD}$ -to- $V_{SS}$  ESD protection circuits.

voltage stress between  $V_{SS}$  and  $V_{DD}$  power lines. Due to the parasitic resistance and capacitance along  $V_{SS}/V_{DD}$  power lines in CMOS IC's as well as the voltage drops on the input-to- $V_{SS}$  and  $V_{DD}$ -to- $V_{SS}$  ESD protection elements, such nondirect ESD discharging path had been reported to cause some unexpected ESD damages on internal circuits beyond ESD protection circuits [12]–[16]. Thus, an ESD protection circuit for advanced submicron CMOS IC's should perform

effective and direct ESD discharging path from input and output pads to both  $V_{SS}$  and  $V_{DD}$  power lines. This is especially necessary for deep-submicron CMOS ASIC with larger chip size and longer  $V_{DD}/V_{SS}$  power lines which often surround the whole chip.

Moreover, in deep-submicron CMOS technology, the thickness of gate oxide had been scaled down to be thinner [2]. This much thinner gate oxide is more sensitive to ESD stress. For

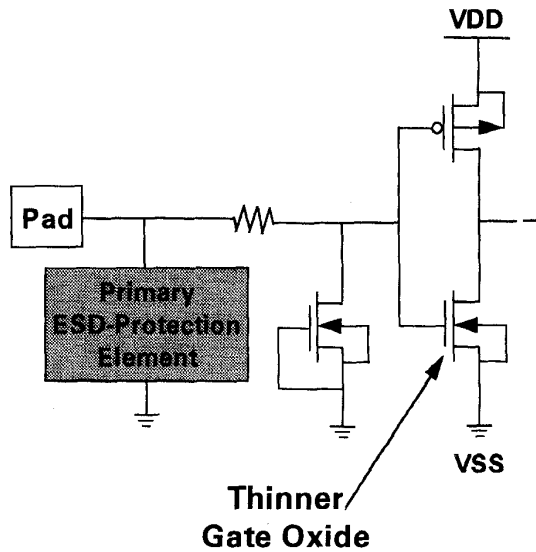


Fig. 3. A conventional input ESD protection circuit with gate-grounded NMOS to clamp ESD voltage across the gate oxide of input stage.

ESD protection of the input pad, the gate-grounded NMOS device is often used as the secondary protection element to clamp ESD voltage across the gate oxide of input stage. A conventional input ESD protection circuit is shown in Fig. 3. ESD voltage across the input gate oxide is initially clamped by the snapback-trigger voltage (due to punchthrough or avalanche breakdown) of gate-grounded NMOS [17]–[19]. But, the voltage margin between gate-oxide breakdown and snapback breakdown is also much reduced in deep-submicron low-voltage CMOS technology. If the drain breakdown voltage of the gate-grounded NMOS is near to (or even higher than) the gate-oxide breakdown voltage, the gate oxide of input stage could be first ruptured by ESD voltage even if there is a gate-grounded NMOS to protect it. This condition is easy to happen, especially in deep-submicron low-voltage CMOS technology with much thinner gate oxide. Thus, the voltage difference between the gate-oxide breakdown and the drain snapback breakdown of short-channel NMOS device is an important voltage margin for ESD design.

In this paper, a capacitor-couple ESD protection scheme is proposed to overcome above issues. Not only to ensure uniform ESD current distribution but also to lower snapback-trigger voltage of NMOS and PMOS devices, this proposed capacitor-couple ESD protection circuit can perform effective ESD protection for deep-submicron low-voltage CMOS ASIC with thinner gate oxide. This work has been successfully verified in a  $0.5\ \mu\text{m}$  3 V CMOS technology with thinner gate oxide of  $90\ \text{\AA}$  [20].

## II. CHARACTERISTICS OF CMOS DEVICES FOR ESD PROTECTION

The operating region of gate-grounded NMOS device for ESD protection is in its snapback region [18]. ESD failure threshold of MOS device was found to be strongly correlated to the snapback voltage of parasitic lateral bipolar action

in MOS device [19]. The ESD robustness of MOS device is increased as its snapback voltage is decreased. Snapback voltage depends on device parameters such as junction profile, channel length, and gate bias. To find general application for on-chip ESD protection without modifying the CMOS process, the effort in this section is focused to find the dependence of gate bias on the snapback-trigger voltage of short-channel CMOS devices.

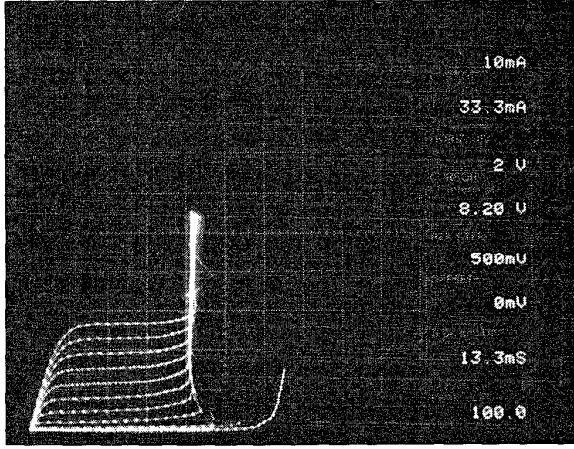
The curves shown in Fig. 4(a) are I-V characteristics of drain snapback breakdown of NMOS device with channel length of  $0.8\ \mu\text{m}$  under various positive gate biases. As there is positive voltage on its gate, NMOS device is turned on to conduct current from drain to source. If drain voltage is still increased, NMOS will finally enter into its snapback region. In Fig. 4(a), the holding voltage for NMOS in its snapback region is about 8.2 V. Before thermal breakdown (or called as second breakdown), NMOS device can be safe in its snapback region to conduct current. But, the I-V curve for NMOS entering into its snapback region under positive gate bias is quite different to that of NMOS with gate grounded. The snapback-trigger voltage obviously decreases as its gate voltage increases. The dependence of this gate-biased effect on NMOS snapback-trigger voltage is shown in Fig. 4(b), where the snapback-trigger voltage can be lowered from 13 V to about 8.5 V. A short-channel PMOS also has similar I-V characteristics to those of NMOS due to lateral *p-n-p* bipolar action. Fig. 5(a) shows the I-V curves of PMOS device with channel length of  $0.8\ \mu\text{m}$  under various negative gate biases. The dependence of gate-biased effect on PMOS snapback-trigger voltage is shown in Fig. 5(b) where the magnitude of snapback-trigger voltage is reduced as its gate-to-source voltage  $V_{gs}$  is more negative.

This gate-biased effect on short-channel NMOS and PMOS devices lights us a way to more effectively protect the thinner gate oxide of deep-submicron low-voltage CMOS IC's even without ESD-implant process. The holding voltage of snapback region in short-channel NMOS and PMOS devices due to lateral bipolar action is much lower than its drain snapback-breakdown voltage (under 0-V gate bias). If suitable ESD-transient voltage is coupled to the gate of ESD-protection NMOS/PMOS device under ESD-stress condition, the snapback-trigger voltage of ESD-protection device can be reduced. Therefore, the lateral bipolar action in ESD-protection NMOS/PMOS device can be earlier triggered on to bypass ESD current. Then, ESD voltage is clamped by the lower snapback holding voltage. Based on this concept, a capacitor-couple ESD protection circuit is proposed to effectively protect the thinner gate oxide of CMOS devices in deep-submicron low-voltage CMOS ASIC without process modification to save fabrication cost.

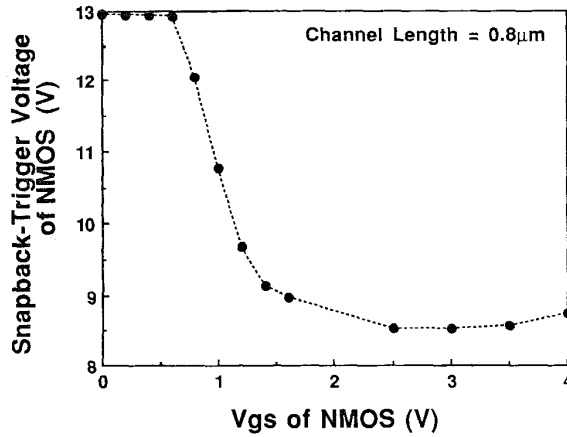
## III. CAPACITOR-COUPLE ESD PROTECTION CIRCUIT

### A. Circuit Configuration

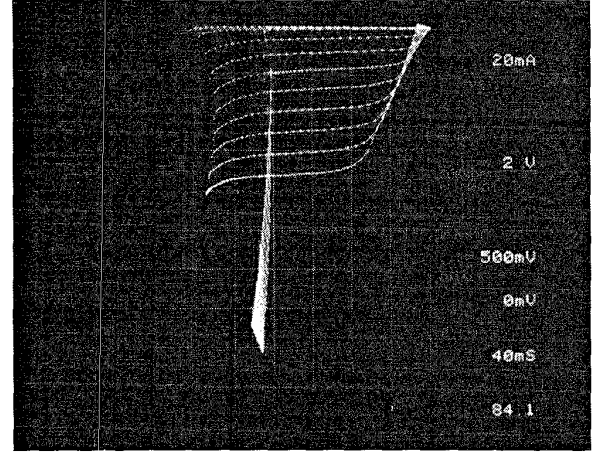
The capacitor-couple ESD protection circuit for input pad to ensure uniform ESD current flow, as well as, to lower snapback-trigger voltage of ESD-protection devices is shown



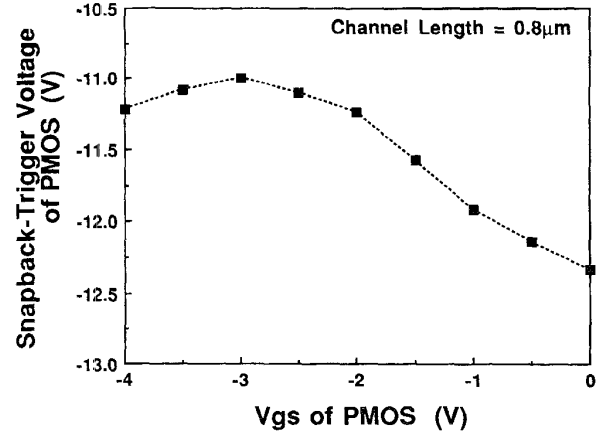
(a)



(b)



(a)



(b)

Fig. 4. (a) The I-V characteristics of drain snapback breakdown of short-channel thin-oxide NMOS device with different gate biases from 0 to 5 V. (b) The dependence of gate-biased effect on NMOS snapback-trigger voltage.

Fig. 5. (a) The I-V characteristics of drain snapback breakdown of short-channel thin-oxide PMOS device with different gate biases from 0 to -5 V. (b) The dependence of gate-biased effect on PMOS snapback-trigger voltage.

in Fig. 6. In Fig. 6, there is a thin-oxide PMOS (NMOS) device Mp1 (Mn1) arranged between input pad and  $V_{DD}$  ( $V_{SS}$ ). A capacitor  $C_p$  ( $C_n$ ) is connected between the gate of Mp1 (Mn1) and the input pad. A resistor  $R_p$  ( $R_n$ ) is connected between the gate of Mp1 (Mn1) and  $V_{DD}$  ( $V_{SS}$ ). The drain of Mp1 (Mn1) is connected to the input pad, whereas the source of Mp1 (Mn1) is connected to  $V_{DD}$  ( $V_{SS}$ ). There also exists a junction diode Dp1 (Dn1) between the input pad and  $V_{DD}$  ( $V_{SS}$ ) with its anode connected to the input pad ( $V_{SS}$ ) and its cathode connected to  $V_{DD}$  (the input pad). This diode Dp1 (Dn1) is inherently formed by the parasitic  $p$ - $n$  junction between drain and bulk of Mp1 (Mn1) device. A poly resistor  $R$  is connected from input pad to internal circuits.

Capacitor  $C_p$  ( $C_n$ ) is designed to couple suitable ESD-transient voltage to the gate of Mp1 (Mn1) to lower snapback-trigger voltage of Mp1 (Mn1). With lower snapback-trigger voltage, Mp1 and Mn1 can be earlier triggered into their snapback regions to bypass ESD current. Resistor  $R_p$  ( $R_n$ ) is designed to sustain the coupled voltage longer in time on the

gate of Mp1 (Mn1) to help Mp1 (Mn1) device into its snapback region with lower snapback-trigger voltage. The four modes of ESD stress are one-by-one protected by this capacitor-couple ESD protection circuit to avoid the unexpected ESD damage in internal circuits.

### B. Operating Principles

In normal CMOS operating condition with  $V_{DD}$  and  $V_{SS}$  power supplies, the high (low) voltage level of input signal is clamped by Dp1 (Dn1) to about  $V_{DD} + 0.6$  V ( $V_{SS} - 0.6$  V). Because the gate of Mp1 (Mn1) is connected to  $V_{DD}$  ( $V_{SS}$ ) through resistor  $R_p$  ( $R_n$ ), Mp1 (Mn1) is always kept off during normal operations of CMOS IC's. Thus, the capacitor-couple ESD protection circuit is inactive as CMOS IC is in normal operating condition, as well as the voltage level of input signal can be clamped between  $V_{DD} + 0.6$  V and  $V_{SS} - 0.6$  V.

In ESD-stress condition, there are four modes of ESD stress on a pad as those shown in Fig. 1. As PS-mode ESD stress

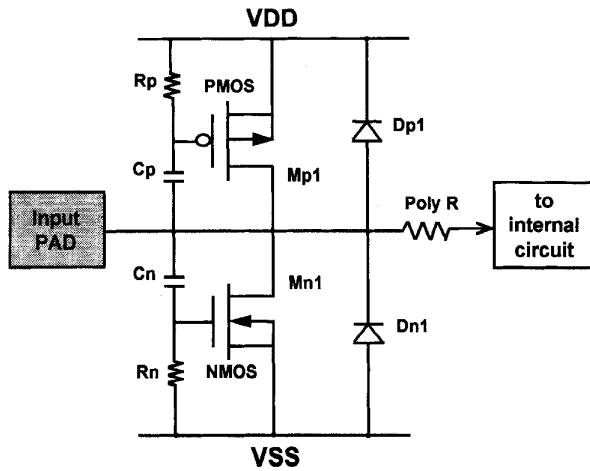


Fig. 6. The proposed capacitor-couple ESD protection circuit.

occurs on the input pad of Fig. 6, ESD-transient voltage is coupled to the gate of Mn1 through capacitor  $C_n$ . Because ESD event is inherently a quick transition, capacitor  $C_n$  can be designed to couple ESD-transient voltage to the gate of Mn1. This coupled voltage on the gate of Mn1 leads to lower snapback-trigger voltage of Mn1 to avoid overstress across the gate oxide of input stage. With lower snapback-trigger voltage, Mn1 can be quickly triggered into its snapback region to bypass ESD current. ESD voltage on the pad is clamped to the snapback holding voltage of Mn1 about 8.2 V, which is below the gate-oxide breakdown voltage. The suitable  $C_n(R_n)$  to couple (sustain) gate voltage for lowering snapback-trigger voltage of Mn1 can be easily designed with consideration on device dimension of Mn1.

As NS-mode (PD-mode) ESD stress occurs on the input pad, diode Dn1 (Dp1) is forward biased to bypass ESD current. The negative (positive) ESD voltage on the input pad will be clamped to about  $-0.6$  V ( $+0.6$  V), so the internal circuits can be protected against ESD damage. Diode under forward-biased condition can sustain very high ESD stress.

As ND-mode ESD stress occurs on the input pad with relatively grounded VDD, negative ESD-transient voltage is coupled to the gate of Mp1 through capacitor  $C_p$ . This coupled voltage on the gate of Mp1 leads to lower snapback-trigger voltage to avoid overstress across the gate oxide of input stage. With lower snapback-trigger voltage, Mp1 can be quickly triggered into its snapback region to bypass ESD current and clamp the negative ESD voltage to its snapback holding voltage. Suitable  $C_p(R_p)$  to couple (sustain) gate voltage for lowering snapback-trigger voltage of Mp1 can be easily designed with consideration on device dimension of Mp1.

The four modes of ESD stress on the input pad are one-by-one protected by the capacitor-couple Mn1, diode Dn1, diode Dp1, and capacitor-couple Mp1, respectively. The magnitude and holding time of coupled voltage on the gate of Mn1 (Mp1) can be adjusted by  $C_n$  and  $R_n$  ( $C_p$  and  $R_p$ ) to make ESD-protection device active only in ESD-stress condition but inactive in normal operating condition of CMOS IC's. A design model has been developed in next section to calculate

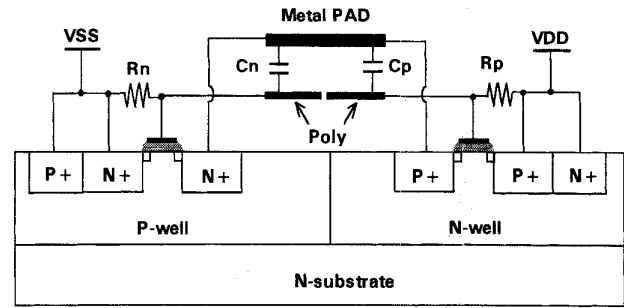


Fig. 7. Schematic cross-sectional view of the capacitor-couple ESD protection circuit.

suitable  $C_n$  and  $R_n$  ( $C_p$  and  $R_p$ ) for this capacitor-couple ESD protection circuit.

### C. Realization of Capacitor-Couple ESD Protection Circuit

There are several ways to realize coupling capacitor and sustaining resistor in deep-submicron CMOS technology. The most efficient way to achieve this capacitor-couple effect without increasing total layout area to the pad has been shown in Fig. 7. In Fig. 7, it is a schematic cross-sectional view of this capacitor-couple ESD protection circuit, where the  $n$ -substrate twin-well CMOS technology is used to demonstrate device structure. This capacitor-couple ESD protection circuit can be realized in any CMOS or BiCMOS technologies with  $p$ -well,  $n$ -well, or twin-well structure in  $p$ -type or  $n$ -type substrate. To achieve the capacitor-couple effect without increasing extra layout area to the pad,  $C_n$  and  $C_p$  are realized by inserting the poly layer right under the metal pad.  $R_n$  and  $R_p$  are also realized by poly lines around the input pad. The capacitance of  $C_n$  and  $C_p$  can be adjusted by different overlap area between poly layer and metal pad. The resistance of  $R_n$  and  $R_p$  can be adjusted by different length of poly lines.

A practical layout example in a  $0.5\ \mu\text{m}$  3-V CMOS SRAM process is shown in Fig. 8 with device dimension of  $W/L = 500/1.0\ (\mu\text{m})$  for both Mn1 and Mp1. In Fig. 8,  $C_n(C_p)$  is realized with capacitance of  $0.2\ \text{pF}$ .  $R_n(R_p)$  is realized with resistance of  $78\ \text{K}\Omega$ . Mn1 and Mp1 are surrounded by double guard rings ( $N^+$  and  $P^+$  diffusion) to prevent  $V_{DD}$ -to- $V_{SS}$  latchup issue. The total layout area of this input cell (including the pad of  $100 \times 100\ \mu\text{m}^2$  in Fig. 8 is only  $307 \times 144\ \mu\text{m}^2$ .

## IV. DESIGN MODEL OF CAPACITOR-COUPLE TECHNIQUE

A design model is developed in this section to determine adequate coupling capacitance and sustaining resistance for the capacitor-couple ESD protection circuit, which is triggered on in ESD-stress condition but kept off in normal operating condition of CMOS IC's.

### A. Design Model of Capacitor-Couple ESD Protection Circuit

An ESD-transient input waveform for model formulation is considered as a ramp voltage with peak voltage  $V_p$  of 10 V and rise time  $t_r$  of 10 ns as shown in Fig. 9. Since the gate-oxide thickness of CMOS devices in the  $0.5\text{-}\mu\text{m}$  3-V CMOS

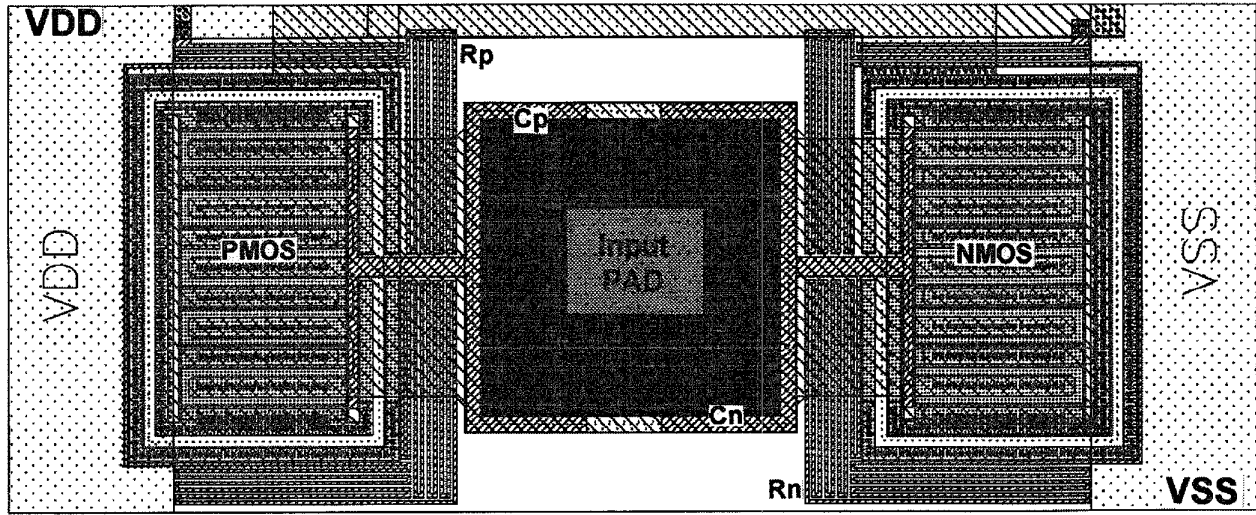


Fig. 8. A practical layout example of the capacitor-couple ESD protection circuit.

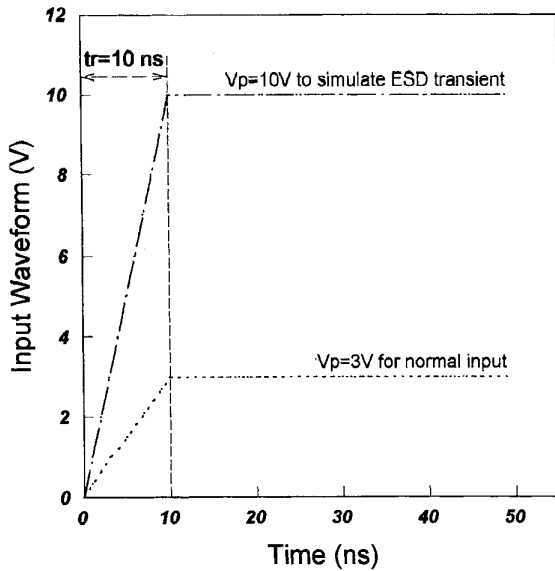


Fig. 9. Input waveform to simulate ESD-transient voltage before gate-oxide breakdown for model derivation.

SRAM process is only 90 Å, such thinner gate oxide could be ruptured if a voltage above 10 V is across it. So, the peak voltage  $V_p$  in model derivation is set to 10 V. A normal input signal is also shown in Fig. 9 with peak voltage of 3 V and rise time of 10 ns to simulate normal input signal on the input pad. The capacitor-couple effect should be designed to trigger on the ESD-protection NMOS/PMOS when the pad is under ESD stress. But, the ESD-protection NMOS/PMOS should not be triggered on by any normal input signal when the pad is under normal operation of CMOS IC's. For simplicity, the capacitor-couple effect on ESD-protection NMOS and PMOS is separately considered in model derivation. The model formulation on half of capacitor-couple ESD protection circuit with Mn1 device is described in the following.

The first step is to determine the operating region of NMOS in the capacitor-couple ESD protection circuit. To determine operating region of NMOS, the drain-source voltage  $V_{ds}$  under various gate-source voltage  $V_{gs}$  is classified. There are three operating regions of ESD-protection NMOS under PS-mode ESD stress.

- NMOS OFF*, when  $t < tr$ : While  $V_{gs}(t) < V_{tn}$ , NMOS is off;
- NMOS ON*, when  $t < tr$ : As  $V_{gs}(t) \geq V_{tn}$ , but  $V_{ds}(t) > [V_{gs}(t) - V_{tn}]$ , NMOS is in saturation region;
- NMOS ON*, when  $t \geq tr$ : NMOS remains in saturation region, because of  $V_{ds}(t) > [V_{gs}(t) - V_{tn}]$ .

The second step is to find the large-signal equivalent circuit of the capacitor-couple ESD protection circuit. The large-signal equivalent circuit of MOSFET with drain current and five parasitic capacitors is used in model derivation [21]. The resultant large-signal equivalent circuits of the capacitor-couple ESD-protection NMOS under above three different operating regions are summarized in Fig. 10. With suitable linearization on parasitic capacitors of MOSFET [21] (which is estimated as the average value over its operating region), each large-signal equivalent circuit of Fig. 10 can be treated as a linear circuit. The third step is to solve the coupled gate voltage in time domain. The solved  $V_{gs}(t)$  corresponding to different operating regions can be expressed as

$$V_{gs}(t) = R_n \cdot C_{gdt}^{OFF} \cdot \frac{V_p}{tr} \left[ 1 - \exp \left( \frac{-t}{R_n(C_{gdt}^{OFF} + C_{gst}^{OFF})} \right) \right] \quad (1)$$

as NMOS is off and  $t < tr$

$$V_{gs}(t) = R_n \cdot C_{gdt}^{SAT} \cdot \frac{V_p}{tr} - \left( R_n \cdot C_{gdt}^{SAT} \cdot \frac{V_p}{tr} - V_{tn} \right) \times \exp \left( -\frac{t - t_1}{R_n(C_{gdt}^{SAT} + C_{gst}^{SAT})} \right) \quad (2)$$

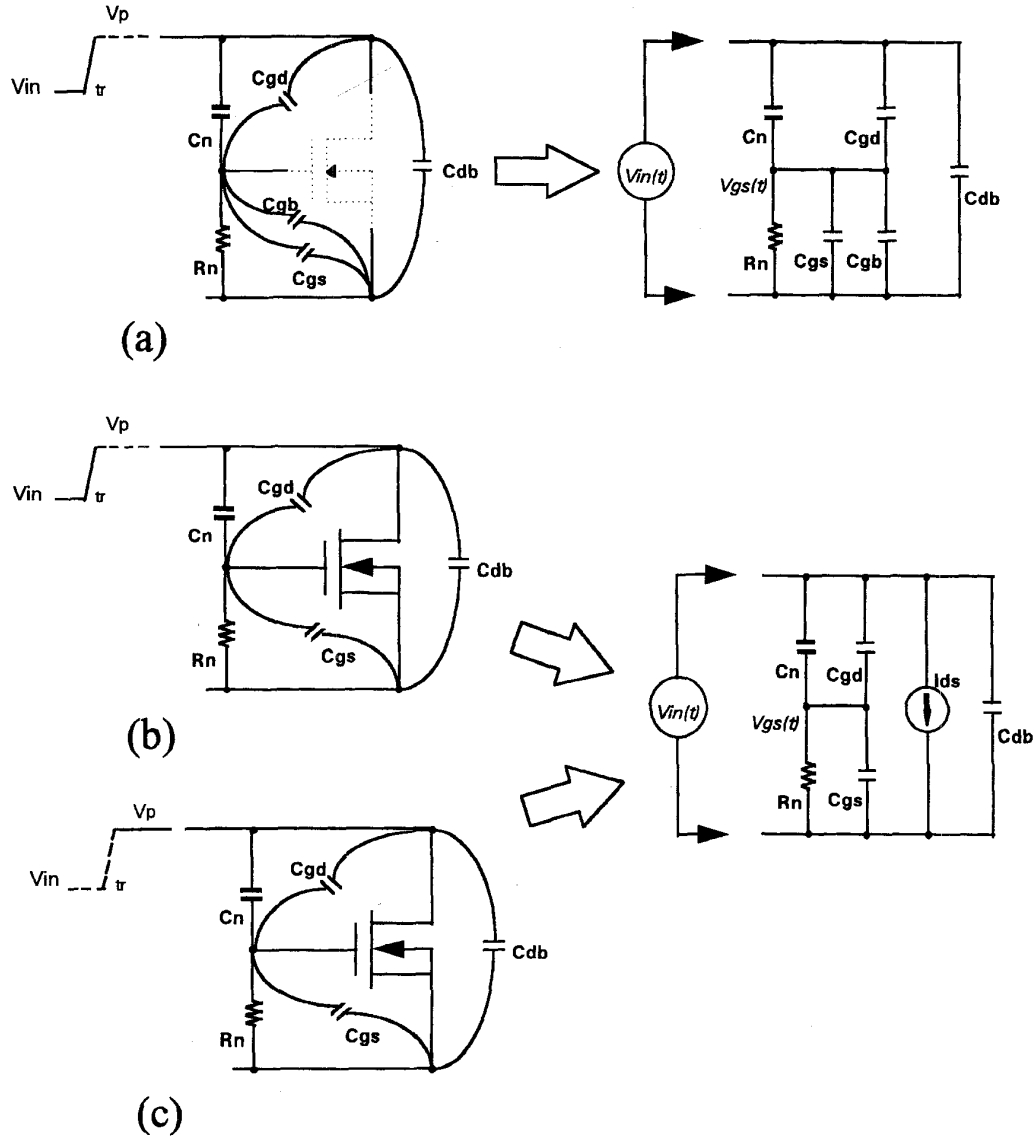


Fig. 10. The large-signal equivalent circuits for the capacitor-couple ESD-protection NMOS device under three different operating regions. (a) Protection NMOS off ( $V_{gs} < V_{th}$  and  $t < tr$ ). (b) Protection NMOS on ( $V_{gs} \geq V_{th}$  and  $t < tr$ ). (c) Protection NMOS on ( $V_{gs} \geq V_{th}$  and  $t \geq tr$ ).

as NMOS is in saturation region and  $t < tr$

$$V_{gs}(t) = V_{gsm} \cdot \exp\left(-\frac{t - tr}{R_n(C_{gdt}^{SAT} + C_{gst}^{SAT})}\right) \quad (3)$$

as NMOS is in saturation region but  $t \geq tr$  where

$R_n$  is the sustaining resistance;

$V_{tn}$  is the threshold voltage of NMOS;

$C_{gdt}^{OFF}$  is the total gate-drain capacitance of NMOS in off region, which includes  $C_n$ ;

$C_{gdt}^{SAT}$  is the total gate-drain capacitance of NMOS in saturation region, which includes  $C_n$ ;

$C_{gst}^{OFF}$  is the total gate-source capacitance of NMOS in off region;

$C_{gst}^{SAT}$  is the total gate-source capacitance of NMOS in saturation region;

$V_{gsm}$  is the maximum voltage coupled to the gate of NMOS;

$V_p$  is the simulated peak voltage of ESD;

$tr$  is the rise time of ESD voltage; and

$t_1$  is the time when the coupled gate voltage  $V_{gs}(t)$  first reaches the threshold voltage  $V_{tn}$ .

The capacitance used in (1)–(3) is summarized in Table I. The coupled gate voltage  $V_{gs}(t)$  in time domain calculated by above derived equations is shown in Fig. 11, which is triggered by a 10-V ramp voltage with rise time of 10 ns. The device dimension of ESD-protection NMOS in Fig. 11 is 500/1.0 ( $\mu\text{m}$ ). The coupling capacitance  $C_n$  is 50 fF, and the sustaining resistor  $R_n$  is 84 K $\Omega$ .  $V_{tn}$  is 0.635 V in the 0.5  $\mu\text{m}$  3 V CMOS SRAM process. As seen in Fig. 11, the coupled gate voltage first rises up due to the 10 V ramp voltage applied to the input pad. This  $V_{gs}(t)$  will reach its maximum

TABLE I  
CAPACITANCES OF CAPACITOR-COUPLE ESD-PROTECTION  
NMOS USED IN THE DESIGN MODEL

$$C_{gdt}^{OFF} = C_n + C_{ox} \cdot W_n \cdot L_D$$

$$C_{gst}^{OFF} = C_{ox} \cdot W_n \cdot (L_n + L_D)$$

$$C_{gdt}^{SAT} = C_n + C_{ox} \cdot W_n \cdot L_D$$

$$C_{gst}^{SAT} = C_{ox} \cdot W_n \cdot \left(\frac{2}{3} L_n + L_D\right)$$

where  $C_{ox}$  is the gate-oxide capacitance per unit area;  
 $C_n$  is the coupling capacitance;  
 $L_D$  is the lateral diffusion;  
 $L_n$  is the channel length of NMOS;  
 $W_n$  is the channel width of NMOS.

value  $V_{gsm}$  on the time when the input ramp voltage reaches its peak value of 10 V. Larger  $C_n$  will lead to higher  $V_{gsm}$  on the gate of ESD-protection NMOS. Then, this coupled gate voltage is gradually discharged to 0 V through the resistor  $R_n$ .

Based on above model formulation, the maximum coupled gate voltage can be obtained by calculating (2) at  $t = tr$ , which is expressed as

$$V_{gsm} = R_n \cdot C_{gdt}^{SAT} \cdot \frac{V_p}{tr} - \left( R_n \cdot C_{gdt}^{SAT} \cdot \frac{V_p}{tr} - V_{tn} \right) \cdot \left[ \frac{R_n \cdot C_{gdt}^{OFF} \cdot \frac{V_p}{tr}}{R_n \cdot C_{gdt}^{OFF} \cdot \frac{V_p}{tr} - V_{tn}} \right]^{(C_{gdt}^{OFF} + C_{gst}^{OFF}) / (C_{gdt}^{SAT} + C_{gst}^{SAT})} \cdot \exp \left( -\frac{tr}{R_n (C_{gdt}^{SAT} + C_{gst}^{SAT})} \right). \quad (4)$$

The time  $t_1$  when  $V_{gs}(t)$  first rises up to reach  $V_{tn}$ , as well as the time  $t_2$  when  $V_{gs}(t)$  falls below  $V_{tn}$  again, are two important parameters in the design model. These two parameters are also indicated in Fig. 11. They can be obtained by setting (1) and (3) equal to  $V_{tn}$ , respectively. The time  $t_1$  and  $t_2$  can be obtained as

$$t_1 = R_n \cdot (C_{gdt}^{OFF} + C_{gst}^{OFF}) \cdot \ln \left[ \frac{R_n \cdot C_{gdt}^{OFF} \cdot \frac{V_p}{tr}}{R_n \cdot C_{gdt}^{OFF} \cdot \frac{V_p}{tr} - V_{tn}} \right] \quad (5)$$

and

$$t_2 = tr + R_n \cdot (C_{gdt}^{SAT} + C_{gst}^{SAT}) \cdot \ln \left[ \frac{V_{gsm}}{V_{tn}} \right]. \quad (6)$$

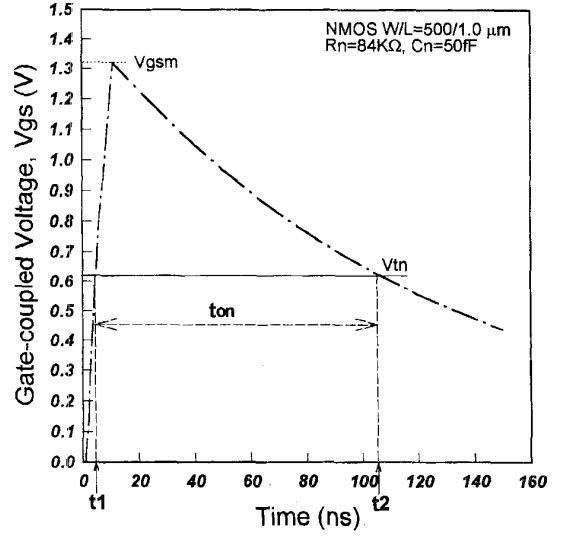


Fig. 11. The coupled voltage waveform of  $V_{gs}(t)$  under the triggering of a 10 V ramp voltage with rise time of 10 ns, which is calculated by the derived design model.

The turn-on time of ESD-protection NMOS during ESD stress is an important factor to design suitable  $C_n$  and  $R_n$  in the capacitor-couple ESD protection circuit. Usually, the NMOS turn-on time,  $t_{on}$ , is designed in the range of 100–200 ns, which just fitted the transient duration of ESD stress. The turn-on time of ESD-protection NMOS can be obtained by

$$t_{on} = t_2 - t_1. \quad (7)$$

All above equations are derived from capacitor-couple ESD-protection NMOS in PS-mode ESD-stress condition. Similar design model for the half ESD-protection circuit from input pad to VDD with PMOS device in the ND-mode ESD-stress condition can be also obtained, if adequate replacement is made in the derived equations.

#### B. Comparison Between Model Calculation and HSPICE Simulation

The ESD protection circuit should be turned on only when the circuit is under ESD stress. The dependence of  $C_n$  and  $R_n$  ( $C_p$  and  $R_p$ ) on the coupled gate voltage of ESD-protection NMOS (PMOS) can be calculated by the derived design model. The accuracy of this design model is verified by HSPICE simulation.

Fig. 12 and Fig. 13 show the dependence of NMOS turn-on time on the coupling capacitance  $C_n$  and sustaining resistance  $R_n$ , respectively, with both model-calculated and HSPICE-simulated results. The solid dots represent the HSPICE-simulated results and the dashed lines show the model-calculated results. The NMOS turn-on time is nearly a linear function of  $C_n$  in Fig. 12. Larger  $C_n$  causes longer NMOS turn-on time to bypass ESD current. In Fig. 13, the NMOS turn-on time is also nearly a linear function of  $R_n$ . Larger  $R_n$  also causes longer NMOS turn-on time to bypass ESD current. Fig. 14 shows the relation between the maximum coupled gate voltage ( $V_{gsm}$ ) and  $C_n$  under different  $R_n$ . It is

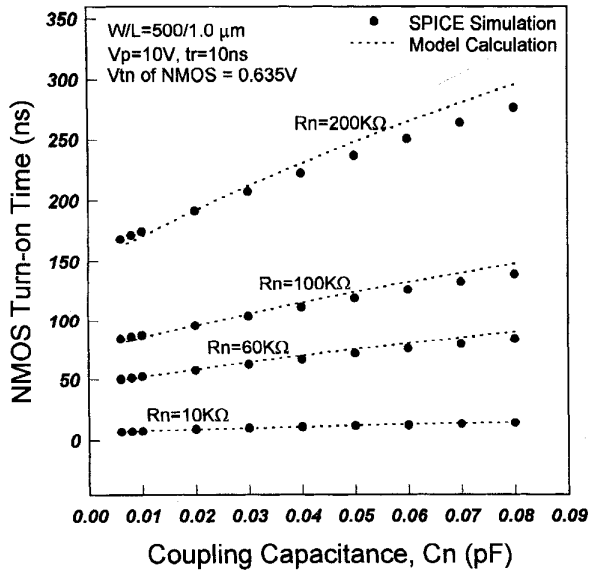


Fig. 12. Comparison between model-calculated and HSPICE-simulated results about the effect of  $C_n$  on NMOS turn-on time under different  $R_n$ .

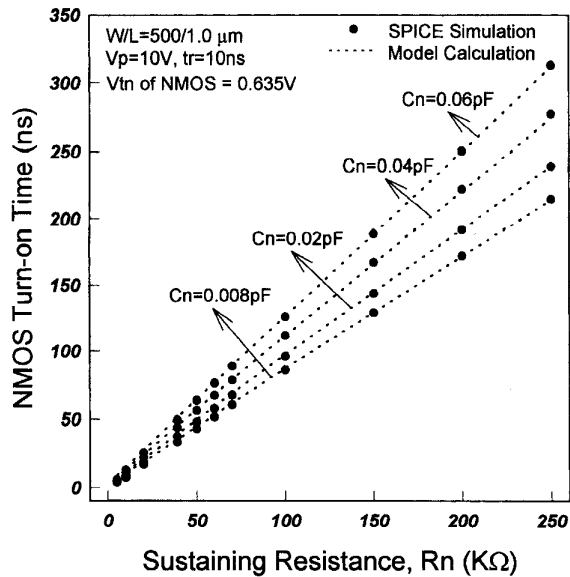


Fig. 13. Comparison between model-calculated and HSPICE-simulated results about the effect of  $R_n$  on NMOS turn-on time under different  $C_n$ .

shown that larger  $C_n$  and  $R_n$  cause higher  $V_{gsm}$  on the gate of ESD-protection NMOS.

Fig. 15 depicts the overall effects between  $C_n$  and  $R_n$  under different NMOS turn-on time from 50 to 200 ns. For longer turn-on time, either  $R_n$  or  $C_n$  has to be designed with larger value. The undesired design region, shown in Fig. 15, means that the  $C_n$  or  $R_n$  are overdesigned in the capacitor-couple ESD protection circuit. This will cause voltage degradation on the normal 3 V input signal, because the voltage coupled to the gate of ESD-protection NMOS with such  $C_n$  and  $R_n$  is higher than its threshold voltage. So,  $R_n$  and  $C_n$  in this undesired region should be avoided in this capacitor-

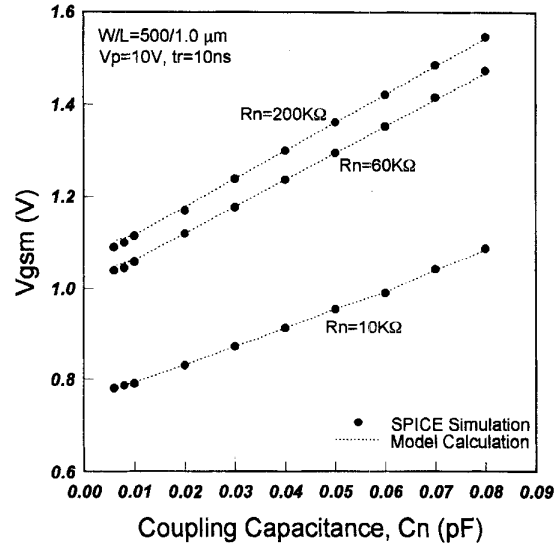


Fig. 14. Comparison between model-calculated and HSPICE-simulated results about the effect of  $C_n$  on  $V_{gsm}$  (maximum coupled gate voltage) under different  $R_n$ .

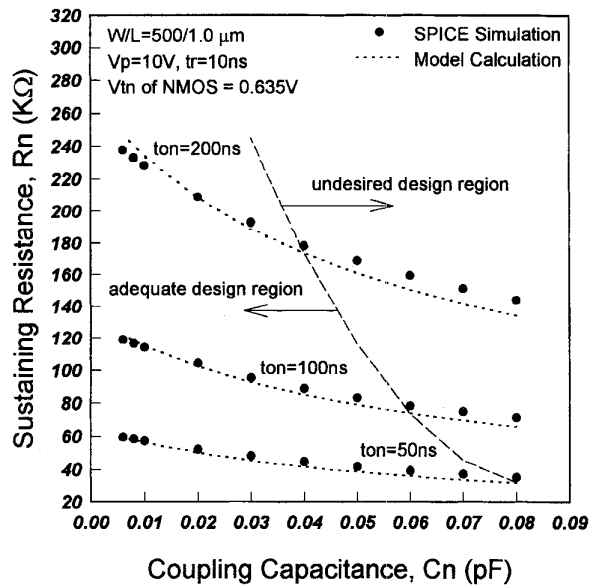


Fig. 15. Overall relation between  $C_n$  and  $R_n$  under different NMOS turn-on time with both model-calculated and HSPICE-simulated results.

couple ESD protection circuit. In the adequate design region of Fig. 15, the ESD-protection NMOS is not triggered on by the normal 3 V input signal, but it can be triggered on by the 10 V 10 ns ramp voltage under turn-on time from 50 to 200 ns. The adequate design region for  $R_n$  and  $C_n$  in Fig. 15 is located around the region of smaller value, so  $C_n$  and  $R_n$  can be practically realized by the poly layer as shown in Figs. 7 and 8 without occupying extra layout area.

Another issue on the capacitor-couple technique is the rise time of 10 V ramp voltage, which is used to simulate the ESD-transient voltage before the gate oxide of input stage is ruptured. In the design model, the rise time  $t_r$  has been

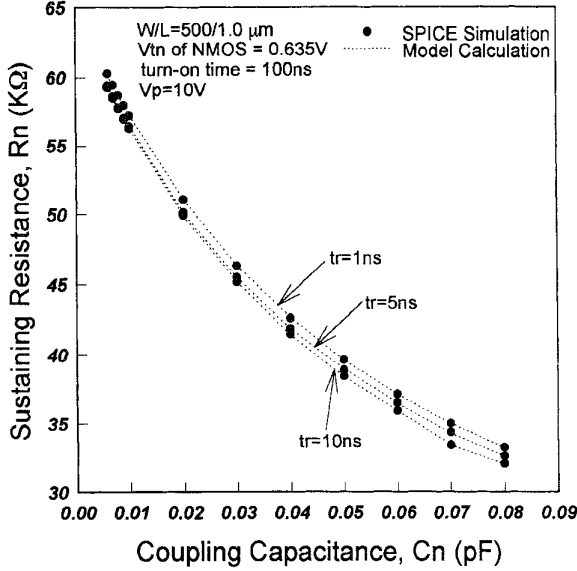


Fig. 16. The relation of  $C_n$  and  $R_n$  to keep NMOS turn-on time of 100 ns under different rise time of the 10 V ramp voltage.

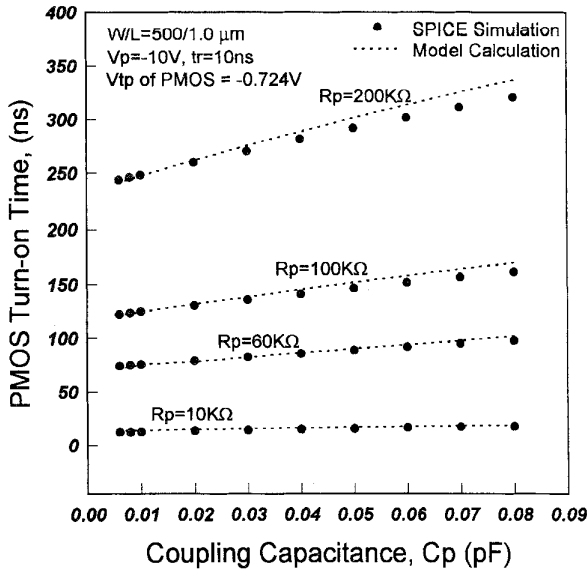


Fig. 17. Comparison between model-calculated and *HSPICE*-simulated results about the effect of  $C_p$  on PMOS turn-on time under different  $R_p$ .

considered in equations (1)–(7). The sensitivity of  $t_r$  on the design of  $R_n$  and  $C_n$  is analyzed in Fig. 16, where the NMOS turn-on time is kept as a constant of 100 ns. The peak voltage of ESD-simulated input voltage is still kept as 10 V, but its rise time is separately calculated with 1, 5, and 10 ns. In Fig. 16, it is shown that the variation between different curves due to different rise time of input ramp voltage is below 5%. Hence, the adequate design region in Fig. 15 for  $R_n$  and  $C_n$  is almost suitable for this capacitor-couple ESD protection circuit to protect both Human-Body-Model ESD stress (with rise time of 5–10 ns) and Machine-Model ESD stress (with rise time of 1–2 ns).

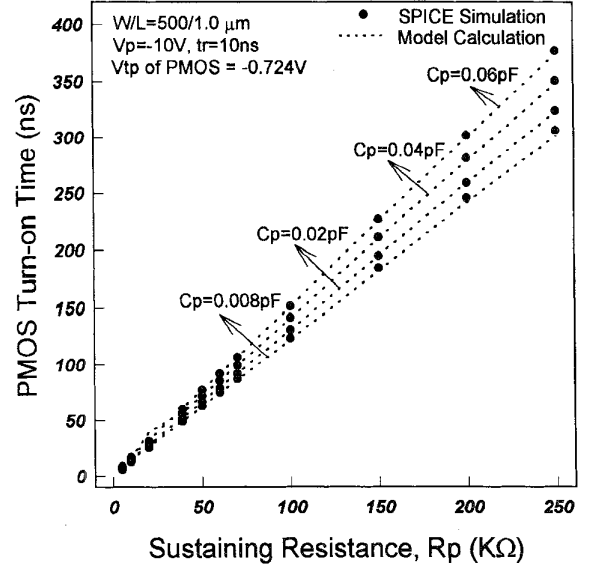


Fig. 18. Comparison between model-calculated and *HSPICE*-simulated results about the effect of  $R_p$  on PMOS turn-on time under different  $C_p$ .

The dependence of PMOS turn-on time on coupling capacitance  $C_p$  and sustaining resistance  $R_p$  is also calculated by the design model and compared with *HSPICE*-simulated results in Figs. 17 and 18, respectively. The effect of  $C_p$  and  $R_p$  on the PMOS turn-on time is similar to that of  $C_n$  and  $R_n$  on the NMOS turn-on time. The adequate design region and undesired design region about  $R_p$  and  $C_p$  for ESD-protection PMOS to accurately operate in CMOS IC's is shown in Fig. 19 with comparison to *HSPICE*-simulated results. The adequate design region for  $R_p$  and  $C_p$  in Fig. 19 is also located around the smaller-value region, so  $R_p$  and  $C_p$  for ESD-protection PMOS can be realized by the poly layer as shown in Figs. 7 and 8. This makes the capacitor-couple ESD protection circuit more suitable for high-pin-count CMOS IC's even in the pad-limited condition.

From Figs. 12 to 19, good agreement exists between *HSPICE*-simulated and model-calculated results to verify this derived design model. With wide-range verification in the design model, suitable design of capacitor-couple ESD protection circuit can be easily obtained by this design model instead of iterative trial-and-error *HSPICE* simulation.

## V. EXPERIMENTAL RESULTS

Based on the design model of capacitor-couple ESD protection circuit, one set of test circuits with different device dimensions has been designed and fabricated in a 0.5  $\mu\text{m}$  3 V CMOS SRAM process. A microphotograph of the fabricated capacitor-couple ESD protection circuit is shown in Fig. 20, which is corresponding to the layout of Fig. 8. The test chip is assembled in IC package for ESD testing and for verification of capacitor-couple efficiency.

### A. Verification of Capacitor-Couple Efficiency

To verify this capacitor-couple effect, an NMOS device with  $W/L = 20/1.0$  ( $\mu\text{m}$ ) is also on-chip designed with its gate

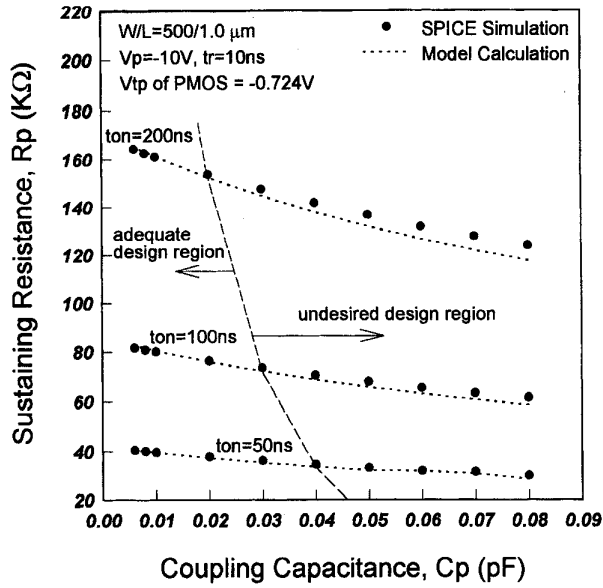


Fig. 19. Overall relation between  $C_p$  and  $R_p$  under different PMOS turn-on time with both model-calculated and *HSPICE*-simulated results.

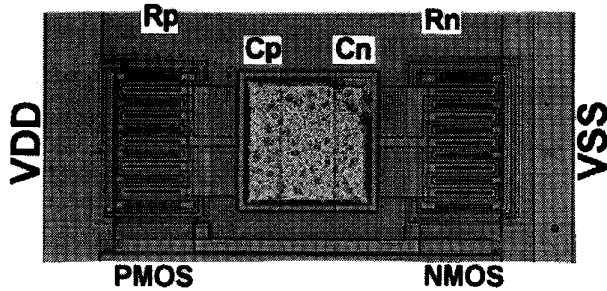


Fig. 20. A microphotograph of the fabricated capacitor-couple ESD protection circuit.

connected to the gate of ESD-protection NMOS to monitor the coupled gate voltage. The setup to measure this capacitor-couple efficiency is shown in Fig. 21 with the monitor NMOS Mn2. A positive pulse-type voltage waveform with rise time of 5 ns (generated by pulse generator Hp8116A) is used to simulate ESD-transient voltage and applied to the input pad. This is to simulate the PS-mode ESD-stress condition. An oscilloscope is used to monitor the voltage waveform in time domain to investigate the capacitor-couple effect. The gate voltage of Mn1 will arise from zero if a sharp-rising ESD-like voltage pulse is applied to the input pad. The voltage coupled to the gate of Mn1 can be monitored by Mn2 device due to their gates are connected together. If the gate of Mn1 (also of Mn2) is coupled to some voltage level through  $C_n$ , Mn2 will be turned on to conduct current through the external resistor  $R_{ext}$ . Thus, the voltage at node "x" will be pulled down from 5 V synchronously when the input voltage pulse is applied.

A typical measured result is shown in Fig. 22, where an input pulse with rising peak of 8.6 V (CH1) can cause a maximum voltage drop (at x node) of 1.77 V (CH2) from 5 V. This voltage drop on  $R_{ext}$  of 1 KΩ causes a drain current

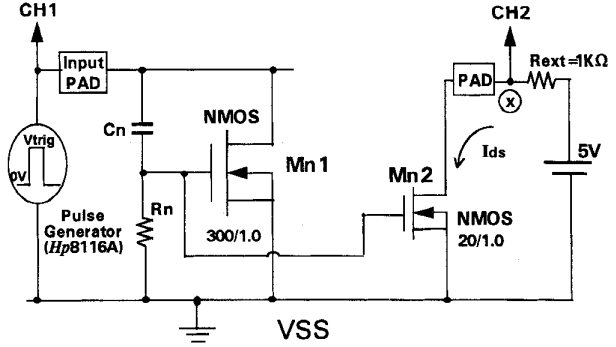


Fig. 21. Experimental setup to measure the capacitor-couple efficiency in the capacitor-couple ESD-protection NMOS.

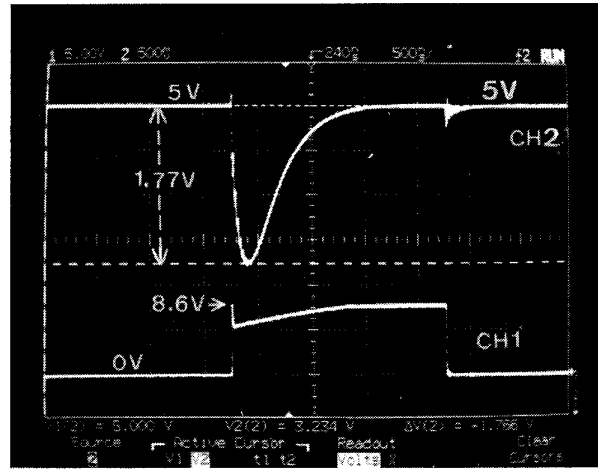


Fig. 22. Typical measured voltage waveforms in the setup of Fig. 21 (X-axis: 500 ns/div.; CH1: 5 V/div.; CH2: 0.5 V/div.).

of 1.77 mA into Mn2. By measuring the I-V characteristics of a separated NMOS device which is the same as Mn2 in the same test chip, the corresponding maximum coupled voltage on the gate of Mn1 can be found about 2.3 V. After capacitor coupling, the gate voltage of Mn1 is discharged below  $V_{tn}$  again by  $R_n$ . Then, Mn2 is turned off, and the voltage of node "x" will be restored to 5 V again as shown in CH2 of Fig. 22. In Fig. 22, the turn-on time of Mn2 (also of Mn1) is as long as 1.22  $\mu$ s as the coupled gate voltage is still higher than  $V_{tn}$ . From above measured results, the coupling effect of  $C_n$  and the voltage sustaining capability of  $R_n$  can be verified.

To verify the capacitor-couple efficiency among  $C_p$ ,  $R_p$ , and ESD-protection PMOS Mp1, a measurement setup is shown in Fig. 23 with an on-chip monitor PMOS Mp2 of  $W/L = 20/1.0$  ( $\mu$ m). In Fig. 23, the gate voltage of Mp1 drops from zero if a sharp-falling ESD-like negative voltage pulse is applied to the input pad. A pulse generator (HP8116A) is used to apply a negative voltage pulse to the input pad (CH3) with VDD pad grounded. This is to simulate the ND-mode ESD-stress condition. The negative voltage coupled to the gate of Mp1 through  $C_p$  is monitored by Mp2. If the gate of Mp1 (also of Mp2) is coupled to some negative voltage level, Mp2 will be turned on to conduct current to external

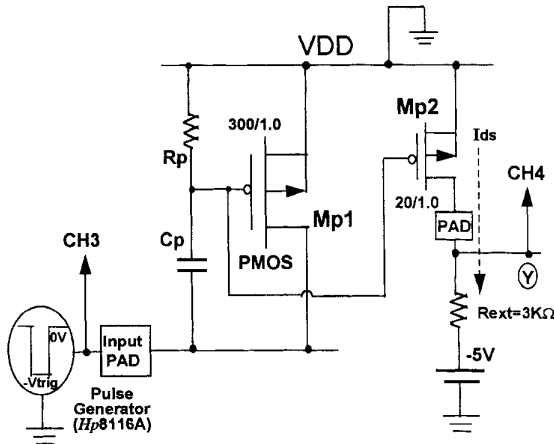


Fig. 23. Experimental setup to measure the capacitor-couple efficiency in the capacitor-couple ESD-protection PMOS.

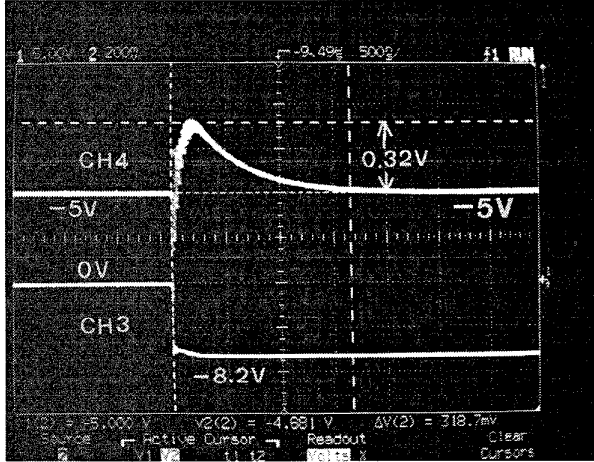


Fig. 24. Typical measured voltage waveforms in the setup of Fig. 23 (X axis: 500 ns/div.; CH3: 5 V/div.; CH4: 0.2 V/div.).

resistor  $R_{ext}$ . Thus, the voltage at node "Y" (CH4) in Fig. 23 is pulled up from  $-5$  V synchronously when the input voltage pulse is applied.

A typical measured result of capacitor-couple PMOS is shown in Fig. 24, where an input pulse with falling voltage peak of  $-8.2$  V (CH3) and falling time of 5 ns can cause a maximum voltage increase of 0.32 V at node "Y" (CH4) from its initial bias of  $-5$  V. This causes a drain current about 0.1 mA through Mp2 and  $R_{ext}$  of 3 K $\Omega$  to the  $-5$  V power supply. The corresponding maximum coupled voltage on the gate of Mp1 can be found as 1.14 V. The negative gate voltage of Mp1 will be discharged to become higher than  $V_{tp}$  again by  $R_p$  where  $V_{tp}$  is the negative threshold voltage of PMOS. After the falling trigger, Mp2 is turned off and the voltage at node "Y" is restored to  $-5$  V again. The turn-on time is about 1.66  $\mu$ s.

Fig. 25 shows the relation between the measured turn-on time of ESD-protection NMOS/PMOS and the pulse-type trigger voltage on the input pad. The NMOS (PMOS)

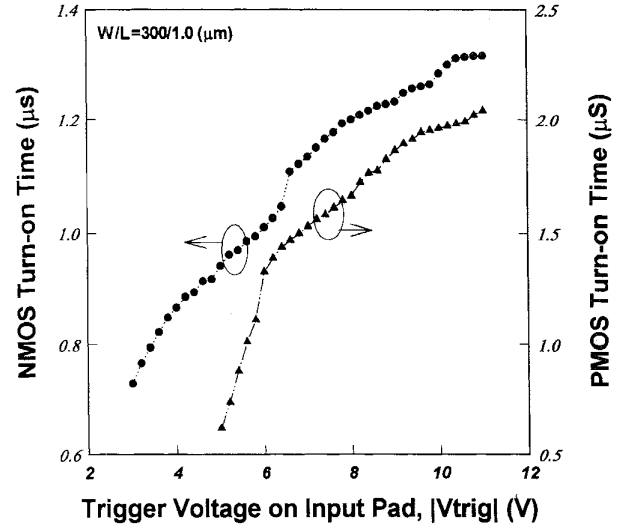


Fig. 25. Measured results of turn-on time of capacitor-couple ESD-protection NMOS and PMOS with different input voltage peaks.

turn-on time increases as the magnitude of input voltage increases. The coupling capacitance and sustaining resistance in the test circuit are 0.14 pF and 140 K $\Omega$ , respectively, for both capacitor-couple NMOS and PMOS. In Fig. 25, the measured turn-on time of PMOS is longer than that of NMOS with the same trigger voltage on input pad. For symmetrical performance of ESD protection, the coupling capacitance and sustaining resistance have to be better designed with equal turn-on time in the ESD-protection NMOS and PMOS.

The experimental results shown here is just to demonstrate the fundamental function of coupling capacitance and sustaining resistance in the capacitor-couple ESD protection circuit. For practical applications in different submicron or deep-submicron CMOS technologies,  $C_n(C_p)$  and  $R_n(R_p)$  have to be adequately adjusted to meet the required turn-on time of ESD-protection device during ESD transition.

### B. ESD Testing Results

Two well-known industrial standards of ESD testing, Human-Body-Model (HBM, MIL-STD-883C method 3015.7) and Machine-Model (MM, EIAJ-IC-121 method 20), are used to find the ESD failure threshold of the fabricated capacitor-couple ESD protection circuit in the four-mode ESD-stress conditions. The failure criterion is defined as the ESD voltage to cause input leakage current above 1  $\mu$ A under 5-V  $V_{DD}$  and 0-V  $V_{SS}$  biases. ESD testing results (the ESD-pass voltage) of the fabricated test circuits with different device dimensions are listed in Table II (for HBM ESD testing) and Table III (for MM ESD testing), which are tested by the ESD tester HANWA HED-S5000 (produced in Japan). Without large device dimension but with lower trigger voltage to protect the thinner gate oxide, the capacitor-couple ESD protection circuit can pass the commercial specification of 2 KV HBM and 200 V MM ESD voltage. It is also found that the ESD-pass voltage is almost linearly increased as the channel width is increased either in HBM or MM ESD. In Table II, the

TABLE II  
HUMAN-BODY-MODEL ESD TESTING RESULTS

W/L ( $\mu\text{m}$ ) Mode	500/1.2	500/1.0	500/0.8	500/0.6	400/1.0	300/1.2	300/1.0	300/0.8	300/0.6
ND	-3.5K	-3.25K	-3.25K	-3.5K	-2.75K	-2K	-2K	-2K	-2.25K
PD	>	>	>	>	>	>	>	>	>
NS	>	>	>	>	>	>	>	>	>
PS	4K	4.75K	5.75K	7.25K	4K	2K	2.25K	4.75K	5.5K

( > Beyond 8KV)

TABLE III  
MACHINE-MODEL ESD TESTING RESULTS

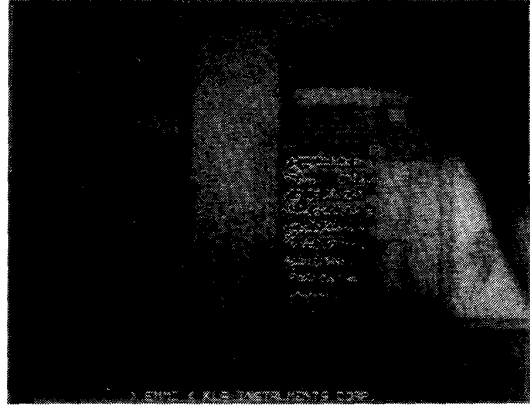
W/L ( $\mu\text{m}$ ) Mode	500/1.2	500/1.0	500/0.8	500/0.6	400/1.0	300/1.2	300/1.0	300/0.8	300/0.6
ND	-240	-240	-220	-200	-200	-200	-200	-200	-180
PD	320	360	300	280	340	320	260	220	240
NS	-550	-550	-550	-550	-550	-550	-550	-550	-550
PS	450	450	450	450	450	450	450	450	300

ND: Negative to VDD  
PD: Positive to VDD

NS: Negative to VSS  
PS: Positive to VSS



(a)



(b)

Fig. 26. EMMI photograph of ESD-damaged hot spots among the multiple fingers of (a) capacitor-couple ESD-protection PMOS after ND-mode ESD stress and (b) capacitor-couple ESD-protection NMOS after PS-mode ESD stress.

shorter channel length of ESD-protection NMOS obviously performs a higher ESD-pass voltage under the PS-mode HBM ESD testing, because the shorter channel length leads to a higher current gain in the parasitic lateral bipolar action of ESD-protection NMOS device. This gives us a reference to choose suitable device dimension for practical applications.

### C. Failure Analysis

The uniform current distribution in ESD protection devices was verified by using photon-emission microscopy (EMMI). Fig. 26 shows EMMI analysis of the capacitor-couple ESD

protection circuit after ESD stress. Fig. 26(a) presents the damaged hot spots on the capacitor-couple ESD-protection PMOS, which had been damaged by HBM ESD in the ND-mode condition. The damage on capacitor-couple ESD-protection NMOS due to PS-mode HBM ESD stress is shown in Fig. 26(b). The device dimensions ( $W/L$ ) of ESD-protection NMOS and PMOS in Fig. 26 are both 500/1.0 ( $\mu\text{m}$ ). In Fig. 26, all the five fingers of ESD-protection PMOS (NMOS) are uniformly turned on and damaged by the ND-mode (PS-mode) ESD voltage. This verifies the uniform turn-on characteristics of the capacitor-couple ESD protection circuit.

## VI. CONCLUSION

A capacitor-couple ESD protection circuit has been successfully designed, fabricated, and verified in a 0.5- $\mu\text{m}$  3-V CMOS technology. Through capacitor-couple design, the PS-mode (ND-mode) ESD-transient voltage is coupled to the gate of ESD-protection NMOS (PMOS) to lower its snapback-trigger voltage, as well as to earlier trigger on the parasitic lateral bipolar action in the MOS device to bypass ESD current. The PD-mode (NS-mode) ESD voltage is clamped by the parasitic diode  $D_{p1}$  ( $D_{n1}$ ) in the ESD-protection PMOS (NMOS). Thus, the thinner gate oxide in deep-submicron low-voltage CMOS technology can be effectively protected. With the poly layer inserting under the metal pad to realize the coupling capacitance and the poly lines extending around the pad to realize the sustaining resistance, a small layout area of the capacitor-couple ESD protection circuit has been demonstrated without increasing extra layout area to the IC chip. A timing-original design model has been also derived to calculate the capacitor-couple efficiency for the capacitor-couple ESD protection circuit without trial-and-error HSPICE simulation. Experimental results have verified that this capacitor-couple technique can offer more effective ESD protection for the thinner gate oxide. Not only to ensure uniform ESD current distribution among the multiple fingers of ESD-protection devices but also to earlier trigger on the ESD-protection devices to bypass ESD current, the ESD-pass voltage is found to be higher than 2 kV and 200 V in HBM and MM ESD testing, respectively. The ESD-pass voltage is linearly increased as the device dimension of ESD-protection NMOS/PMOS is increased. The proposed capacitor-couple ESD protection circuit is very suitable for deep-submicron low-voltage CMOS ASIC in the high-pin-count or the pad-limited application to save silicon cost. This capacitor-couple technique can be also applied to the CMOS output buffer to improve ESD robustness of the output pad.

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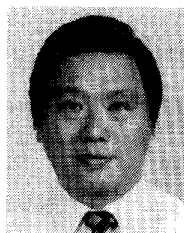
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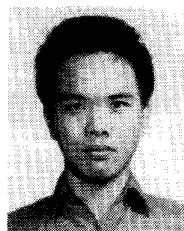


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