

ESD PROTECTION TO OVERCOME INTERNAL GATE-OXIDE DAMAGE ON DIGITAL-ANALOG INTERFACE OF MIXED-MODE CMOS IC's

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Abstract: This paper reports an ESD internal gate-oxide damage occurred on the digital-analog interface of a mixed-mode CMOS IC. A new ESD protection method is proposed to rescue this internal gate-oxide damage by adding ESD-protection devices on the long metal line between digital-analog interfaces. Experimental verification has confirmed that the IC product can be rescued to pass 2-KV ESD stress from the digital/analog VDD to digital/analog VSS pads without causing any internal damage again.

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INTRODUCTION

As the improvement of submicron and deep-submicron CMOS technologies, the internal circuits of CMOS IC's become more sensitive to ESD stress. Even with input/output ESD protection circuits, there are still some unexpected ESD damages at the internal circuits beyond the input/output ESD protection circuits [1]-[4]. The internal damages, which had been reported, most occurred due to the junction breakdown on the drain of thin-oxide devices or parasitic field-oxide devices in CMOS IC's.

In this paper, a new internal damage due to the breakdown on the gate oxide of internal circuits in the digital-analog interface is reported. This unexpected ESD damage has been overcome by a new ESD protection design at the interface between the digital and analog parts.

THE UNEXPECTED ESD DAMAGE ON INTERNAL CIRCUITS

Since an ESD stress may have positive or negative voltage polarity on an input (or output) pin with reference to grounded VDD or VSS pins, there are four different ESD-stress modes on an input (or output) pin [5]. The four modes of ESD stresses on an input (or output) pin are illustrated in Fig.1. Moreover, ESD current could enter into any pin and go out from another pin of an IC. To practically verify the whole-chip ESD reliability, two additional testing conditions have to be considered into the ESD testing [6]. These two additional ESD testing conditions are shown in Figs.2 (a) and 2(b). In Fig.2(a), the ESD voltage is stressed on an input (or output) pin as other input and output pins are grounded but both the VDD and VSS pins are floating. In

Fig.2(b), the ESD voltage is directly stressed on the VDD pin with grounded VSS pin but all input and output pins are floating. In these two ESD testing conditions, the CMOS IC's are more vulnerable to internal ESD damage even if there are input and output ESD protection circuits on the input and output pads.

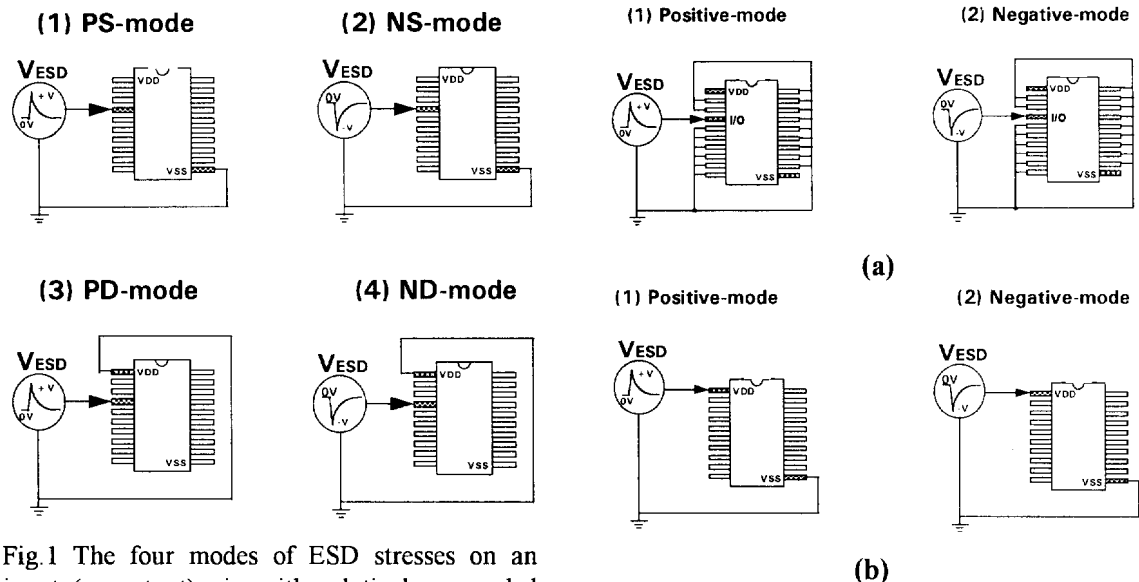


Fig.1 The four modes of ESD stresses on an input (or output) pin with relatively grounded VDD or VSS pins.

Fig.2 Two additional ESD-testing conditions to verify the whole-chip ESD reliability.

The schematic circuit diagram of a mixed-mode IC in our case is shown in Fig.3, where the input of inverter in the analog part is from the output of digital part with a long metal line. The VDD and VSS pads of the analog part are separated from those of the digital part. There is a gate-grounded thin-oxide NMOS device made as VDD-to-VSS ESD protection device between the digital VDD and digital VSS power lines. Between the analog VDD and VSS power lines, there is also a gate-grounded thin-oxide NMOS device made as VDD-to-VSS ESD protection device. Under the human-body-model (HBM) PS-mode ESD stress, a positive ESD voltage applied to the pad with VSS pad grounded, the input and output pads of the mixed-mode IC can sustain above 4 KV without causing any damage on the input, output, and the internal circuits. But, if a 2-KV positive ESD stress is applied to both the digital VDD and analog VDD pads with both digital VSS and analog VSS grounded, several output functions are failed. By tracing the data-process circuits and operation-control circuits, the failure is focused between the digital-analog interfaces.

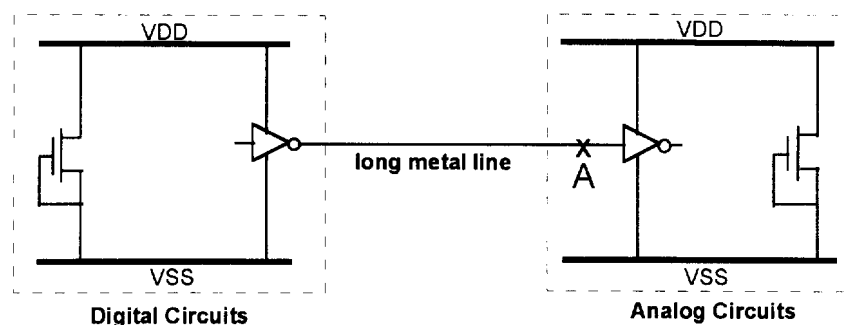


Fig.3 A schematic diagram of the digital-analog interface in a mixed-mode IC.

To point out the failure location, the photo-emission microscope (EMMI) is used to find the hot spot on the digital-analog interfaces. The measured EMMI picture is shown in Fig.4, where the failure spots are located around the input gates of an analog inverter. To verify the failure is due to gate-oxide damage, the long metal line from the digital part is cut at the "A" point in Fig.3 by a laser cutter, and internal probing technique is used to measure the leakage current at the point "A" with 5-V VDD and 0-V VSS biases. The measured result is shown in Fig.5, where there is about 2-mA leakage current on the gates of PMOS and NMOS devices of the analog inverter. This confirms that the positive ESD stress from the VDD to VSS causes internal gate-oxide damage between the digital-analog interfaces.

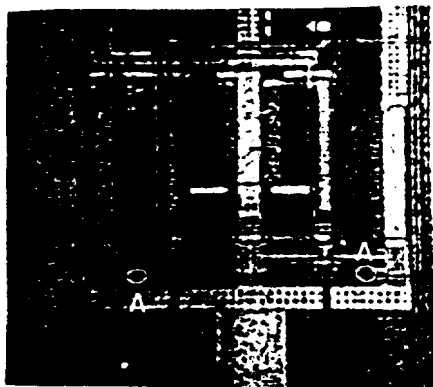


Fig.4 The EMMI picture to show the location of internal ESD damage.

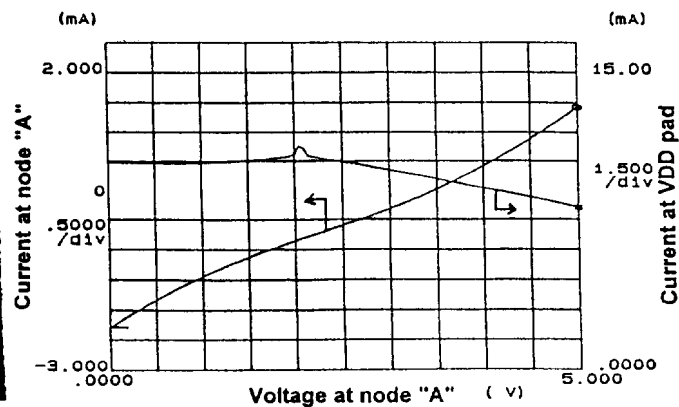


Fig.5 The measured leakage current on the input gates of analog inverter.

SOLUTIONS TO RESCUE THIS MIXED-MODE IC

To overcome this internal gate-oxide damage between the digital-analog interfaces, a new ESD protection circuit is added near to the input gates of the analog inverter as shown in Fig.6. The added ESD protection circuit is made by a PMOS and an NMOS devices with their gates shorted to their sources, respectively. The same ESD protection circuit is also added to the digital inverter with input signal from the analog part to avoid similar ESD damage. The device dimensions of ESD-protection PMOS and NMOS devices are designed under different lengths of the metal line, which is connected between the digital and analog circuits. An empirical design rule for device dimension of this internal ESD-protection device under different metal-line lengths is summarized in Table I. Following this design rule to add the ESD-protection devices on the long metal line between the digital-analog interfaces, the mixed-mode IC can be rescued to pass 2-KV ESD stress from the digital/analog VDD to digital/analog VSS pads without causing any internal damage.

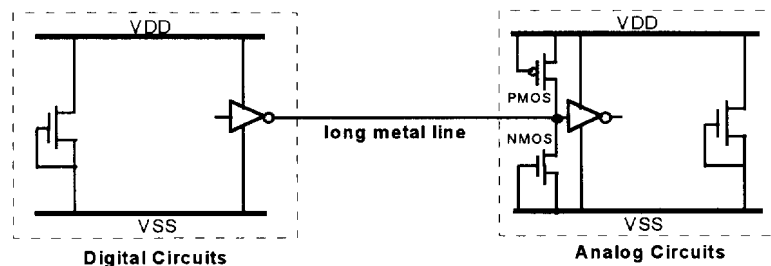


Fig.6 The proposed ESD protection method to rescue the ESD damage between the digital-analog interface.

Table I

The empirical design rule for the device dimensions of internal ESD-protection devices under different lengths of the metal line between digital and analog circuits.

Length of the long metal line	Device dimension of ESD protection devices (μm)
$500\mu\text{m} \leq L < 1000\mu\text{m}$	NMOS W/L=20/0.7 ; PMOS W/L=20/0.7
$1000\mu\text{m} \leq L < 1500\mu\text{m}$	NMOS W/L=40/0.7 ; PMOS W/L=40/0.7
$1500\mu\text{m} \leq L < 2000\mu\text{m}$	NMOS W/L=60/0.7 ; PMOS W/L=60/0.7

Another solution to avoid such internal ESD damages is to consider the whole-chip ESD protection design. Especially in the mixed-mode IC with multiple VDD and VSS power pins. A schematic diagram to show a whole-chip ESD protection design for a mixed-mode IC is illustrated in Fig. 7. By using this alternative solution, the unexpected internal ESD damage can also be overcome for the mixed-mode IC.

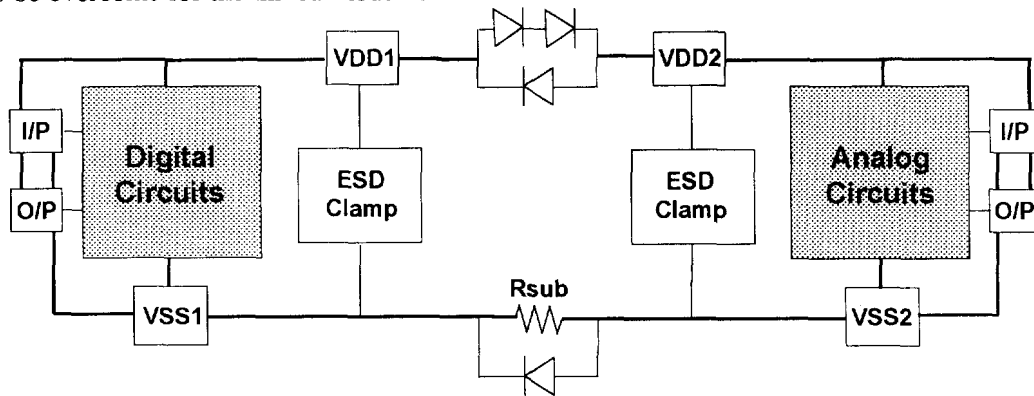


Fig.7 A schematic diagram to show the whole-chip ESD protection design for a mixed-mode IC.

CONCLUSION

An unusual ESD damage on an internal gate oxide between the digital-analog interface of a mixed-mode IC has been reported. Two solutions have been proposed to rescue such unexpected internal ESD damage. One is an empirical rule by using additional ESD protection devices between the analog and digital interfaces. The other is to adopt a whole-chip ESD protection concept on the beginning of chip design. These two solutions can effectively provide the mixed-mode IC with stronger ESD robustness under any ESD-testing conditions.

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