A Gate-Coupled PTLSCR/NTLSCR ESD Protection Circuit for Deep-Submicron Low-Voltage CMOS IC's

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***Abstract*— A novel electrostatic discharge (ESD) protection circuit, which combines complementary low-voltage-triggered lateral SCR (LVTSCR) devices and the gate-coupling technique, is proposed to effectively protect the thinner gate oxide of deep submicron CMOS IC's without adding an extra ESD-implant mask. Gate-coupling technique is used to couple the ESD-transient voltage to the gates of the PMOS-triggered/NMOS-triggered lateral silicon controlled rectifier (SCR) (PTLSCR/NTLSCR) devices to turn on the lateral SCR devices during an ESD stress. The trigger voltage of gate-coupled lateral SCR devices can be significantly reduced by the coupling capacitor. Thus, the thinner gate oxide of the input buffers in deep-submicron low-voltage CMOS IC's can be fully protected against ESD damage. Experimental results have verified that this proposed ESD protection circuit with a trigger voltage about 7 V can provide 4.8 (3.3) times human-body-model (HBM) [machine-model (MM)] ESD failure levels while occupying 47% of layout area, as compared with a conventional CMOS ESD protection circuit.**

***Index Terms*—Electrostatic discharge, ESD protection circuit, gate-couple technique, low-voltage-triggered lateral SCR, PMOS-triggered lateral SCR, NMOS-triggered lateral SCR, human-body model, machine model, charged-device model, ESD-implant process.**

I. Introduction

ELECTROSTATIC discharge (ESD) protection has become an important but difficult design for CMOS IC's in deep submicron technologies, due to the thinner gate oxide, shorter channel length, shallower drain/source junction, lightly-doped drain (LDD) structure, polycide, and silicided diffusion, which seriously degrade the ESD robustness of CMOS IC's [1], [2]. In practical IC products, an ESD protection circuit made around each input (or output) pad is required to provide higher protection levels with smaller layout area to save chip size. Area-efficient ESD protection circuits are especially demanded in high-pin-count, pad-limited CMOS VLSI/ULSI circuits.

Moreover, the thickness of the gate oxide is scaled down in deep-submicron CMOS technologies for low-voltage applications [2]. This thinner gate oxide is more sensitive to ESD stress. For ESD protection of an input pad, the gate-grounded NMOS device is often used as the secondary protection element to clamp the voltage across the gate oxide of input devices. But, the voltage margin between the gate-oxide breakdown and the drain snapback breakdown is also reduced in deep submicron CMOS technology. Therefore, the thinner gate oxide may be ruptured by ESD voltage before drain snapback breakdown of the secondary-protection NMOS device. ESD reliability of the thinner gate oxide has therefore become a design challenge in deep-submicron low-voltage CMOS IC's.

In this paper, a novel ESD protection circuit, which combines both the low-voltage-triggered lateral SCR (LVTSCR) devices and the gate-coupling technique, is proposed to protect the thinner gate oxide of deep submicron CMOS IC's more effectively [3]. Section II provides an overview of recent methods for ESD protection, which include the ESD-implant process, the gate-coupling technique, the LVTSCR device, and the protection against internal damage. In Section III, the proposed gate-coupled PTLSCR/NTLSCR ESD protection circuit is discussed. Experimental results are presented in Section IV and finally we draw some conclusions.

II. Recent Advances in ESD Protection

A. ESD-Implant Process

One of the most important features in submicron CMOS technologies which degrades ESD robustness of CMOS IC's is the LDD structure [1], [2], [4]. The LDD structure had been widely used in submicron CMOS devices to overcome the hot-carrier reliability problems [5], [6]. To improve the ESD robustness of CMOS output buffers, some submicron CMOS technologies offer an additional "ESD implant" mask into the process flow to make a stronger device structure for output transistors or input ESD protection circuits [7]–[10]. A schematic diagram is shown in Fig. 1 to clearly explain the structural difference between the LDD and ESD-implant devices. The ESD-implant process results in a heavy-doping drain and source with deeper junction depths to eliminate the LDD structure of CMOS transistors. Because the lateral diffusion of heavy-doping drain/source region may cause punchthrough or current leakage between drain and source, the minimum channel length of ESD-implant transistors has to be increased. This may cause an increase in the dimensions of the ESD-implant device to provide the same current driving

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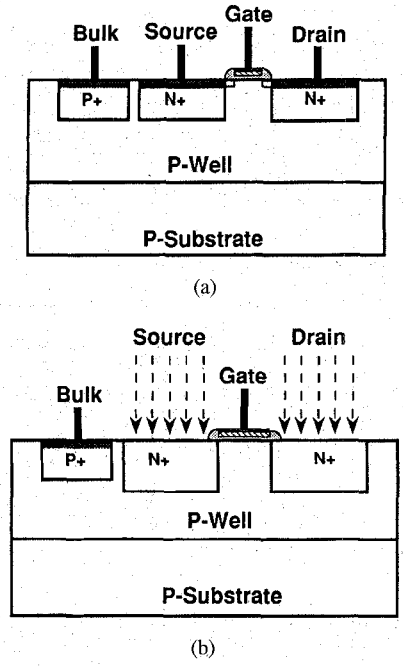


Fig. 1. Schematic cross-sectional view to show the device structure in (a) the LDD process and (b) the ESD-implant process.

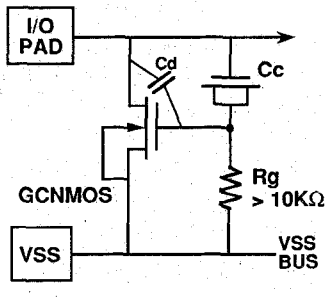


Fig. 2. Schematic circuit diagram to show the gate-coupling technique of ESD protection by a bootstrap thin-oxide NMOS [2].

capability as that of an LDD device with shorter channel length. Using an ESD-implant process, the ESD reliability of CMOS IC's can be significantly improved. However, the cost of IC fabrication is also increased due to the additional mask and process steps.

B. Gate-Coupling Technique

Another method to improve ESD reliability of submicron CMOS technologies is to adopt the "gate-coupling" technique to ensure the uniform ESD current flow among the multiple fingers of a large-dimension NMOS device [11]–[14]. One of the more effective designs with this gate-coupling technique is shown in Fig. 2 [2]. In Fig. 2, a thin-oxide NMOS acts as a coupling capacitor, and the gate of the GCNMOS is tied to VSS through a 10-kΩ N-well resistor [2], [14]. The on-time (for its gate voltage above the NMOS threshold voltage) of the GCNMOS during an ESD event was chosen about 15 $\sim$ 20 ns [2], roughly corresponding to the risetime of a human-body-model (HBM) ESD pulse.

To effectively protect the thinner gate oxide in deep submicron CMOS technologies, another gate-coupling design was

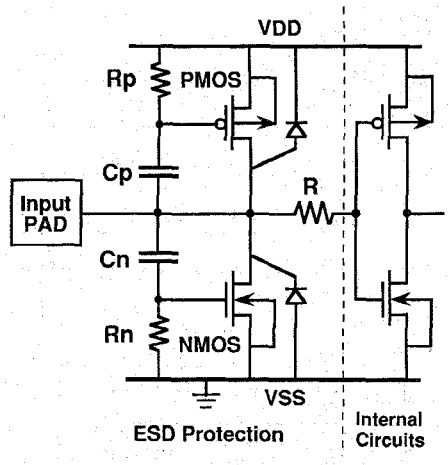


Fig. 3. A gate-coupled CMOS ESD protection circuit used to protect the thinner gate oxide of the input buffer in a 0.5-μm 3-V CMOS process [15].

reported to reduce the trigger voltage of ESD-protection devices [15]. This gate-coupled ESD protection circuit is shown in Fig. 3. The trigger voltage of ESD-protection NMOS/PMOS can be reduced below the gate-oxide breakdown voltage of the input buffer in a 0.5-μm 3-V CMOS process [15].

ESD failure levels of these gate-coupled CMOS devices are essentially limited to their physical capability of power dissipation. To provide high ESD robustness in advanced CMOS processes, such CMOS ESD-protection devices should be designed with much larger device dimensions. But, this will occupy more layout area.

C. LVTSCR Device

Due to the inherent capability of high-power delivery, the lateral SCR device has been used as a primary protection element to bypass ESD stress. Experimental results have shown that the lateral SCR device can sustain high ESD stress within the smallest layout area as compared to other traditional ESD protection elements [16]. A variation of lateral SCR is to use LVTSCR devices to protect submicron CMOS IC's [17]–[19]. A schematic cross-sectional view of the LVTSCR device is drawn in Fig. 4, where a short-channel thin-oxide NMOS is inserted into the lateral SCR structure to lower its trigger voltage [17]. The dc trigger voltage of a pure lateral SCR device in CMOS technology is equivalent to the breakdown voltage of the p-n junction between N-well and P-substrate, which is about 30 $\sim$ 50 V in submicron CMOS technology. But, the trigger voltage of LVTSCR can be lowered to the drain snapback-breakdown voltage of short-channel thin-oxide NMOS device [17]. With sufficiently lower trigger voltage, the LVTSCR can provide effective ESD protection without the assistance of secondary-protection elements and therefore reduce layout area.

To perform full ESD-protection function from the pad to both VSS and VDD, a complementary-LVTSCR structure was proposed to protect the input pad [18]. This complementary-LVTSCR ESD protection circuit is redrawn in Fig. 5, where a short-channel thin-oxide PMOS (NMOS) is inserted into the lateral SCR structure to form the LVTSCR1 (LVTSCR2) device. This complementary-LVTSCR structure can be merged

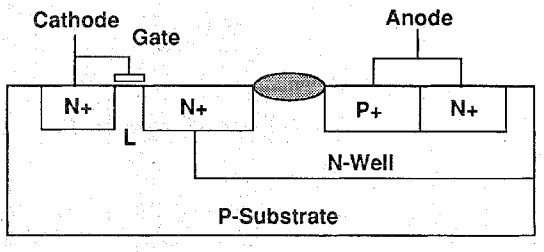


Fig. 4. Schematic cross-sectional view of the LVTSCR device [17].

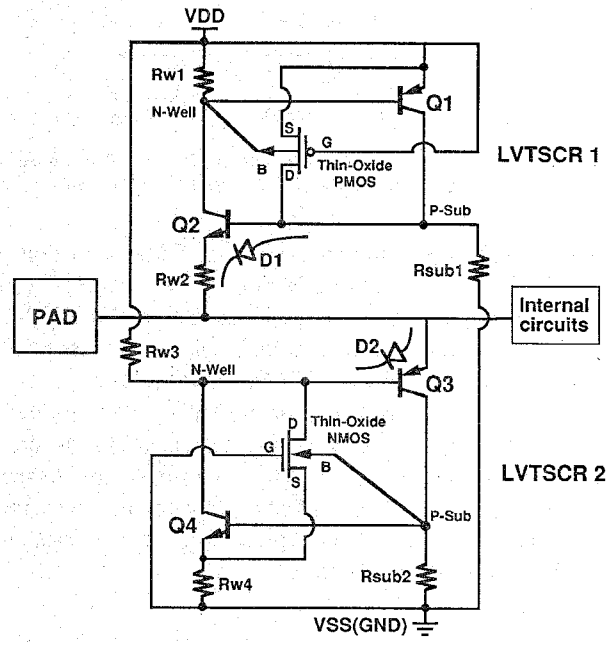


Fig. 5. The complementary-LVTSCR ESD protection circuit [18].

into the layout of the CMOS output buffer to effectively protect the output PMOS and NMOS transistors of submicron CMOS IC's [19].

Although the trigger voltage of the LVTSCR device is lowered to the drain snapback breakdown voltage of short-channel thin-oxide CMOS devices, this voltage may still be close to the breakdown voltage of the gate oxides in some deep-submicron low-voltage CMOS technologies. So, for application in such advanced CMOS IC's, the trigger voltage of the LVTSCR may have to be further reduced to provide enough voltage margin for protecting this thinner gate oxide.

D. Issue of Internal Damage

Besides the protection devices used in ESD protection circuits, there is still an important issue of unexpected ESD damage on the internal circuits of CMOS IC's beyond the input or output circuits. Since an ESD stress may have positive or negative voltage on an input (or output) pin with reference to grounded VDD or VSS pins, there are four different ESD-stress conditions on a pin as shown in Fig. 6.

1) PS mode: ESD stress at a pin with positive voltage polarity to the VSS pin when the VDD pin and other input/output pins are floating.

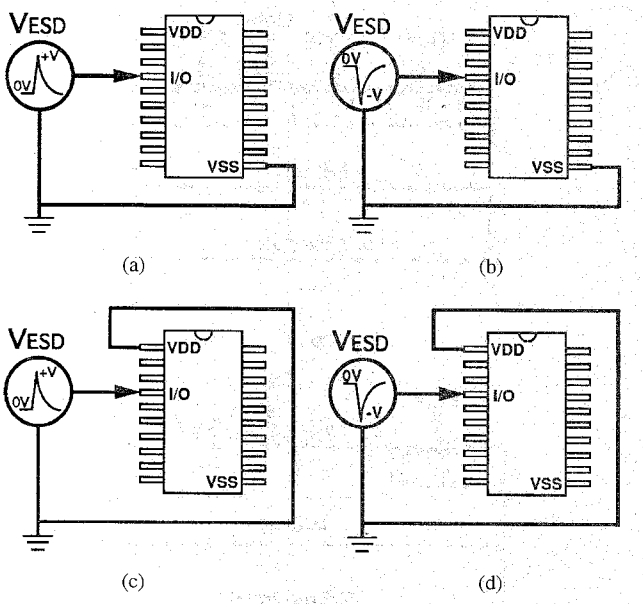


Fig. 6. The four modes of ESD stresses on a pin with reference to grounded VDD or VSS pins. (a) PS-mode, (b) NS-mode, (c) PD-mode, and (d) ND-mode.

2) NS mode: ESD stress at a pin with negative voltage polarity to the VSS pin when the VDD pin and other input/output pins are floating.
3) PD mode: ESD stress at a pin with positive voltage polarity to the VDD pin when the VSS pin and other input/output pins are floating.
4) ND mode: ESD stress at a pin with negative voltage polarity to the VDD pin when the VSS pin and other input/output pins are floating.

These ESD voltages could cause damages on both the input/output devices and the internal circuits of CMOS IC's.

In traditional ESD design, ESD protection is emphasized from the pad to VSS (or ground). There is no additional ESD protection element arranged between the pad and VDD. In this case, unexpected ESD damage has been found to occur in internal circuits apart from the ESD protection circuits [20]–[27]. Fig. 7 shows a schematic diagram to explain the unexpected discharging paths from an input pad to internal circuits in CMOS IC's under the ND-mode ESD-stress condition. The ND-mode ESD-stress voltage between the input pad and VDD is first diverted to the floating VSS power line through the input ESD protection circuit between the input pad and VSS. The diverted negative ESD voltage on the VSS line will cause voltage stress on the internal circuits between VSS and VDD power lines. If this voltage stress cannot be effectively and quickly bypassed through a VDD-to-VSS ESD protection circuit, the ND-mode ESD current may flow into the internal circuits and cause unexpected ESD damages. Because most devices and layout spacings in the internal circuits are often drawn following the minimum design rules to save chip size, such internal circuits are very weak to ESD stress. Due to the parasitic resistance (Rdd and Rss) and capacitance (C) along the VDD and VSS power lines, as well as the voltage drop on the VDD-to-VSS ESD protection element, such ND-mode ESD stresses can cause ESD damages in the internal

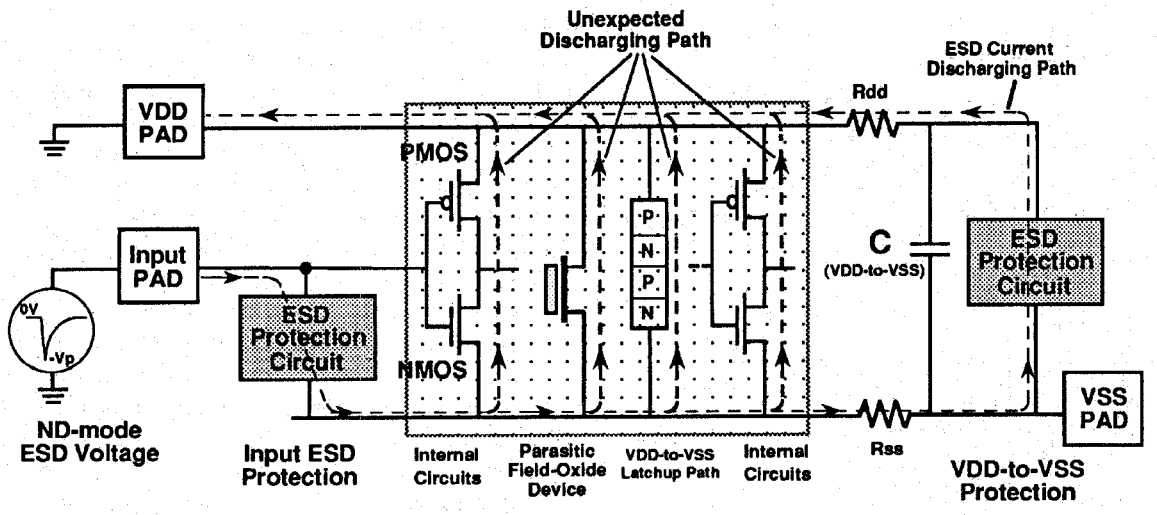


Fig. 7. Schematic circuit diagram to explain the unexpected ESD current discharging paths along internal circuits under the ND-mode ESD-stress condition.

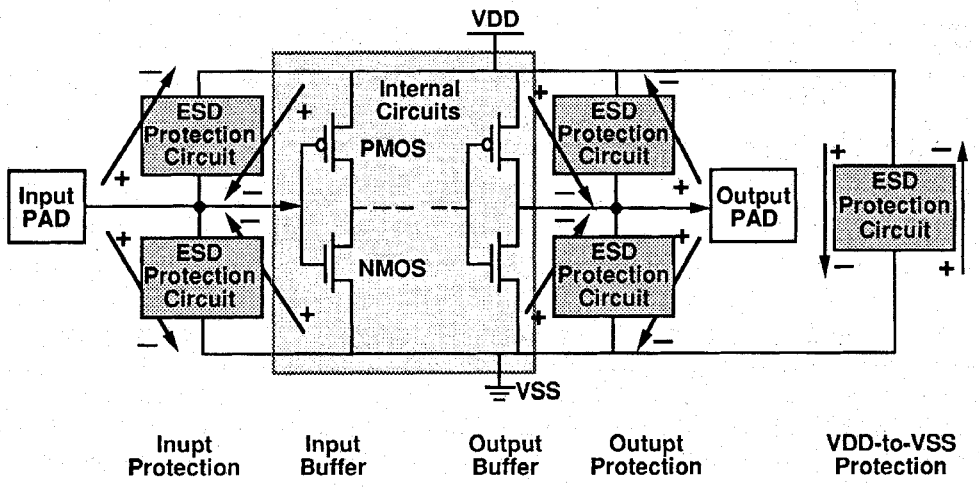


Fig. 8. Schematic circuit diagram to show the concept of whole-chip ESD protection.

circuits. Thus, an effective ESD protection circuit for input or output pads of advanced submicron CMOS IC's should provide discharging paths from the pad to both the VSS and VDD lines. This is especially necessary for a CMOS VLSI/ULSI with a larger die size and much longer VDD and VSS power lines [25]. A schematic circuit diagram to explain the concept of whole-chip ESD protection is shown in Fig. 8. Providing whole-chip ESD protection design including consideration of VDD and VSS power lines will prevent ESD damage in the internal circuits of a CMOS IC.

Recently, another method to reduce the danger of ESD damage in internal circuits is to provide a more efficient VDD-to-VSS ESD protection circuit [28]–[33]. In [28]–[30], a control circuit based on RC time constant is designed to turn on a short-channel thin-oxide NMOS device, connected between the VDD and VSS power lines. To effectively bypass ESD current through the turned-on NMOS without causing damage on itself, such a short-channel thin-oxide NMOS is designed with a device dimension (W/L) as large as 8000/0.8 (μm) [28]. Such a design can avoid ESD damage on the internal circuits, but the layout area has to be much increased to realize this effective VDD-to-VSS ESD protection design.

III. Gate-Coupled PTLSCR/NTLSCR ESD Protection Circuit

To effectively protect the thinner gate oxide of deep-submicron low-voltage CMOS IC's while avoiding ESD damage in internal circuits, a new ESD protection circuit is presented. This ESD protection circuit combines both the advantages of complementary-LVTSCR devices which provide highest ESD protection capability within smallest layout area [18] and the much lower trigger voltage by using a gate-coupling technique [15].

A. Circuit Configuration and Device Structures

The proposed ESD protection circuit is shown in Fig. 9 with the corresponding cross-sectional view in Fig. 10. A practical layout example is shown in Fig. 11. In Fig. 9, there is one PMOS-triggered lateral SCR (PTLSCR) device between the pad and VDD and one NMOS-triggered lateral SCR (NTLSCR) device between the pad and VSS. The PTLSCR

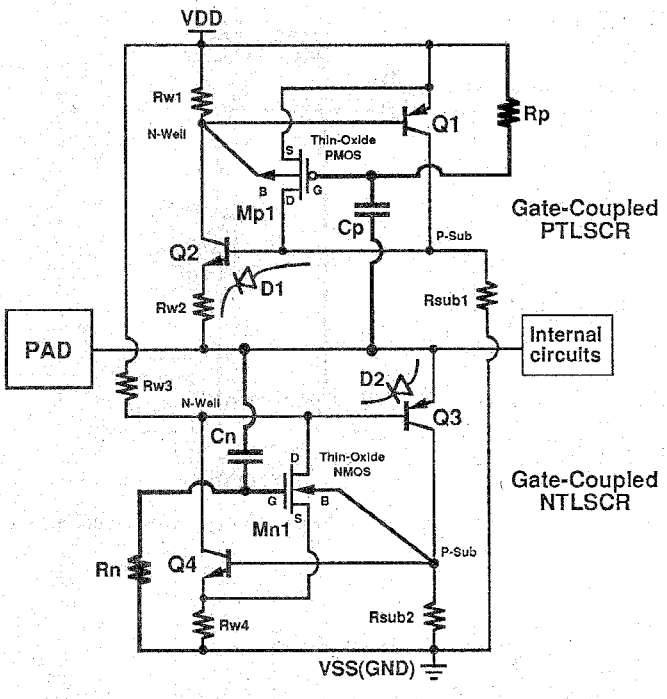


Fig. 9. The proposed gate-coupled PTLSCR/NTLSCR ESD protection circuit.

is made by inserting a short-channel thin-oxide PMOS (Mp1) into a lateral SCR structure to lower its trigger voltage. In the PTLSCR, the drain of Mp1 (P^+ diffusion) is made across the junction of an N-well and the P-substrate as shown in Fig. 10. The trigger voltage of the PTLSCR is equivalent to the drain snapback-breakdown voltage of the Mp1, if the gate of Mp1 is connected to VDD [18]. The NTLSCR is made by inserting a short-channel thin-oxide NMOS (Mn1) into a lateral SCR structure to lower its trigger voltage. In NTLSCR, the drain and source of Mn1 (N^+ diffusion) are made across the junction of N-well and P-substrate as shown in Fig. 10. The trigger voltage of NTLSCR is equivalent to the drain snapback-breakdown voltage of the Mn1, if the gate of Mn1 is connected to VSS [18]. The use of the N-well structure instead of just an N^+ diffusion, as the cathodes of PTLSCR and NTLSCR, is to enhance the emitter efficiency of lateral n-p-n bipolar transistors in the lateral SCR devices. This N-well cathode can provide more effective conducting path to bypass ESD current.

But, in deep-submicron low-voltage CMOS technology with the much thinner gate oxide, the drain snapback-breakdown voltage could be close to the gate-oxide breakdown voltage. Thus, the gate-coupling technique [15] is used to much lower the ESD-trigger voltage of the PTLSCR and NTLSCR to effectively protect the thinner gate oxide of the input buffer. The gate-coupling technique is realized by the capacitors Cp and Cn for the PTLSCR and NTLSCR, respectively. In Fig. 10, Cp and Cn are realized by the poly layer right under the metal pad without increasing total layout area of the pad. By modifying the overlap area between the poly layer and the metal pad, the capacitance of Cp and Cn can be adjusted. Capacitors Cp and Cn are designed to couple suitable ESD-transient voltage to the gates of Mp1 and Mn1, respectively. A larger voltage coupled to the gates of Mp1 and Mn1 will lead to a lower trigger voltage of the PTLSCR and NTLSCR. The coupled voltage on the gates of Mp1 and Mn1 is sustained longer in time by the resistors Rp and Rn to effectively turn on the PTLSCR and NTLSCR, respectively. Rp and Rn can be realized by the poly lines as shown in Fig. 11 without occupying extra layout area at the pad.

There are two parasitic diodes D1 and D2 in Figs. 9 and 10. The diode D1 exists at the junction of the P-substrate (connected to VSS) and the N-well (this n-well is also as the cathode of the PTLSCR). The diode D2 exists at the junction of another N-well (connected to VDD) and a P^+ diffusion (this P^+ diffusion also functions as the anode of the NTLSCR). These two diodes also contribute to ESD protection and input voltage clamping. The parasitic resistance in the N-well and P-substrate are also shown in Figs. 9 and 10.

The layout example shown in Fig. 11 demonstrates a compact layout style for this ESD protection circuit. The poly layer is used to realize Cp, Cn, Rp, and Rn. Due to the excellent ESD-protection capability of an SCR device, the silicon area used for this ESD protection circuit can be reduced considerably to perform the required ESD-protection specification.

B. Modified Design for Advanced CMOS Processes

In gate-coupling technique, a resistor is needed to sustain the gate voltage longer in time to turn on the device to bypass ESD current. To hold the gate voltage long enough during ESD transition, the resistors Rp or Rn have the order about several tens to several hundreds KΩ [14], [15], which can be realized by the well-resistor [14]. In Fig. 11, the resistors Rp and Rn are realized by the poly lines, which is especially suitable for the CMOS process with a poly layer of high sheet resistance, such as an SRAM process. But, in some standard digital CMOS processes, the poly layer has a very low sheet resistance to improve circuit speed. For example, the sheet resistance of poly layer in a 0.8-μm single-poly double-metal digital CMOS process is only about $3 \sim 4\ \Omega$. In other advanced CMOS processes, polycide has been adopted to reduce the sheet resistance of the poly layer. With such low poly sheet resistance, it becomes impractical to realize Rp and Rn in the order of KΩ by using the poly lines.

A modified gate-coupled PTLSCR/NTLSCR ESD protection circuit is shown in Fig. 12 for advanced CMOS processes [3]. The corresponding cross-sectional view and layout example of this modified ESD protection circuit are shown in Figs. 13 and 14, respectively. The main difference between this modified ESD protection circuit and the original one in Fig. 9 is the realization of the sustaining resistors Rp and Rn. In Fig. 12, the ESD-transient voltage coupled to the gate of Mp1 (Mn1) is sustained longer in time by the long-channel thin-oxide Mp2 (Mn2) device. The gate of Mp2 (Mn2) is connected to VSS (VDD) through a resistor Rp2 (Rn2). This resistor Rp2 (Rn2) can be made by a poly line without high resistance. Rp2 and Rn2 are used to protected the gates of Mp2 and Mn2, respectively. These resistors (Rp2 and Rn2) cause a time delay for the delivery of ESD stress on the VDD

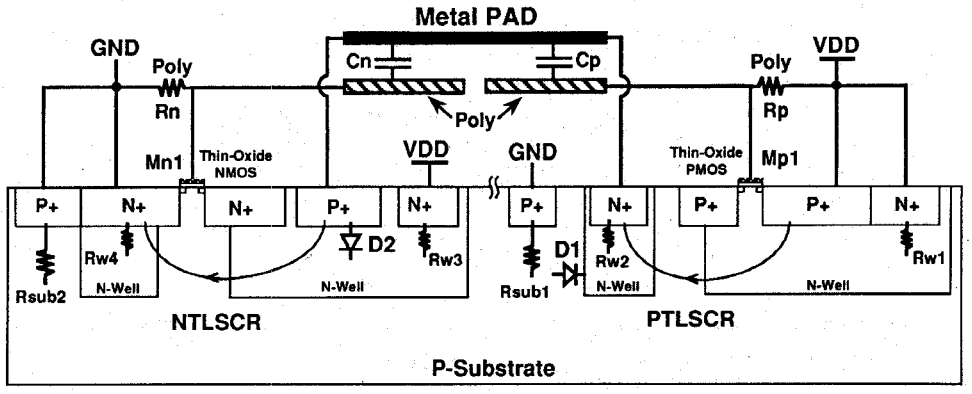


Fig. 10. Schematic cross-sectional view of the gate-coupled PTLSCR and NTLSCR devices.

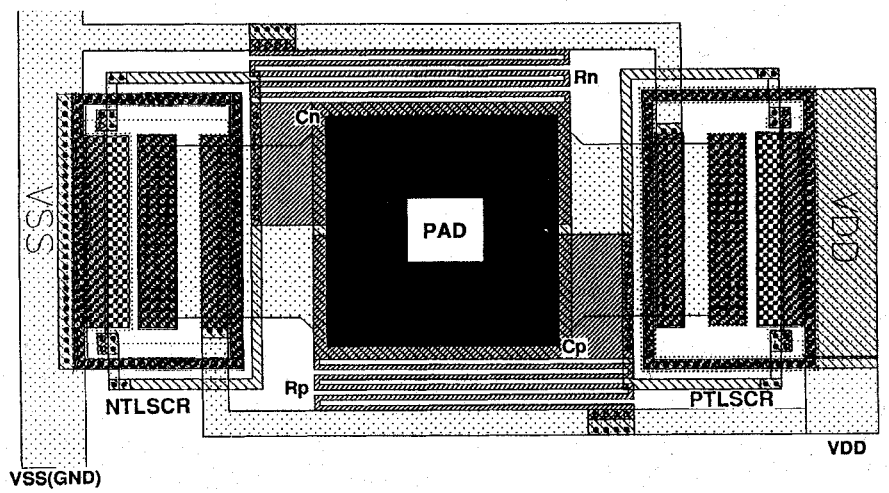


Fig. 11. A practical layout example of the gate-coupled PTLSCR/NTLSCR ESD protection circuit.

or VSS lines to the gates of Mp2 and Mn2, even with a low poly sheet resistance.

C. Operating Principles

The operation of this modified gate-coupled PTLSCR/NTLSCR ESD protection circuit is discussed below.

1) Normal Operating Conditions: Under normal CMOS operating conditions with VDD and VSS power supplies, Mp2 with its gate connected to VSS through a resistor Rp2 is turned on to bias the gate of Mp1 at VDD, so the Mp1 is off. This keeps the PTLSCR in its off state. Transistor Mn2, its gate connected to VDD through a resistor Rn2, is turned on to bias the gate of Mn1 at VSS, so the Mn1 is off. This keeps the NTLSCR also in its off state. Thus, the PTLSCR and the NTLSCR in the ESD protection circuit are guaranteed to be off under the normal CMOS operating conditions.

Moreover, the high-voltage level of input signals on the pad is clamped by the parasitic diode D2. When an input signal has a voltage overshoot greater than VDD, the diode D2 will be forward biased to clamp the overshooting voltage at around VDD + 0.6 V. The low-voltage level of input signals on the pad is also clamped by the parasitic diode D1. When an input signal has a voltage undershoot below VSS, the diode D1 will be forward biased to clamp the undershooting voltage at around VSS − 0.6 V. Thus, the input signal is clamped between VDD + 0.6 V and VSS − 0.6 V. Thus, the PTLSCR and the NTLSCR are guaranteed not to be triggered on by the overshooting/undershooting input signals under the normal operating conditions. Diodes D1 and D2 are parasitically present in the PTLSCR and NTLSCR structures, respectively, as shown in Fig. 13. The current path in the forward-biased diodes is opposite to the conducting path of the PTLSCR and NTLSCR, so the layout can be drawn to keep the PTLSCR and NTLSCR off under the normal CMOS operating conditions.

2) ESD-Stress Conditions: Since an ESD voltage on a pin may have positive or negative polarities to VDD or VSS, there are four modes of ESD stresses at each pin of a CMOS IC as shown in Fig. 6. In the PS-mode ESD-stress condition (with grounded VSS but floating VDD), there is some positive ESD-transient voltage coupled to the gate of Mn1 through the capacitor Cn. This coupled positive voltage on the gate of Mn1 is designed to be above the threshold voltage of Mn1 to turn it on. After the Mn1 is turned on, the NTLSCR will be triggered on to bypass the ESD current. When the NTLSCR is triggered on, its holding voltage is only around 1 ~ 2 V. The positive ESD-stress voltage on the pad is clamped to around 1 ~ 2 V, so the gate oxide of the input buffer can be fully protected. By

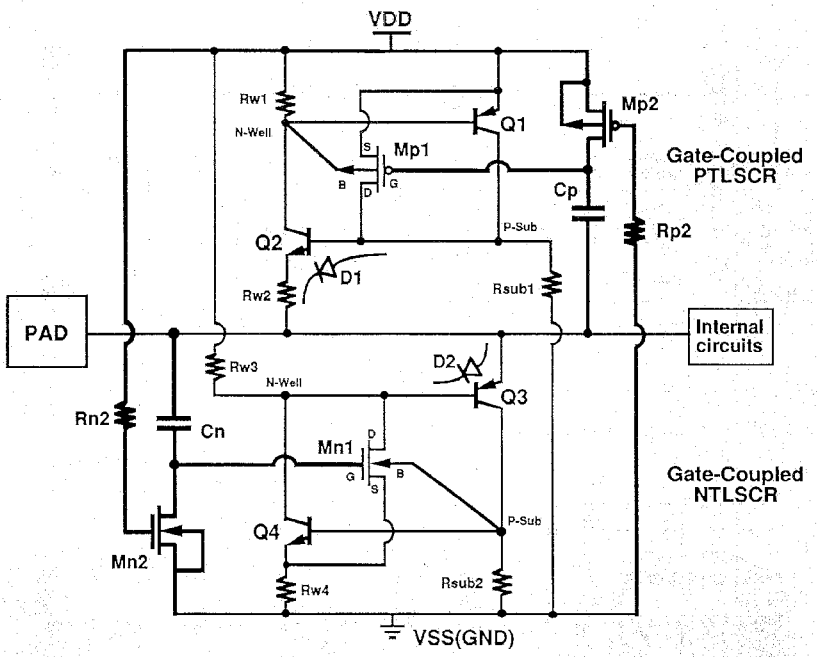


Fig. 12. The modified gate-coupled PTLSCR/NTLSCR ESD protection circuit for the advanced CMOS process.

suitably designing the capacitor Cn, the ESD-transient voltage coupled to the gate of Mn1 can be controlled to adjust the ESD-trigger voltage of the NTLSCR for different applications.

In the NS-mode (PD-mode) ESD stress, the parasitic diode D1 (D2) is forward biased and turned on to bypass ESD current from the pad to VSS (VDD). The negative (positive) ESD-stress voltage on the pad is clamped to around $-0.6 \sim -0.8$ V ($0.6 \sim 0.8$ V), so the gate oxide of the input buffer can be fully protected. A diode with proper layout in the forward-biased condition can perform high ESD robustness.

In the ND-mode ESD stress (with grounded VDD but floating VSS), there is some negative ESD-transient voltage coupled to the gate of Mp1 through the capacitor Cp. This coupled negative voltage on the gate of Mp1 is designed to turn the Mp1 on. After the Mp1 is turned on, the PTLSCR will be triggered on to bypass the ESD current. When the PTLSCR is triggered on, its holding voltage is only around $-1 \sim -2$ V. The negative ESD voltage on the pad is clamped to around $-1 \sim -2$ V, so the gate oxide of the input buffer can be fully protected. By suitably designing the capacitor Cp, the ESD-transient voltage coupled to the gate of Mp1 can be controlled to adjust the ESD-trigger voltage of the PTLSCR for different applications.

Thus, the four modes (PS, NS, PD, and ND) of ESD stresses are protected by the gate-coupled NTLSCR, D1, D2 and the gate-coupled PTLSCR devices. The ESD over-stress voltage on the pad can be clamped by this proposed ESD protection circuit to very low voltage levels (only $\pm 0.6 \sim \pm 2$ V), so the thinner gate oxide in deep-submicron low-voltage CMOS technologies can be fully protected.

D. Design Consideration for Gate-Coupling Effect

In the PS-mode ESD stress, the VDD line is floating with an initial voltage close to the grounded VSS due to the P-substrate/N-well junction present everywhere on the chip. Initially, the Mn2 is off with a very high resistance to hold the coupled ESD-transient voltage on the gate of Mn1 to turn on the NTLSCR. Then, the positive ESD voltage is discharged by the NTLSCR. Before the positive ESD voltage is completely discharged, it may be diverted to the floating VDD power line through the diode D2 and the resistor Rw3 (or the PMOS device in CMOS output buffer, which is connected between the pad and VDD). This diverted ESD voltage on the VDD power line may bias the Mn2 and turn it on. Resistor Rn2 added between the gate of Mn2 and VDD will cause a time delay to turn on the Mn2. Once on, the Mn2 acts as a resistor to discharge the coupled voltage on the gate of Mn1. A longer channel is used in the Mn2 to increase its turn-on resistance. The time for the NTLSCR device to fully turn on is dependent on the drain current of Mn1, which is dependent on the gate voltage of Mn1. A larger drain current in the Mn1 leads to a quicker turn-on of the lateral SCR structure in the NTLSCR device [34]. By controlling the Cn to adjust the voltage on the gate of Mn1 and increasing the time delay to turn on the Mn2, the NTLSCR can be triggered faster to bypass the ESD current. Cn is designed to couple the voltage from the pad to the gate of Mn1 above the threshold voltage of Mn1 under the ESD-stress condition, but to couple the input voltage to the gate of Mn1 below the threshold voltage under the normal operating conditions. A timing-based design model to calculate the suitable couple efficiency of Cn in the gate-coupled CMOS ESD protection circuit [15] has been derived and verified in [35]. For practical applications, a suitable design of the capacitor Cn can be easily achieved through the circuit simulation (such as HSPICE) with consideration on the parasitic capacitance between the VDD and VSS lines. The VDD-to-VSS parasitic capacitance increases the time delay to turn on the Mn2, which also enhances the turn-on speed of the gate-coupled NTLSCR.

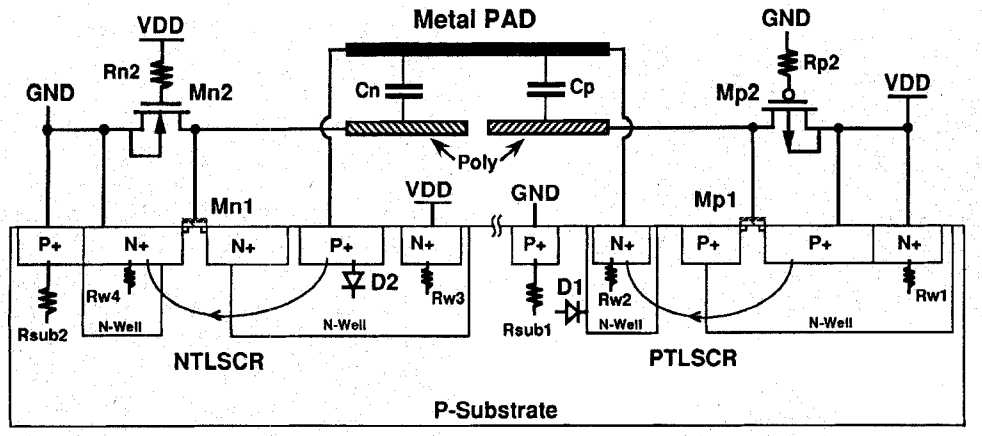


Fig. 13. Cross-sectional view of the modified gate-coupled PTLSCR and NTLSCR devices.

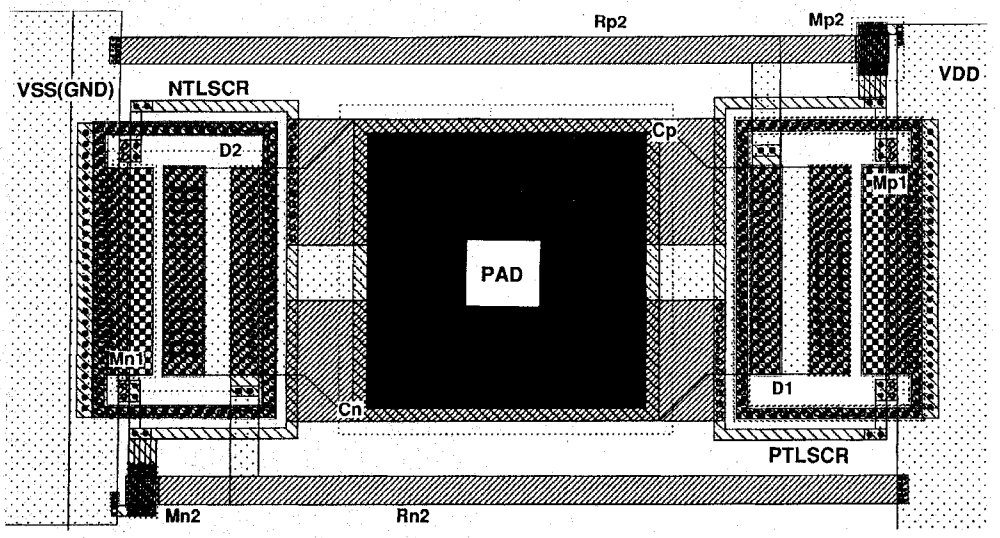


Fig. 14. A layout example of the modified gate-coupled PTLSCR/NTLSCR ESD protection circuit.

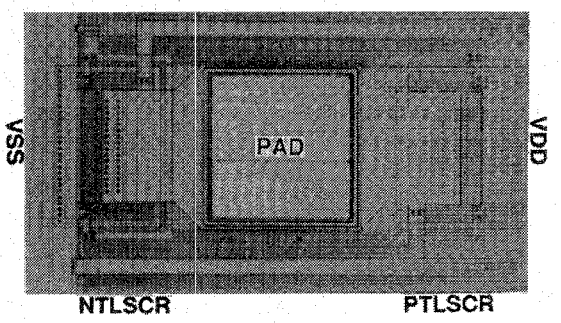
A similar design consideration is also applied to the Cp, Mp1, Mp2, and Rp2 in the gate-coupled PTLSCR device to bypass the ND-mode ESD stress.

IV. Experimental Results

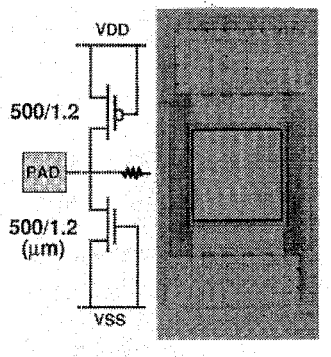
A test chip has been fabricated by using a 0.6-μm CMOS technology. A microphotograph of a pad with the modified ESD protection circuit is shown in Fig. 15(a), which is corresponding to the layout of Fig. 14. The device dimensions (W/L) of Mp1 and Mn1 are 75/1.0 (μm). The coupling capacitor Cp (Cn) in the layout is about 0.4 pF, and the device dimensions of Mp2 and Mn2 are 10/10 (μm). In Fig. 15(b), a conventional CMOS ESD protection circuit formed by a PMOS and an NMOS with W/L = 500/1.2 (μm) is also tested as a reference in the same test chip. The spacing from the drain contact to the poly-gate edge is drawn as 5 μm in the conventional CMOS ESD protection circuit.

A. Device Characteristics

The measured dc I–V characteristics of the gate-coupled PTLSCR and the gate-source-shorted PMOS in the conventional CMOS ESD protection circuit are shown in Fig. 16. In Fig. 16(a), the I–V curves of the PTLSCR are measured by applying different negative voltages to the gate of Mp1 with the VDD grounded, and the pad is stressed with a varying negative voltage. When the gate voltage of Mp1 is 0 V, the trigger voltage (current) of the PTLSCR is -16.82 V (-12.35 mA). But, as the negative gate voltage of Mp1 is increased, the trigger voltage of the PTLSCR is reduced as shown in Fig. 16(a). The effect of the coupled voltage on the gate of Mp1 on the trigger voltage of PTLSCR is shown in Fig. 17. The voltage coupled to the gate of Mp1 in order to trigger on the PTLSCR can be adjusted by the capacitor Cp. With a lower trigger voltage, the PTLSCR can be triggered faster into its latching state to bypass the ND-mode ESD stress. The holding voltage (current) of the PTLSCR is -1.45 V (-10.2 mA). The typical turn-on resistance of the PTLSCR is about $1 \sim 2\ \Omega$. Fig. 16(b) shows the snapback characteristics of a PMOS in the conventional CMOS ESD protection circuit with its gate connected to its source. The trigger voltage (current) of the PMOS with W/L of 500/1.2 (μm) is -15.58 V (-18.45 mA), and its snapback holding voltage (current) is -14.44 V (-12.05 mA). The snapback holding voltage is close to the



(a)

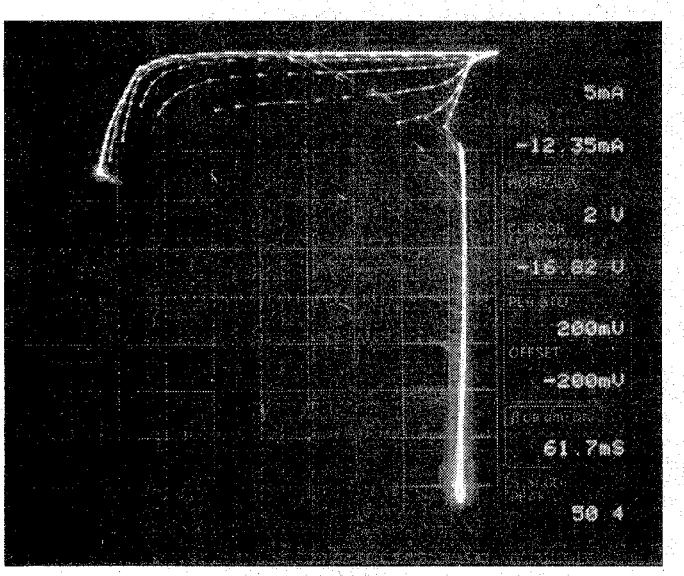


(b)

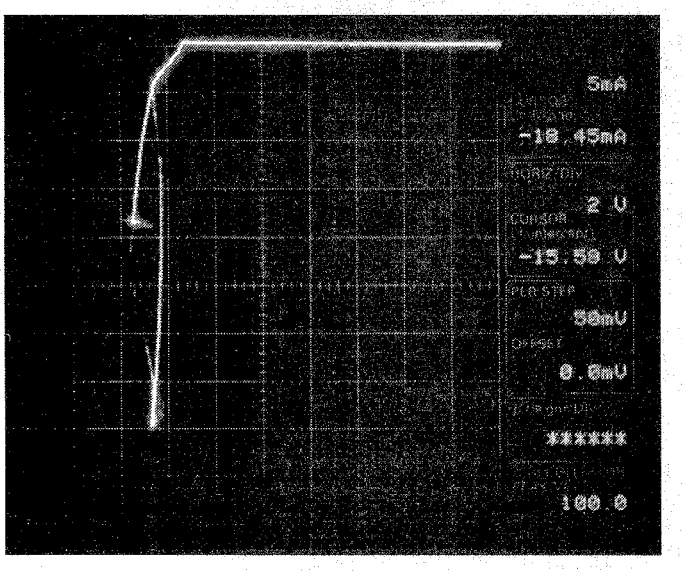
Fig. 15. The microphotograph of a pad with (a) the modified gate-coupled PTLSCR/NTLSCR ESD protection circuit corresponding to the layout of Fig. 14 and (b) the conventional CMOS ESD protection circuit with a PMOS device and an NMOS device.

trigger voltage due to the low gain of the parasitic lateral p-n-p device in the PMOS transistor.

The dc I–V characteristics of the gate-coupled NTLSCR and the gate-grounded NMOS is shown in Fig. 18. In Fig. 18(a), the I–V curves of the NTLSCR are measured by applying different positive voltages to the gate of Mn1 and a varying positive voltage on its anode. Fig. 18(b) shows the snapback characteristics of a gate-grounded NMOS in the conventional CMOS ESD protection circuit with W/L of 500/1.2 (μm). With the gate voltage of Mn1 at 0 V, the trigger voltage (current) of NTLSCR is 13.04 V (0.7 mA). But, if the gate voltage of Mn1 is increased, the trigger voltage of the NTLSCR is reduced. The effect of the coupled voltage on the gate of Mn1 on the trigger voltage of NTLSCR is shown in Fig. 19. The voltage coupled to the gate of Mn1 in order to trigger on the NTLSCR can be adjusted by the capacitor Cn. With a lower trigger voltage, the NTLSCR can be triggered faster into its latching state to bypass the PS-mode ESD stress. The holding voltage (current) of the NTLSCR is 1.25 V (6.18 mA). The typical turn-on resistance of the NTLSCR is about $1 \sim 2\ \Omega$. In Fig. 18(b), the trigger voltage (current) of the gate-grounded NMOS is 13.78 V (12.8 mA), and its snapback holding voltage (current) is 9.52 V (9.85 mA). The snapback holding voltage much lower than the trigger voltage is due to the higher gain of the parasitic lateral n-p-n device in the NMOS transistor. The holding voltage of NTLSCR is lower than that of the gate-grounded NMOS, so the ESD power dissipation in the NTLSCR is much lower than that in the gate-grounded NMOS. This is the main reason why an NTLSCR can sustain higher



(a)



(b)

Fig. 16. The I–V characteristics of (a) the PTLSCR with different negative voltages on the gate of Mp1 and (b) a PMOS device with its gate shorted to its source.

ESD stress within smaller layout area than a gate-grounded NMOS device.

B. ESD Test Results

ESD test results for the modified gate-coupled PTLSCR/NTLSCR ESD protection circuit are summarized in Table I. The conventional CMOS ESD protection circuit formed by a PMOS and an NMOS of W/L = 500/1.2 (μm) is also tested for comparison. The ESD tester used in this measurement is the *ZAP*MASTER produced by KeyTek Instrument Corp. [36]. The four modes of ESD stresses using both the HBM and machine-model (MM) ESD pulses are applied to the circuits to test their ESD robustness. The failure criterion is defined as the leakage current at the pad exceeds 1 μA under 5-V voltage bias after an ESD stress. The lowest (in absolute value) ESD failure voltage among

TABLE I
COMPARISON OF HBM AND MM ESD TESTING RESULTS

	Conventional CMOS ESD Protection Circuit with Large Dimension (W/L)				This Work			
	PMOS (500/1.2)		NMOS (500/1.2)		Gate-Couple PTLSCR		Gate-Couple NTLSCR	
Layout Area ($\mu m \times \mu m$)	158 X 92		166 X 100		110.2 X 68.3		107.0 X 65.2	
ESD-Sress Condition	PD-Mode	ND-Mode	PS-Mode	NS-Mode	PD-Mode	ND-Mode	PS-Mode	NS-Mode
HBM ESD Failure Voltage (V)	above 8000	-3000	1200	above -8000	above 8000	-5750	above 8000	above -8000
MM ESD Failure Voltage (V)	450	-350	150	-850	750	-500	600	-700

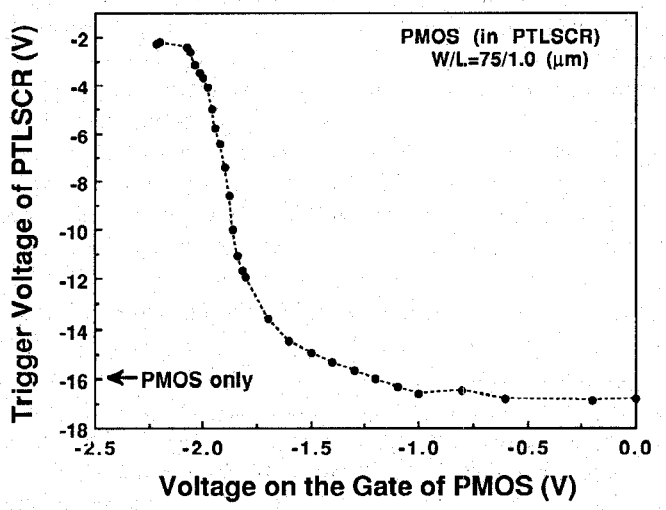
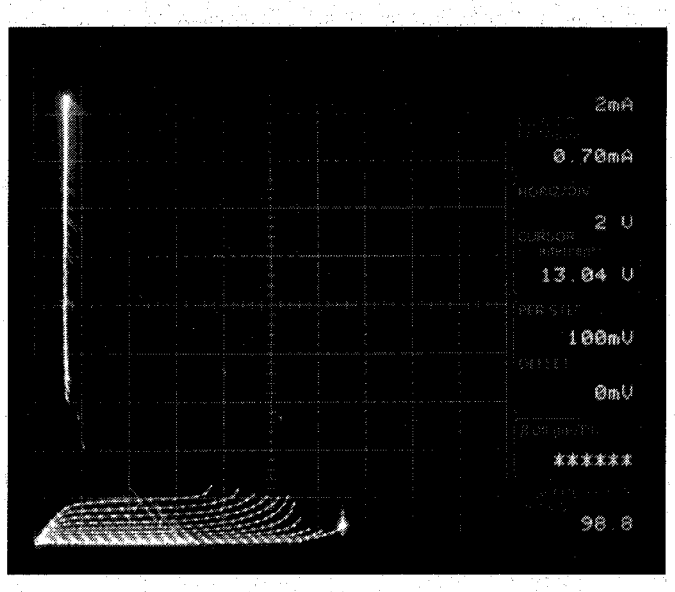
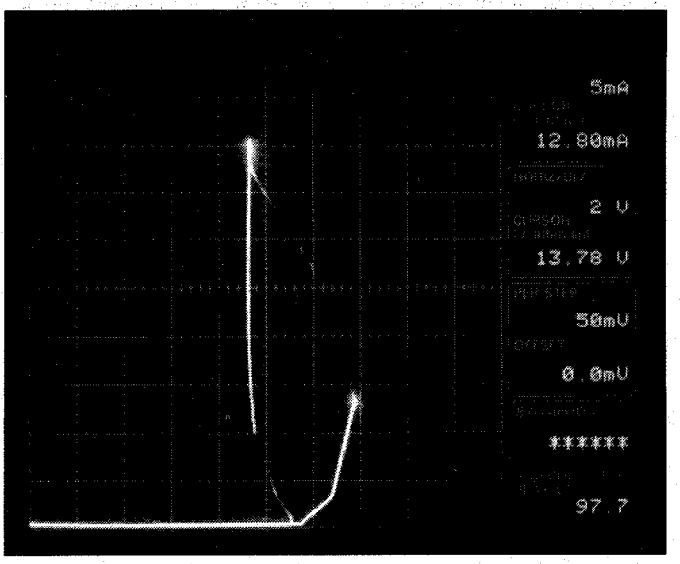


Fig. 17. Dependence of the trigger voltage of PTLSCR on the gate voltage of Mp1.



(a)



(b)

Fig. 18. The I–V characteristics of (a) the NTLSCR with different positive voltages on the gate of Mn1 and (b) a gate-grounded NMOS device.

the four modes of ESD stresses at the same pin is defined as the ESD failure threshold of the pin. The results in Table I show that this proposed ESD protection circuit can sustain up to 5750 (500) V of HBM (MM) ESD stress in a smaller layout area, but the ESD failure threshold of the conventional CMOS ESD protection circuit is only 1200 (150) V, even with a much larger layout area. The ESD protection devices in this proposed ESD protection circuit occupy 46.6% of the layout area of the conventional CMOS ESD protection circuit, but can sustain 4.8 (3.3) times HBM (MM) ESD-stress voltage. This verifies the excellent ESD-protection capability of the proposed gate-coupled PTLSCR/NTLSCR ESD protection circuit for deep-submicron CMOS IC's with smaller layout area.

The charged-device-model (CDM) ESD test is also applied to the proposed ESD protection circuit and the conventional CMOS ESD protection circuit to investigate their ESD robustness. In the CDM ESD test, a positive (or negative) ESD voltage is applied to the substrate by the *ZAP*MASTER socketed tester. The CDM ESD takes place when the input pad is grounded. A target of ± 1000 V is commonly used as an acceptable CDM ESD level for IC products. The CDM ESD test results are listed in Table II. The positive CDM ESD level of the conventional CMOS ESD protection circuit is greater than 2000 V because the NMOS device in the CMOS ESD

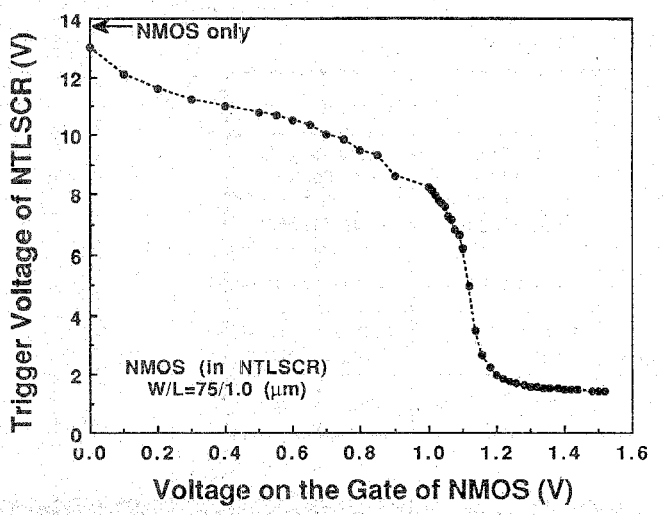


Fig. 19. Dependence of the trigger voltage of NTLSCR on the gate voltage of Mn1.

protection circuit provides a low-resistance forward-biased diode from the p-substrate to the input pad. In the negative CDM ESD test (the p-substrate is negatively charged and then the input pad is grounded), the NMOS device in the CMOS ESD protection circuit will go into snapback breakdown due to the reverse-biased drain-substrate junction. The NMOS device is expected to be weak in the negative CDM ESD stress, but the negative CDM ESD level of the conventional CMOS ESD protection circuit is up to -1900 V. This improvement is owing to the parasitic diode in the PMOS device connected from the input pad to VDD [37]. The positive (negative) CDM ESD level of the proposed gate-coupled PTLSCR/NTLSCR ESD protection circuit is up to 1400 V (-1900 V). In [37], it was reported that an LVTSCR device stands a low positive CDM ESD level of 300 V only. But, this proposed ESD protection circuit can sustain a positive CDM ESD stress as high as 1400 V because there is an N-well/p-substrate diode (D1) in the PTLSCR device structure. In Fig. 13, the diode D1 is formed by an N-well (connected to the pad) in the p-substrate. A P^+ diffusion (connected to VSS) in the p-substrate is placed close to the N-well of diode D1 in the layout. This diode provides an efficient discharging path to discharge the positive CDM ESD voltage from the p-substrate to the pad. The negative CDM ESD level is also improved by the diode D2 (connected from the pad to VDD) in the NTLSCR device structure. So, with the proper device and layout design as shown in Figs. 13 and 14, this proposed ESD protection circuit with smaller layout area can still provide robust enough ESD protection against the CDM ESD stress.

C. Gate-Coupling Efficiency

To verify the gate-coupling effect, a negative voltage pulse is directly applied to the pad with the VDD grounded to determine the ESD-trigger voltage of the gate-coupled PTLSCR in the ND-mode ESD-stress condition. The experimental setup is shown in Fig. 20(a) with a pulse generator *HP*8116. The rise time of a voltage pulse generated by *HP*8116 is around 7 ns, which is close to the rise time of HBM ESD event. An oscilloscope is used to monitor the voltage waveform of a negative pulse on the input pad. When the gate-coupled PTLSCR device is triggered on by the negative voltage pulse, the voltage waveform of the applied negative voltage pulse will be degraded due to the finite current output capability of the pulse generator *HP*8116. By using this direct and simple method to monitor the voltage waveform at the pad, the minimum voltage peak of the applied voltage pulse to trigger on the gate-coupled PTLSCR can be determined. The typical measured minimum voltage to trigger on the gate-coupled PTLSCR in the fabricated ESD protection circuit is shown in Fig. 20(b). It is shown in Fig. 20(b) that a negative voltage pulse of -7.56 V can trigger on the gate-coupled PTLSCR, while the trigger voltage of PTLSCR with 0 V on the gate of Mp1 is as high as -16.8 V.

TABLE II
CHARGED-DEVICE-MODEL ESD TESTING RESULTS

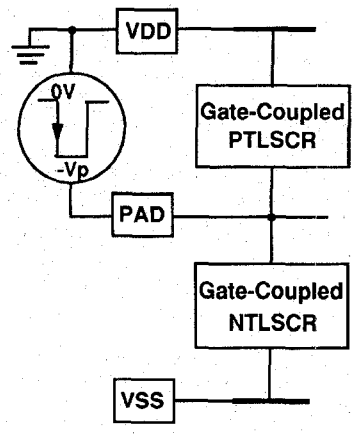
	CDM(+)	CDM(-)
This Work (Fig.15(a))	1400V	-1900V
Conventional ESD Protection Circuit (Fig.15(b))	>2000V	-1900V

Similar experimental setup can be used to measure the ESD-trigger voltage of the gate-coupled NTLSCR device in the PS-mode ESD-stress condition. The measurement setup is shown in Fig. 21(a), where a positive voltage pulse is directly applied to the pad with the VSS grounded to find the ESD-trigger voltage of the gate-coupled NTLSCR. By monitoring the voltage waveform at the pad, the minimum voltage peak to trigger on the gate-coupled NTLSCR can be determined. The typical measured minimum voltage to trigger on the gate-coupled NTLSCR in the fabricated ESD protection circuit is shown in Fig. 21(b). It is found in Fig. 21(b) that a positive voltage pulse of 7.03 V can trigger on the gate-coupled NTLSCR, while the trigger voltage of NTLSCR with 0 V on the gate of Mn1 is as high as 13.24 V.

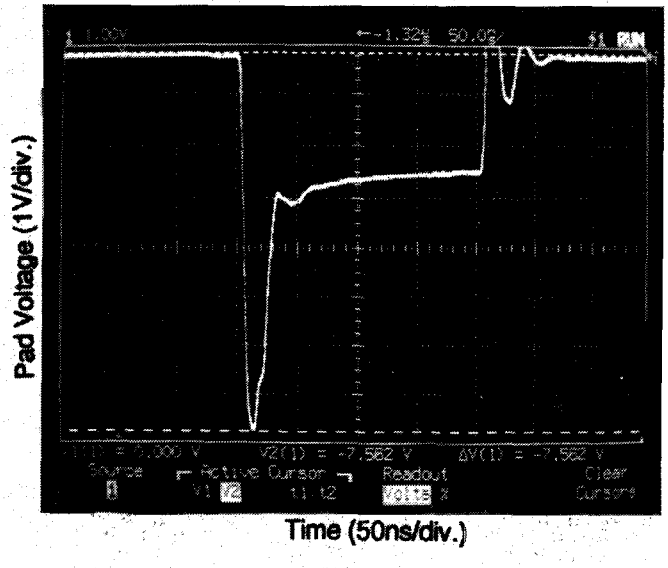
Figs. 20(b) and 21(b) have verified the efficiency of the gate-coupling technique to lower the ESD-trigger voltage of the PTLSCR and NTLSCR. With a trigger voltage of -7.56 V (7.03 V) in the gate-coupled PTLSCR (NTLSCR), this ESD protection circuit is not triggered on by the normal input signal with the voltage level from $0 \sim 3$ V in the low-voltage (3-V) IC operation (or $0 \sim 5$ V in the normal 5-V IC operation). The trigger voltage in the gate-coupled PTLSCR and NTLSCR devices also has enough voltage margin to the breakdown voltage of a 90-Å gate oxide, so the thinner gate oxide of input buffers in deep-submicron low-voltage CMOS IC's can be effectively protected.

D. Input Leakage

The leakage current is a concern for an ESD protection circuit connected to an input or output pin. Fig. 22 shows the comparison of leakage currents between the fabricated

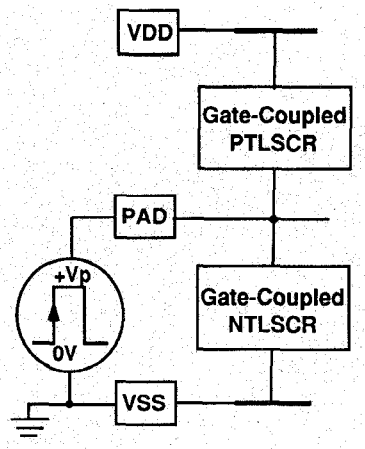


(a)

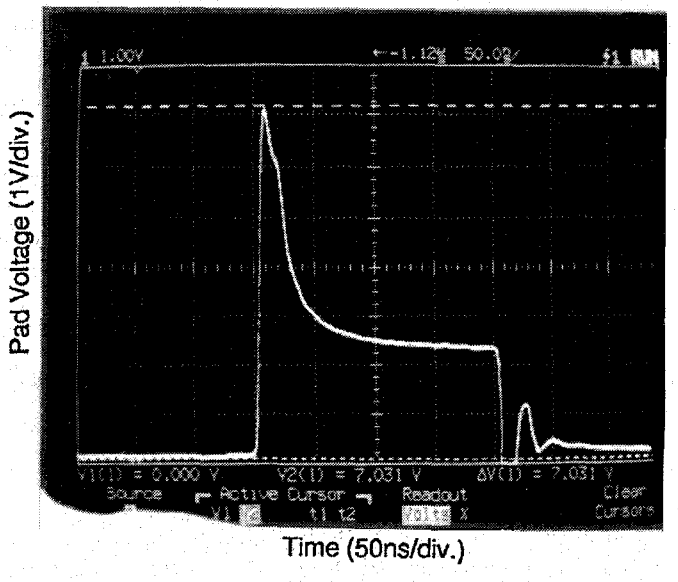


(b)

Fig. 20. (a) An experimental setup to measure the ESD-trigger voltage of the gate-coupled PTLSCR device in the ND-mode ESD-stress condition. (b) The measured voltage waveform at the pad as the gate-coupled PTLSCR is triggered on by the applied negative voltage pulse.



(a)



(b)

Fig. 21. (a) An experimental setup to measure the ESD-trigger voltage of the gate-coupled NTLSCR device in the PS-mode ESD-stress condition. (b) The measured voltage waveform at the pad as the gate-coupled NTLSCR is triggered on by the applied positive voltage pulse.

gate-coupled PTLSCR/NTLSCR ESD protection circuit and the conventional CMOS ESD protection circuit. The leakage current is measured (using an HP4145) by applying a voltage ramp from 0 V to 5 V to the input pad with 5-V VDD and 0-V VSS bias condition. In the line A of Fig. 22, the maximum input leakage current at 5-V bias in the gate-coupled PTLSCR/NTLSCR ESD protection circuit is only 1.7 pA. The maximum input leakage current in the conventional CMOS ESD protection circuit is up to 10.5 pA (the line B in Fig. 22). The input leakage current is related to the diffusion area connected to the pad. The layout area of the gate-coupled PTLSCR/NTLSCR ESD protection circuit is only 0.47 times that of the conventional CMOS ESD protection circuit, and hence the leakage current in the gate-coupled PTLSCR/NTLSCR ESD protection circuit is lower. Moreover, the input junction capacitance is also related to the diffusion area connected to the pad. The input capacitance of this gate-coupled PTLSCR/NTLSCR ESD protection circuit is therefore smaller than that of the conventional CMOS ESD protection circuit. With low leakage current and low input capacitance, as well as without a resistor between the pad and internal circuits, this gate-coupled PTLSCR/NTLSCR ESD protection circuit is more suitable to protect the output or input pins of analog IC's in high-precision applications.

V. Conclusion

By understanding both the turn-on mechanism of a lateral SCR device [34] and the capacitor-coupling design [35], the gate-coupling technique is merged into LVTSCR devices to invent an effective ESD protection circuit for deep-submicron low-voltage CMOS IC's without any process modification. A practical design example of the proposed gate-coupled PTLSCR/NTLSCR ESD protection circuit has been successfully verified. The ESD trigger voltage of the gate-coupled PTLSCR and NTLSCR devices can be modified by adjusting

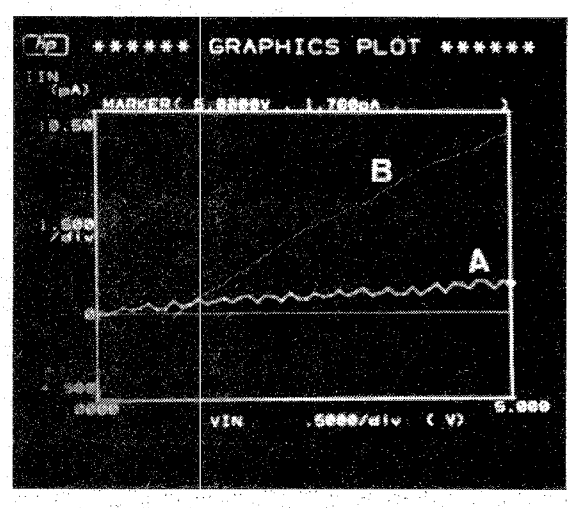


Fig. 22. Comparison of input leakage currents between the gate-coupled PTLSCR/NTLSCR ESD protection circuit (line A) and the conventional CMOS ESD protection circuit (line B) with 5-V VDD and 0-V VSS. X axis (0.5 V/div.) is voltage applied on the input pad, whereas Y axis (1.5 pA/div.) is the measured leakage current on the input pad.

the capacitors Cn and Cp, respectively. With a lower and tunable trigger voltage, this proposed ESD protection circuit is very suitable for deep submicron CMOS IC's in low-voltage, low-cost, high-density, high-speed, and high-reliability applications.

This proposed ESD protection circuit can also be merged into the layout of a CMOS output buffer to effectively protect the output transistors of deep submicron CMOS IC's. This ESD protection circuit can also be implemented in any conventional or advanced CMOS or BiCMOS processes.

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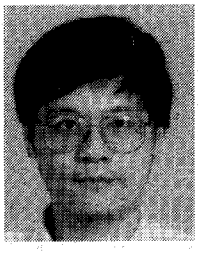

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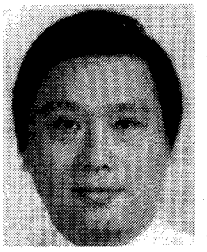

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