Area-Efficient Layout Design for CMOS Output Transistors

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Abstract—A novel layout design to effectively reduce the layout area of the thin-oxide NMOS and PMOS devices in CMOS output buffers with ESD consideration is proposed. With respect to the traditional finger-type layout, the large-dimension output NMOS and PMOS devices are realized by multiple octagonal cells. Without using extra ESD-optimization process, the output NMOS and PMOS devices in this octagon-type layout can provide higher driving/sinking current and better ESD robustness within smaller layout area. The drain-to-bulk parasitic capacitance at the output node is also reduced by this octagon-type layout. Experimental results in a 0.6- μ m CMOS process have shown that the output driving (sinking) current of CMOS output buffers in per unit layout area is increased 47.7% (34.3%) by this octagontype layout. The HBM (MM) ESD robustness of this octagontype output buffer in per unit layout area is also increased 41.5% (84.6%), as comparing to the traditional finger-type output buffer. This octagon-type layout design makes a substantial contribution to the submicron or deep-submicron CMOS IC's in high-density and high-speed applications.

I. INTRODUCTION

S CMOS technology has been scaled down into the A submicron regime, the advanced processes, such as thinner gate oxide, shorter channel length, shallower source/drain junction, Lightly-Doped Drain (LDD) structure, and silicided diffusion, greatly degrade electrostatic discharge (ESD) robustness of submicron CMOS IC's [1], [2]. In order to attain acceptable ESD robustness, the protection devices in the submicron CMOS ESD protection circuits often have to be designed with larger dimensions than those in the traditional long-channel CMOS technologies. Besides, in order to provide CMOS output buffers with enough driving/sinking capability, the device dimensions (width/length ratios) of output NMOS and PMOS devices are generally enlarged up to several hundreds. Moreover, the device dimensions of CMOS output buffers in the low-voltage application (V_{DD} = 3.3 V, 2.5 V, ...) are considerably increased to provide sufficient driving/sinking capability. With such large device dimensions of output transistors, the tapered buffers have been designed to provide high-speed operations [3]-[8]. The larger output transistors need more inverter stages inserted in the tapered buffer to minimize the propagation delay for highspeed applications. This causes an extra increase of layout area

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on the CMOS output buffer. However, submicron CMOS IC's in the high-integration applications may have the pin counts exceeding 200. In such high-pin-count submicron CMOS IC's, the pad pitch is reduced to around only 100 μ m. The layout area available for each output (or input) pad with the output transistors (or ESD protection circuits) including latchup guard rings is seriously limited. Even if the traditional finger-type layout style is adopted to draw large-dimension NMOS and PMOS devices, the total layout area of output or input pads with output buffers, ESD protection circuits, and latchup guard rings would still have to be reduced while the submicron CMOS IC is in the pad-limited condition.

Several articles had been written to overcome the aforementioned problems. In 1989, Baker [9] proposed a waffle (rectangular) layout style to enhance the ESD hardness of an NMOS output transistor. In [9], the waffle layout is shown to offer better ESD protection capability than the finger-type layout within the same layout area. In 1992, Vemuru [10] confirmed that the waffle-type layout contributes about 10% area reduction to that of the finger-type layout, as well as the waffle-type layout produces a lower gate resistance suitable for wide-band or low-noise applications.

Recently, the relations between the layout parameters and the ESD hardness of thin-oxide output NMOS devices in submicron CMOS technologies have been investigated. It had been found that the spacing from the drain contact to the edge of gate oxide is an important layout parameter to the ESD robustness of thin-oxide devices in the nonsilicided process [11]-[13]. A larger spacing from the drain contact to the gate-oxide edge leads to higher ESD reliability. The suitable spacing was found to be about $5 \sim 6 \ \mu m$ in submicron CMOS technologies to sustain better ESD protection without significantly increasing the layout area. The spacing from the source contact to the edge of gate oxide in the finger-type layout can be reduced below 1 μ m, but that in the waffle-type layout is kept the same as the spacing from the drain contact to the gate-oxide edge. Under this spacing constraint, the waffle style will occupy more layout area than the traditional fingertype style with the same W/L ratio. Therefore, how to reduce the layout area without affecting the ESD reliability and the output driving capability has become an important challenge to the CMOS output buffer in submicron or deep-submicron CMOS technologies.

In this paper, a new layout design is proposed to realize CMOS output buffers with a reduced layout area and enhanced ESD reliability, but without using any extra ESD-optimization process. The new layout style is to implement the smalldimension NMOS (or PMOS) device into a cell with an



Fig. 1. A schematic top view of the traditional finger-type layout for an NMOS device.

octagonal layout structure, called as the octagon cell. Then an NMOS (or PMOS) of large dimension can be assembled by a plurality of small-dimension octagon cells. Using this layout design, the layout area of a CMOS output buffer with the same large device dimensions only requires $60 \sim 80\%$ of the layout area of the traditional finger-type layout. This new octagon-type layout can be used as well to improve ESD robustness of input ESD protection circuits with the thin-oxide NMOS or PMOS devices.

II. CONSIDERATION ON THE TRADITIONAL FINGER-TYPE LAYOUT

The traditional finger-type layout for an NMOS device is shown in Fig. 1. Its cross-sectional view along the line A-A' of Fig. 1 is shown in Fig. 2, which is demonstrated in an N-well/p-substrate CMOS process. In Fig. 1, a largedimension NMOS device is separated as four parallel smalldimension NMOS devices. The number of fingers depends on the device dimension. The spacing from the drain contact to the poly-gate edge is marked as "d," while the spacing from the source contact to the poly-gate edge is marked as "S". For better ESD robustness of the CMOS output buffer in nonsilicided submicron CMOS technologies without using extra ESD-optimization process, the value of "d" is preferably about 5~6 μ m [11], [12]. Since the value of S has no important effect on the ESD reliability of the CMOS output buffer, a preferred value of S of about 1 μ m is often used in the finger-type layout to save layout area. Outside the source region, there are two latchup guard rings surrounding the whole NMOS device. One is the P+ diffusion connected to ground (GND) to offer the substrate bias. The other is the N+ diffusion connected to VDD as a dummy collector to prevent CMOS latchup. As shown in Figs. 1 and 2, the spacing for suitable latchup guard rings is denoted as S_1 , which is process dependent and is often specified in the design rules.

However, in the traditional finger-type layout, there is another important spacing denoted as " S_2 " in Fig. 1, which may degrade the ESD robustness of a CMOS output buffer. To explain the importance of this spacing S_2 , a schematic crosssectional view taken along the line B-B' of Fig. 1 is illustrated in Fig. 3. In Fig. 3, a parasitic diode D_1 exists between the P+ diffusion (connected to GND) in the p-substrate and the N+ diffusion of the drain. If the spacing S_2 is too small, the diode D_1 will break down to discharge ESD current (due to the peak-discharging effect on the finger's end of the drain) before the NMOS drain breaks down when a positive ESD voltage occurs on the output pad. Because the drain edge in this side has a peak structure and is shorter than the edge parallel to the source side, this diode D_1 is vulnerable to ESD stress if S_2 is too small. Even the spacing from the drain contact to this edge (D_1) is larger than the spacing d in the finger-type NMOS device, the ESD hot spot may still occur at this edge due to the peak structure at the end of the finger. A typical EMMI photograph of ESD damage on the diode D_1 of a finger-type layout is shown in Fig. 4, where a hot spot occurs only on the end of a drain finger. As the picture shown in Fig. 4, the spacing form the drain contact to the active area edge (in the B-B' direction of Fig. 1) is 5.5 μ m. The drain contact to the poly-gate edge (in the A-A' direction of Fig. 1) is 5 μ m. The spacing S₂ in Fig. 4 is only 4 μ m. The ESD failure in Fig. 4 is due to the Machine-Model (MM) PS-mode ESD stress. The MM ESD stress has a much faster rise time (about $1 \sim 2$ nS) on the ESD current waveform than that (about \sim 15 nS) of the HBM ESD stress. In the faster ESD transition, not only the layout-spacing effect but also the peak-discharging effect of the finger-type layout may cause the unexpected ESD damage on the finger's end. This seriously reduces the ESD performance of CMOS output buffers in the finger-type layout. Thus, in consideration of ESD reliability, this spacing S_2 had better be greater than the spacing from the drain-contact edge to the source-contact edge. But with such a large spacing S_2 , the total layout area of the finger-type device is increased.

The spacings d and S being large or not are dependent on the process which has the silicided/nonsilicided diffusion or a floating substrate. In the advanced CMOS process with the silicided diffusion, a large spacing d becomes useless for ESD improvement in the finger-type layout due to the very low sheet resistance of the silicided material covered on the N+ diffusion. This silicided diffusion seriously reduces the ESD robustness of output transistors [2], [13]. In the silicided process, the spacings d and S are kept at the minimum values of the design rules to save layout area [13], and some extra modified processes or designs are used to improve ESD robustness of I/O devices. But, for technologies with the floating substrates (such as SOI or the DRAM in the p-substrate process with an on-chip negative substrate bias), the spacings d and S should be symmetrically large if the process is nonsilicided [13].



Fig. 2. A schematic cross-sectional view of NMOS device along the line A-A' in Fig. 1.



Fig. 3. A schematic cross-sectional view of NMOS device along the line B-B' in Fig. 1.



Fig. 4. An EMMI microphotograph of ESD damage on a CMOS output buffer after a PS-mode ESD stress. Only a hot spot is observed at the end of a drain finger.

Without modifying the process steps or using any silicidedblock mask in the silicided process, a method to improve the ESD robustness of output buffers with the silicided diffusion is to adopt a modified N-well drain structure for the NMOS device [14], [15]. A schematic cross-sectional view of the modified drain with the N-well structure is illustrated in Fig. 5,



Fig. 5. A schematic cross-sectional view of NMOS device with a modified N-well drain structure in a CMOS process with silicided diffusion.

where the N+ diffusion of the drain region from the drain contact to the gate-oxide edge is broken by the field-oxide region. The drain current is conducted from the drain contact to the channel through the inserted N-well structure. Using this N-well structure to block the silicided diffusion, the ESD robustness of output NMOS devices can be significantly improved without any process modification or extra mask. But, this inserted N-well structure increases the value of the spacing d. So, the layout area of an output NMOS in the finger-type layout with this modified N-well drain structure will be much increased. Of course, if extra ESD-optimization processes are added into the process flow to optimize the drain structure for I/O devices, the spacing d is not necessary as large as $5 \sim 6 \mu m$. However, the cost of fabrication and steps of process flow have to be increased. Generally, the more process steps and masks lead to a lower yield and longer process throughput time, so as to increase the cost of the IC products.

From the aforementioned description on ESD protection in both the nonsilicided and the silicided (by using the N-well drain structure) processes, the spacing d should be increased to avoid the degradation of ESD performance in the submicron or deep-submicron CMOS technologies without using any process modification. But, the increased spacing d, due to ESD consideration, will lead to a significant increase in the layout area of a CMOS output buffer which has large device dimensions.

III. OCTAGON-TYPE LAYOUT DESIGN

To reduce the total layout area of a CMOS output buffer without degrading its ESD reliability and without using extra process modification, a novel octagon-type layout used to



Fig. 6. A schematic top view of the proposed octagon-type layout for an NMOS device.

realize CMOS output transistors [16] is presented in this Section.

A. Layout Structure

A schematic octagon cell to assemble an output NMOS transistor is shown in Fig. 6. Its schematic cross-sectional view along the line A-A' of Fig. 6 in the N-well/p-substrate CMOS process is illustrated in Fig. 7. This octagon-type layout can be implemented by any CMOS or BiCMOS processes. In Fig. 6, the black octagonal region in the center of an octagon cell is the contact for a metal line connecting to the N+ diffusion (drain) of the NMOS device. A dashed line with an octagonal shape enclosing the octagonal drain contact is an N-well, which is made to avoid the ESD-stress-induced contact spiking effect. Under a high ESD stress, the metal on the contact may be ruptured and melted through the N+ diffusion into the p-substrate by the ESD energy. This will cause a short-circuit path from the output pad (connected to the contact) to ground (the bias of the p-substrate). Thus, an N-well inserted into the N+ diffusion of drain, as the cross-sectional view shown in Fig. 7, can effectively improve ESD robustness of the thinoxide NMOS device. In the silicided diffusion process, the modified N-well drain structure of Fig. 5 can be used in the octagon cell to provide the required ESD reliability.

In the advanced submicron or deep-submicron CMOS technologies, the contact damage is very rarely observed where the barrier metals (such as titanium-tungsten) are used between the aluminum metallization and silicon [17]. The use of TiW barrier metal in the contact has greatly improved contact integrity, and high eutectic temperature has almost eliminated the contact melting as a failure mode in advanced technologies [13]. Due to the N-well structure under the drain contact and the use of advanced contact materials, the highest temperature due to current stress is not located on the contact but on the drain junction. So, the drain contact in the octagon-type layout has a reasonable reliability. The large drain contact in Fig. 6 can be separated as multiple small contacts and placed in an octagonal shape to improve contact reliability in the conventional CMOS process with only the aluminum contact.

The gate made by a poly in the octagon cell is also drawn in an octagonal ring. The N+ diffusion of source is also drawn in an octagonal shape. The source contacts of the octagon cell are arranged in an octagonal pattern around the ring gate. Outside the NMOS device, there is a P+ diffusion in the p-substrate connected to ground to offer the substrate bias for the normal CMOS operations. All the layout elements in the octagon cell, including the contact configurations, should be drawn as concentric and symmetrical as possible to ensure uniform current flow in the NMOS device, so as to increase the ESD robustness of output transistors [18].

For ensuring the most uniform ESD current flow, a circletype layout is theoretically the best choice. But, in the present CAD tools used to generate IC layouts and the masks for IC fabrication are still unable to make a real circuit-type device. The octagon layout style is not the only choice to implement the output transistors. The layout style can be implemented in any regular polygon of n sides. For $n \rightarrow \infty$, the layout is nearly a real circle type. But a polygonal layout with a larger n, it becomes more difficult and complex to be drawn in the present CAD tools. Thus, the octagon style is a more practical choice for the present CAD tools of IC layout.

Based on the basic octagon cell of Fig. 6, an NMOS device with larger dimension can be assembled by a plurality of the basic octagon cells. A layout example of a large-dimension NMOS device assembled by 15 octagon cells is shown in Fig. 8, which is realized by a $0.6-\mu m$ single-poly triple-metal CMOS technology with the double latchup guard rings. In Fig. 8, there are P+ diffusions (connected to GND) among the octagon cells to offer the voltage bias for the p-substrate. These uniformly-distributed P+ islands (diffusions) for substrate bias can enhance the uniform turn-on behavior of the multiple octagon cells during the ESD stress. In Fig. 8, the drain contact in each octagon cell is drawn in an octagonal shape with a diameter of 2 μ m, and the spacing d(S) is 5 (1) μ m. Since the spacing S_2 of the finger-type layout is absent in this octagontype layout, the layout area of the octagon-type devices can be further reduced. Moreover, because there is no parasitic diode D_1 directly closing to the drain edge and no peak structure as that of the drain finger's end, the ESD robustness of the octagon-type device is not degraded by the unexpected diode breakdown at the drain finger's end. The total device dimension (W/L) of the output NMOS in Fig. 8 is 804/0.8 (μ m/ μ m), which only occupies a layout area of $110 \times 74 \ \mu$ m². This layout technique can be alternatively applied to realize the large-dimension PMOS device.

B. Calculation of Layout Area

The total layout area of an NMOS transistor in the octagontype layout can be calculated by the following equations:

$$\mathbf{A_{total}} = \left\{ \left[\left(\frac{1 + \sqrt{2}}{8} \right) w + 2L + 2S \right] \cdot N + 2S_1 \right\} \\ \cdot \left\{ \left[\left(\frac{1 + \sqrt{2}}{8} \right) w + 2L + 2S \right] \cdot M + 2S_1 \right\}$$
(1)

where

- L channel length;
- W total channel width of the NMOS device;
- $w = \frac{16d+8c}{1+\sqrt{2}}$, which is the channel width of a single octagon cell;
- d spacing from the drain contact to the poly-gate edge;



Fig. 7. A schematic cross-sectional view of an octagon-type NMOS device along the line A-A' in Fig. 6.



Fig. 8. A layout example of an output NMOS transistor realized by the octagon-type layout with 15 octagon cells.

- S spacing from the center of source contact to the poly-gate edge;
- c diameter of the octagonal drain contact in the octagon cell;
- S_1 total spacing of double guard rings;
- M number of octagon cells in the column direction of the whole NMOS layout; and
- N number of octagon cells in the row direction of the whole NMOS layout.

The total number of the octagon cells in a whole NMOS layout is $M \times N$. The total perimeter of the drain N+ diffusion in the whole NMOS layout is the same as W. The total layout area of the drain N+ diffusion can be obtained as

$$\mathbf{A}_{\mathbf{D}} = \left(\frac{1+\sqrt{2}}{32}\right) \cdot w^2 \cdot M \cdot N. \tag{2}$$

The layout area and the perimeter of the drain diffusion have an effect on the drain capacitance of the NMOS device. Using the HSPICE level-28 capacitance parameters [19], the total drain capacitance can be calculated as

$$\mathbf{C}_{\mathbf{Drain}} = \mathbf{C}_J \cdot \mathbf{A}_{\mathbf{D}} + \mathbf{C}_{J \mathrm{GATE}} \cdot W \tag{3}$$

where C_J is the bulk junction capacitance, and C_{JGATE} is the gate-edge sidewall bulk junction capacitance.

A similar calculation applied to investigate the total layout area and the drain capacitance of an NMOS device in the finger-type layout is described in the Appendix.

C. Comparison to Finger-Type Layout

To verify the area-efficient advantage of the proposed octagon-type layout, comparisons of the total layout area between the traditional finger-type layout and the octagontype layout are made in Fig. 9 with different spacings dfrom $3 \sim 10 \ \mu\text{m}$. This spacing d for ESD consideration in the silicided (using N-well structure without silicided-block mask) or nonsilicided diffusion processes has an impact on the total layout area of output CMOS buffers. The total layout area in Fig. 9 includes the spacing S_1 of 10.3 μ m (the spacing of double latchup guard rings) in both finger-type and octagontype layouts. In the traditional finger-type layout, the spacing S_2 is 6 μ m. The length of each poly finger in the traditional finger-type layout is equal to each other. A quasiminimum layout area of the finger-type layout, following the 0.6- μ m CMOS design rules as shown in the Appendix, is used as a comparison reference. All the channel lengths of NMOS devices in the finger-type layout or octagon-type layout are 0.8 μ m. The spacing S (from the source contact to the polygate edge) in both the finger-type and the octagon-type layouts is kept the same as 1 μ m. In Fig. 9(a), as the spacing d is 3 μ m, the total layout area of the octagon-type layout is a little (about 5%) less than that of the finger-type layout. In Fig. 9(b), as the spacing d is 5 μ m, the total layout area of an octagon-type NMOS device with a larger channel width is significantly reduced as compared to that of the finger-type layout. For example, as the NMOS device dimension (W/L)is 800/0.8, the total layout area in the traditional finger-type



Fig. 9. Comparisons of total layout area between the finger-type layout and octagon-type layout under different spacings d: (a) $d = 3 \mu m$; (b) $d = 5 \mu m$; (c) $d = 8 \mu m$; and (d) $d = 10 \mu m$.

layout is 10842 μ m², but that in the octagon-type layout is only 8676 μ m². The total layout area of the NMOS in the octagon-type layout is only 80% of that in the finger-type layout. This shows the excellent area efficiency of the octagontype layout. In Fig. 9(c), as the spacing d is increased to 8 μ m, the area ratio of octagon-type layout to finger-type layout is reduced to about 65%. As the spacing d is increased to 10 μ m in Fig. 9(d), this area ratio is reduced to about only 55% if the device channel width is large. The relations between the device channel width and the percentage of area ratio (octagon-type to finger-type) under the different layout parameters d are shown in Fig. 10. It is clearly shown that the octagon-type layout can significantly reduce the total layout area of an output transistor with a large device dimension, while the spacing dis required to be large due to ESD consideration. In Fig. 10, the octagon-type devices have much smaller layout area than the finger-type devices as the spacing d or the channel width are increased. This comparison obviously reveals the excellent advantage of area reduction in this octagon-type layout used to realize the output transistors with large device dimensions.

Moreover, the drain-to-bulk parasitic capacitance at the output node is also reduced by this multiple-cell octagon-type layout design. In Fig. 11, the drain capacitance as a function of device channel width for the octagon-type and finger-type de-



Fig. 10. The relations between the device channel width and the percentage of layout area ratio (octagon-type to finger-type) under different layout parameters d.

vices under the different layout parameters d from 3 to 10 μ m is illustrated. The equations used to theoretically calculate the drain capacitance have been shown in (3) and (A.4) for the octagon-type and the finger-type layouts, respectively. The



Fig. 11. Comparisons of drain parasitic capacitance between the finger-type layout and octagon-type layout under different spacings d: (a) $d = 3 \mu m$; (b) $d = 5 \mu m$; (c) $d = 8 \mu m$; and (d) $d = 10 \mu m$.



Fig. 12. The relations between the device channel width and the percentage of drain capacitance ratio (octagon-type to finger-type) under different layout parameters d.

drain capacitance in the octagon-type layout is only about 70~55% of that in the finger-type layout under the spacing d of 3~10 μ m. The ratio (octagon-type layout to finger-type layout) of the drain capacitance under different spacings d is shown in Fig. 12. The capacitance ratio is almost independent to the device channel width, but strongly dependent to the

spacing d. The relations between the drain capacitance ratio and the spacing d are shown in Fig. 13, which illustrates the reduction in the drain capacitance ratio while the spacing dis increased. Theoretically, there is no the C_{JSW} term, as the third term shown in (A.4), in the (3). Under the same device dimension and the layout spacings, the capacitance ratio eventually has a smaller value than the area ratio. For the typical spacing d of 5 μ m, the drain capacitance ratio is 62.6% in the 0.6- μ m CMOS process. This obviously shows that the octagon-type layout can significantly reduced (about 37.4%) the drain capacitance as comparing to that in fingertype layout. So, this octagon-type layout design provides the CMOS output buffer with a lower output capacitance. Due to the lower capacitance, this octagon-type layout is more suitable for CMOS output buffers in high-speed or high-frequency applications.

D. Discussion

In the processes with the floating substrate, such as the DRAM with a p-type substrate, the negative substrate bias is added to the whole p-substrate. In this condition, the spacing S should be as large as the spacing d to provide a better ESD reliability in a nonsilicided process. As the spacing S is large, the area efficiency of the octagon-type layout is reduced. The



Fig. 13. The relations between the drain capacitance ratio (octagon-type to finger-type) and the spacing d.



Fig. 14. A microphotograph of a fabricated CMOS output buffer with octagon-type layout on both NMOS and PMOS devices.

octagon-type layout may have a layout area near to that of the finger-type layout. But, the spacing S_2 in the finger-type layout still has to be large enough to avoid the unexpected ESD damage on the finger's end. On the contrary, the multiplecell octagon-type layout has a better symmetrical structure to provide the uniform turn-on behavior under the ESD-stress condition.

Besides, in the DRAM layout, it is almost in the corelimited condition. The layout area for the I/O pads including the ESD protection circuits or output buffers is not critical. Therefore, the layout area for the output buffers in the DRAM chip is not seriously limited. However, in the most standard CMOS processes for ASIC applications, the octagon-type layout can provide the excellent area efficiency for the CMOS output buffers without using extra ESD-modification process. Especially, in the pad-limited and high-pin-count condition, the layout area for the I/O pads is seriously limited to save chip size. Under the pad-limited condition, the octagon-type layout can effectively save the layout area for the chips.

IV. EXPERIMENTAL RESULTS

One set of CMOS output buffers realized in the octagontype layout has been fabricated and measured in a 0.6- μ m nonsilicided CMOS process. A microphotograph of the fabricated CMOS output buffer is shown in Fig. 14, where both the NMOS and PMOS devices are realized in the octagontype layout. Corresponding to the layout example of Fig. 8, the device dimensions (W/L) of PMOS and NMOS devices



Vds(0.5V/div)

Fig. 15. The measured I-V curves of the octagon-type output NMOS device in Fig. 14.

in Fig. 14 are all 804/0.8 (μ m/ μ m). The layout area for PMOS or NMOS devices is the same as $110 \times 74 \ \mu$ m², which includes the double latchup rings. A CMOS output buffer realized by the traditional finger-type layout is also fabricated in the same CMOS process with the device dimensions of W/L = 720/0.8for both PMOS and NMOS devices, which occupies a layout area of $112 \times 100 \ \mu$ m². The spacing d in the octagon-type layout and the finger-type layout is the same as 5 μ m. The spacing S_1 of latchup double rings in these two layouts is kept identically.

A. Output Driving/Sinking Current

The I-V curves of the octagon-type NMOS device in Fig. 14 are measured and shown in Fig. 15, where the I-Vcurves are as smooth as those in the finger-type layout. The octagon-type PMOS device also has the same I-V curves as that of a finger-type PMOS device without any degradation on the waveforms of the I-V curves. This verifies that an MOSFET in the octagon-type layout can provide the same device I-V characteristics as that in the finger-type layout. The drain current of the NMOS (PMOS) device under the voltage bias of $V_{\rm ds}$ = 3 V (-3 V) and $V_{\rm gs}$ = 3 V (-3 V) is measured with its source grounded. This drain current is used as a parameter to compare the sinking (driving) capability of per unit layout area in both finger-type and octagon-type layouts. The measured drain currents of CMOS output buffers in these two layouts are summarized in Table I. The current driving/sinking capability of per unit layout area is also listed in Table I to verify the area efficiency. The maximum output sinking (driving) current in per unit layout area of the output NMOS (PMOS) device in the octagon-type layout is 13.12 (6.59) $\mu A/\mu m^2$, but that in the finger-type layout is only 9.77 (4.46) $\mu A/\mu m^2$. So, the NMOS (PMOS) device in the octagon-type layout provides an increase of 34.3% (47.7%) in the output sinking (driving) current of per unit layout area, as comparing to the devices realized by the finger-type layout. This practically confirms the excellent area efficiency of the proposed octagon-type layout design for output transistors.

	Finger-type Layout	Octagon-type Layout
W/L (μm)	720/0.8	804/0.8
Layout Arca (µm ²)	112×110	110×74
NMOS drain current Ids (Vds=Vgs-3V)	120.4 mΛ	106.8 mA
PMOS drain current Ids (Vds-Vgs3V)	-54.95 mA	-53.69 mA
NMOS Ids of per unit Layout Area	9.77 μA/μm²	13.12 µA/µm ²
PMOS Ids of per unit Layout Area	-4.66 μΛ/μm²	-6.59 μΛ/μm ²

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TABLE	Π
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	Finger-type Layout	Octagon-type Layout
	720/0.8	804/0.8
Layout Area (µm ²)	112×110	110×74
IIBM		
ESD pass voltage	6500 V	6000 V
MM		
ESD pass voltage	800 V	950 V
CDM		
ESD pass voltage	> ± 2000 V	> ± 2000 V
HBM pass voltage of		
per unit Layout Area	0.53 V/µm ²	0.74 V/µm ²
MM pass voltage of		
per unit Layout Area	$0.065 \text{ V/}\mu\text{m}^2$	0.12 V/µm ²

TABLE III

	Finger-type Layout		Octagon-type Layout			out		
	PS-mode	NS-mode	PD-mode	ND-mode	PS-mode	NS-mode	PD-mode	ND-mode
HBM (V)	7000	> 8000	>8000	6500	6000	>8000	>8000	8000
MM (V)	800	950	950	850	950	>1000	>1000	950

B. Output ESD Robustness

ESD reliability is another important issue for CMOS output buffers in submicron or deep-submicron CMOS technologies. The ESD test results including the HBM (Human-Body Model), MM (Machine Model), and CDM (Charged-Device Model) ESD events are listed in Table II. There are four modes of ESD stresses on a pin with respect to VDD and VSS pins [20]. In general, the CMOS output buffer is more vulnerable to the PS-mode and ND-mode ESD stresses due to the snapback breakdown of the output NMOS or PMOS devices during ESD events. The CMOS output buffer is stronger in the NS-mode and PD-mode ESD stresses, because the drain-to-bulk parasitic diodes in the CMOS output buffer are forward biased to bypass ESD current. The ESD-sustained voltages of the octagon-type and finger-type CMOS output buffers (in Table II) in the four modes of ESD stresses are listed in Table III in details. The ESD pass voltage of a pin is defined as the value of the highest ESD voltage that the pin can sustain without causing any damage in the four modes of ESD stresses. So, the octagontype (finger-type) layout provides an HBM ESD-pass voltage of 6000 V (6500 V) and an MM ESD-pass voltage of 950 V



Fig. 16. An EMMI microphotograph of ESD damage on a CMOS output buffer in the octagon-type layout after a PS-mode ESD stress. The hot spots are uniformly present on every octagon cell of the NMOS device.

(800 V) in Table III. The CDM ESD test results in Table II are tested by a socket-type CDM ESD tester, which is the ZapMaster produced by the KeyTek corp. with a maximum CDM ESD voltage of ± 2000 V. The CDM ESD pass voltages in both the octagon-type layout and finger-type layout are all greater than 2000 V due to the large device dimensions in the layout.

As seen in Table II, the CMOS output buffer in the octagontype layout can pass 6000-V HBM ESD, but that in the finger-type layout can pass 6500-V HBM ESD. However, in the MM ESD testing, the CMOS output buffer in the octagontype layout can pass 950-V ESD, but that in the finger-type layout can only pass 800-V ESD. This is due to the P+ islands connected to VSS (the N+ islands connected to VDD) as the p-substrate (N-well) bias among the multiple octagon cells of an NMOS (PMOS) device in the octagon-type layout. In the finger-type layout, the P+ diffusion (or N+ diffusion) for the p-substrate (N-well) bias often surrounds the whole NMOS (or PMOS) device only at the outside, but the internal fingers of the finger-type device are far from the substrate bias. This may easily lead to the nonuniform turn-on phenomena among the multiple fingers of a finger-type device during the fast-transient ESD stress and therefore causes a low ESD reliability [18]. Especially, the ESD transition in the MM ESD event is much faster than that of the HBM ESD event. The nonuniform turnon phenomena among the multiple fingers will more easily happen in the MM ESD stress. The ESD current discharging from the drain to the source of the octagon-type NMOS and PMOS devices is quite uniform, so its ESD robustness can be significantly improved within a smaller layout area. This is the main reason why the CMOS output buffer in the finger-type layout with both a larger layout area and a larger drain area is still weaker than that in the octagon-type layout under the MM ESD stresses. An EMMI microphotograph of a CMOS output buffer in the octagon-type layout, which is damaged after the PS-mode HBM ESD stress, is shown in Fig. 16. The hot spots are uniformly present on every octagon cell of the output NMOS device. This is quite different to the hot spot on the finger-type layout of Fig. 4. The octagontype layout design can effectively improve the uniform turn-on characteristics of the output devices during ESD stresses. So, the ESD performance of output devices is also improved by this octagon-type layout design, especially in the faster MM ESD transition.

The ESD robustness of per unit layout area is also calculated and shown in Table II. The ESD robustness of per unit layout 0.74 (0.12) V/ μ m² in HBM (MM) ESD stress, but that in the finger-type layout is only 0.53 (0.065) V/ μ m². Thus, the CMOS output buffer in the octagon-type layout provides an increase of 41.5% (84.6%) in the HBM (MM) ESD robustness of per unit layout area, as comparing to the CMOS output buffer in the finger-type layout. The CDM ESD robustness in per unit layout area of a CMOS output buffer realized by this octagon-type layout can be greater than 0.25 V/ μ m². This has verified the excellent area efficiency of the octagon-type output buffer for ESD protection.

Besides, owing to the high ESD robustness as listed in Table II, the octagon-type CMOS output buffer can become an area-efficient input ESD protection circuit, as the gate of NMOS (PMOS) device in the CMOS output buffer is shorted to ground (VDD).

V. CONCLUSION

An octagon-type layout design for the thin-oxide NMOS and PMOS devices in CMOS output buffers has been successfully verified in a 0.6- μ m CMOS process without using extra ESD-optimization process. The large-dimension output NMOS and PMOS devices are assembled by a plurality of smalldimension octagon cells. Each octagon cell has a concentric and symmetrical layout design including the placement of source contacts and substrate contacts. Experimental results have shown that the driving (sinking) current of per unit layout area of the CMOS output buffer is increased 47.7% (34.3%) by the octagon-type layout, as comparing to the finger-type layout under the same layout spacing d of 5 μ m. The octagontype layout also provides the CMOS output buffer with an increase of 41.5% (84.6%) in the HBM (MM) ESD robustness of per unit layout area, as comparing to the finger-type layout. The CDM ESD pass voltage of per unit layout area of this octagon-type layout is greater than 0.25 V/ μ m². By theoretical calculation, the drain capacitance of an octagon-type output NMOS is only 62.6% of that of the finger-type device, while the spacing d is 5 μ m. The larger spacing d leads to more area saving and smaller drain capacitance in the octagon-type layout.

With theoretical calculation and experimental verification, the large-dimension CMOS output buffers having higher output driving/sinking capability, stronger ESD robustness, but smaller layout area, can be practically achieved by this proposed octagon-type layout design without adding any extra ESD-optimization process. By applying this layout design to both output and input pins of the high-pin-count and padlimited CMOS IC, the chip size can be significantly reduced to save production cost. This proposed octagon-type layout is very suitable for submicron or deep-submicron low-voltage CMOS IC's in high-density and high-speed applications.

APPENDIX

The total layout area of an NMOS transistor in the fingertype layout including double latchup guard rings can be calculated by the following equations. The main design (layout) rules for ESD protection without adding ESD-implant mask in the 0.6-µm CMOS process are summarized in Table IV.

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1. Each finger width for output NMOS and PMOS	$50\mu m \ge w \ge 25\mu m$
2. Output NMOS channel length	0.8µm
3. Output PMOS channel length	$1.5\mu m \ge L \ge 0.8\mu m$
4. Minimum spacing form the drain contact to poly edge	5µm
of output NMOS and PMOS	
5. Minimum spacing form the source contact to poly edge	1µm
of output NMOS and PMOS	

The total layout area of an NMOS transistor in the finger-type layout with double guard rings is

$$\mathbf{A}_{f} = \left[(L+d+S+c) \cdot \frac{W}{w} + 2S_{1} \right] \cdot \left[w + 2(S_{1}+S_{2}) \right]$$
(A.1)

where

- L channel length;
- W total channel width of the transistor;
- w channel width of each poly-gate finger;
- spacing from the drain contact to the poly-gate edge; d
- spacing from the center of source contact to the poly- S^{-} gate edge:
- c the width of a square contact;
- S_1 total spacing of double guard rings; and
- S_2 spacing from the N+ diffusion of the drain to the P+diffusion of the guard ring.

The total number of poly-gate fingers in the whole NMOS layout is W/w = N, where N must be chosen as an integer for uniform layout structure. The total drain area of the finger-type NMOS can be obtained as

$$\mathbf{A}_{Df} = W \cdot \left(d + \frac{c}{2}\right). \tag{A.2}$$

The total perimeter of the drain region (N + diffusion) in the whole finger-type NMOS is

$$\mathbf{P}_{Df} = W + \frac{W}{w} \cdot (2d+c). \tag{A.3}$$

The total drain capacitance is calculated as

$$\mathbf{C}_{Df} = C_J \cdot \mathbf{A}_{Df} + C_{J\text{GATE}} \cdot W + C_{J\text{SW}} \cdot (\mathbf{P}_{Df} - W)$$
(A.4)

where C_{I} and C_{IGATE} have been defined in (3) and C_{ISW} is the sidewall bulk junction capacitance.

The different width of the poly-gate finger leads to a different total layout area of a finger-type NMOS. The minimum layout area of a finger-type NMOS with a specified channel width W can be found by

$$\partial \mathbf{A}_f / \partial N = -2S_1 W / N^2 + 2(L + d + S + c) \cdot (S_1 + S_2)$$
 (A.5)

and

$$\partial \mathbf{A}_f^2 / \partial^2 N = 4S_1 W / N^3. \tag{A.6}$$

Because of $(\partial \mathbf{A}_f^2 / \partial^2 N) > 0$, there is a minimum total layout area when $\partial \mathbf{A}_f / \partial N = 0$. The N to meet this minimum condition is

$$N = \sqrt{\frac{S_1 \cdot W}{(S_1 + S_2) \cdot (L + d + S + c)}}.$$
 (A.7)

N(=W/w) must be chosen as an integer, and the value of w is between 25~50 μ m as specified in the design rules. Putting the suitable N into (A.1), the quasiminimum layout area of a finger-type NMOS transistor can be calculated and used for comparing to the octagon-type layout.

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REFERENCES

- C. Duvvury and A. Amerasekera, "ESD: A pervasive reliability concern for IC technologies," in *Proc. IEEE*, vol. 81, pp. 690–702, May 1993.
- [2] A. Amerasekera and C. Duvvury, "The impact of technology scaling on ESD robustness and protection circuit design," in *Proc. EOS/ESD Symp.*, 1994, vol. EOS-16, pp. 237–245.
- [3] N. C. Li, G. L. Haviland, and A. A. Tuszynski, "CMOS tapered buffer," *IEEE J. Solid-State Circuits*, vol. 25, pp. 1005–1008, Apr. 1990.
 [4] S. R. Vemuru and A. R. Thorbjornsen, "Variable-taper CMOS buffer,"
- [4] S. R. Vemuru and A. R. Thorbjornsen, "Variable-taper CMOS buffer," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1265–1269, Sept. 1991.
- [5] C. Prunty and L. Gal, "Optimum tapered buffer," *IEEE J. Solid-State Circuits*, vol. 27, pp. 118–119, Jan. 1992.
- [6] J.-S. Choi and K. Lee, "Design of CMOS tapered buffer for minimum power-delay product," *IEEE J. Solid-State Circuits*, vol. 29, pp. 1142–1145, Sept. 1994.
- [7] B. S. Cherkauer and E. G. Friedman, "Design of tapered buffers with local interconnect capacitance," *IEEE J. Solid-State Circuits*, vol. 30, pp. 151–155, Feb. 1995.
- [8] _____, "A unified design methodology for CMOS tapered buffers," *IEEE Trans. VLSI Syst.*, vol. 3, pp. 99–111, Jan. 1995.
- [9] L. Baker, R. Currence, S. Law, M. Le, S. T. Lin, and M. Teene, "A waffle layout technique strengthens the ESD hardness of the NMOS output transistor," in *Proc. EOS/ESD Symp.*, 1989, vol. EOS-11, pp. 175–181.
- [10] S. R. Vemuru, "Layout comparison of MOSFET's with large W/L ratios," *Electron. Lett.*, vol. 28, no. 25, pp. 2327–2329, 1992.
- [11] S. Daniel and G. Krieger, "Process and design optimization for advanced CMOS I/O ESD protection devices," in *Proc. EOS/ESD Symp.*, 1990, vol. EOS-12, pp. 206–213.
- [12] A. Amerasekera and C. Duvvury, ESD in Silicon Integrated Circuits. New York: Wiley, 1995.
- [13] C. Duvvury and A. Amerasekera, "State-of-the-art issues for technology and circuit design of ESD protection in CMOS IC's," *Semiconductor Sci. Technol.*, vol. 11, pp. 833–850, 1996.
- [14] D. B. Scott, P. W. Bosshart, and J. D. Gallia, "Circuit to improve electrostatic discharge protection," U.S. Patent 5019888, 1991.
- [15] K. F. Lee, A. Lee, M. L. Marmet, and K. W. Ouyang, "Electro-static discharge protection circuit with bimodal resistance characteristics," U.S. Patent 5 270 565, 1993.
- [16] M.-D. Ker and T.-S. Wu, "Novel octagonal devices structure for output transistors in deep-submicron low-voltage CMOS technology," in *IEDM Tech. Dig.*, 1996, pp. 889–892.
- [17] A. Amerasekera, M. Hannemann, and P. Schofield, "ESD failure modes: characteristics, mechanisms and process influences," *IEEE Trans. Electron Devices*, vol. 39, pp. 430–436, 1992.
- [18] T. L. Polgreen and A. Chatterjee, "Improving the ESD failure threshold of silicided nMOS output transistors by ensuring uniform current flow," *IEEE Trans. Electron Devices*, vol. 39, pp. 379–388, Feb. 1992.
- [19] HSPICE User's Manual–Elements and Models, Meta-Software, CA, vol. 2, 1992.
- [20] M.-D. Ker, C.-Y. Wu, and H.-H. Chang, "Complementary-LVTSCR ESD protection circuit for submicron CMOS VLSI/ULSI," *IEEE Trans. Electron Devices*, vol. 43, pp. 588–598, Apr. 1996.



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