ESD Protection for CMOS Output Buffer by Using Modified LVTSCR Devices with High Trigger Current

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Abstract- Modified designs of the low-voltage triggering semiconductor-controlled rectifier (LVTSCR) devices with high trigger current are proposed to protect the CMOS output buffer against electrostatic discharge (ESD) events in submicrometer CMOS technologies. The high trigger current is achieved by inserting the bypass diodes into the structures of the modified PMOS-trigger lateral SCR (PTLSCR) and NMOS-trigger lateral SCR (NTLSCR) devices. These modified PTLSCR and NTLSCR devices have a lower trigger voltage to effectively protect the output transistors in the ESD-stress conditions, but they also have a higher trigger current to avoid the accidental triggering due to the electrical noise on the output pad in the normal operating conditions of CMOS IC's. Experimental results have verified that the trigger current of the modified PTLSCR (NTLSCR) is increased up to 225.5 mA (218.5 mA). The noise margin to the overshooting (undershooting) voltage pulse on the output pad, without accidentally triggering on the modified NTLSCR (PTLSCR), is more than VDD + 12 V (VSS - 12 V).

Index Terms—ESD, latchup, LVTSCR, noise margin.

I. INTRODUCTION

E LECTROSTATIC discharge (ESD) protection has become a main concern on the reliability of IC products in submicrometer CMOS technologies. Especially, the drains of NMOS and PMOS devices in the CMOS output buffer are often directly connected to the output pad to drive the external load, so the CMOS output buffer is more vulnerable to ESD stress. To improve ESD robustness of a CMOS output buffer and also to drive/sink current to/from the external heavy load, the output NMOS and PMOS devices are often designed with large device dimensions. Even with such large device dimensions, the ESD robustness of the CMOS output buffer had been reported to be seriously degraded by the advanced submicrometer CMOS technologies [1]–[4].

Recently, the lateral semiconductor-controlled rectifier (SCR) device had been used as an ESD-protection element for input protection in submicrometer CMOS IC's [5]–[8]. To effectively protect the CMOS output buffer, the low-voltage triggering SCR (LVTSCR) device has been invented with a much lower trigger voltage [9]–[12]. The trigger voltage of the LVTSCR device is equivalent to the snapback-trigger voltage of the short-channel NMOS (or PMOS) device, which is inserted into the lateral SCR structure, rather than the original switching voltage (about $30\sim50$ V) of the lateral SCR device. To protect the output transistors in the CMOS output buffer, the inserted NMOS (or PMOS) in the LVTSCR should be designed with a shorter channel length than the output NMOS

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(PMOS) in the CMOS output buffer [9]–[12]. But with such a low trigger voltage of the LVTSCR, the corresponding trigger current of the PMOS-trigger lateral SCR (PTLSCR) and NMOS-trigger lateral SCR (NTLSCR) are only about 4.7 mA and 12.3 mA in a $0.6-\mu$ m CMOS technology, respectively [11]. The lower trigger voltage of the PTLSCR and NTLSCR can provide effective ESD protection for the CMOS output buffer, but the lower trigger current may cause the PTLSCR and NTLSCR to be accidentally triggered on by the external overshooting or undershooting noise pulses on the output pin while the CMOS IC is in its normal operating condition.

In this paper, a modified PTLSCR and a modified NTLSCR with lower trigger voltage but higher trigger current are proposed to safely protect the CMOS output buffer without being accidentally triggered on by the electrical noisy pulse when the CMOS IC's are in the normal operating conditions.

> II. MODIFIED PTLSCR/NTLSCR Devices with High Trigger Current

A. Modified Device Designs

The schematic cross-sectional views of the modified PTLSCR and NTLSCR in a P-substrate N-well CMOS process are shown in Fig. 1(a) and (b), respectively. The modified PTLSCR is formed by inserting a bypass diode Dn2 into the PTLSCR structure as shown in Fig. 1(a). The modified NTLSCR is formed by inserting a bypass diode Dp2 into the NTLSCR structure as shown in Fig. 1(b). The Dn2 (Dp2) is located into the latching path of the PTLSCR (NTLSCR). This Dn2 (Dp2) has an effect of reducing the equivalent substrate resistor Rsub1 (N-well resistor Rw2) and an effect of bypassing the latchup trigger current in the P-substrate (the N-well), so the trigger current to initiate the positive-feedback regenerative process of latchup in the PTLSCR (NTLSCR) can be significantly increased [13]–[14]. So, by adding this bypass diode Dn2 (Dp2), the trigger current of the modified PTLSCR (modified NTLSCR) can be significantly increased to avoid the accidental triggering by the external noisy pulse. The trigger voltage of this modified PTLSCR (modified NTLSCR) is still kept the same as the snapback-trigger voltage of the shortchannel PMOS (NMOS) which is inserted in the PTLSCR (NTLSCR) structure [11]. This modified PTLSCR (modified NTLSCR) can be merged with the output PMOS (NMOS) in the layout to save layout area as shown in Fig. 1(a) and (b).

Since ESD voltages may have positive or negative polarities on a pin to either the VDD or the VSS pins, there are four different ESD-stress conditions on an output pin. The four ESD-stress conditions on a pin have been specified as PS, NS, PD, and ND modes in [12]. In the CMOS output buffers, there also exist two parasitic junction diodes, Dp1

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Fig. 1. Schematic cross-sectional views of (a) the output PMOS and the modified PTLSCR device, and (b) the output NMOS and the modified NTLSCR device, in a P-substrate N-well CMOS process.

and Dn1, in the p-n junctions between the drain and bulk of the output PMOS and NMOS. The Dp1 (Dn1) is forward biased in the PD-mode (NS-mode) ESD-stress condition. The diode in its forward-biased condition can sustain high ESD voltage. So, the CMOS output buffer often has a much higher ESD robustness in the PD-mode and NS-mode ESD stresses than it does in the PS-mode and ND-mode ESD stresses. The modified PTLSCR and NTLSCR are therefore used to improve the ESD robustness of the CMOS output buffer in the PS-mode and ND-mode ESD stresses.

By increasing the trigger current of the modified PTLSCR and NTLSCR but without increasing their trigger voltage, these modified PTLSCR and NTLSCR can still provide excellent ESD protection to the CMOS output buffer. With the higher trigger current of the modified PTLSCR and NTLSCR, as well as the voltage-clamping effect of the forward-biased diodes Dp1 and Dn1, the modified PTLSCR and NTLSCR can be guaranteed to be off while the CMOS IC is in its normal operating conditions even if there are the overshooting or undershooting noisy pulses on the output pin.

B. Operating Principles

1) CMOS Normal-Operating Conditions: In CMOS normal operations, the VDD is biased at 3 V for low-voltage application and the VSS is grounded. Under this condition, the modified PTLSCR and NTLSCR are kept off due to the gates of the inserted short-channel PMOS and NMOS being connected to their sources. The CMOS output buffer is controlled by the prebuffer circuits to drive/sink current to/from the external output load.

The diodes Dp1 and Dn1 contribute a voltage-level clamping effect on the output pad. The Dp1 (Dn1) clamps the high-level (low-level) voltage of the output signal to about VDD + 0.6 V (VSS – 0.6 V). Thus, the voltage level of output signals on the output pad is clamped between about 3.6 V and -0.6 V in the normal CMOS operations with 3-V VDD and 0-V VSS. If an unexpected noisy pulse happens to the output pad, the overshooting or undershooting voltage/current can be bypassed by the diodes Dp1 and Dn1. The modified PTLSCR and NTLSCR with higher trigger current have enough noise margin, so the modified PTLSCR and NTLSCR are not triggered on by the external noisy pulse under the clamping guard of diodes Dp1 and Dn1.

2) ESD-Stress Conditions: When a PS-mode (ND-mode) ESD event occurs at the output pad with the relatively grounded VSS (VDD) pin, the positive (negative) ESD voltage is diverted to the anode (cathode) of the modified NTLSCR (PTLSCR), and then to the drain of the inserted short-channel NMOS (PMOS). As the drain voltage is high (low) enough, the inserted short-channel NMOS (PMOS) is first turned on by means of drain snapback breakdown and leads to the selfregeneration of latchup in the modified NTLSCR (PTLSCR). Once latchup happens in the modified NTLSCR (PTLSCR), a path with very low impedance from the output pad to VSS (VDD) is created. Then, the ESD current is mainly discharged through the lateral SCR structure in the modified NTLSCR (PTLSCR). The positive (negative) ESD voltage on the output pad is clamped to near the holding voltage about $1 \sim 2$ V $(-1 \sim -2 \text{ V})$ of the modified NTLSCR (PTLSCR), so the output transistors can be effectively protected by the modified NTLSCR (PTLSCR).

In the NS-mode (PD-mode) ESD event, the parasitic diode Dn1 (Dp1) in the output NMOS (PMOS) is forward turned on to bypass ESD current. The negative (positive) ESD voltage on the pad is clamped by the forward-biased Dn1 (Dp1) to about -0.6 V (+0.6 V). The diodes Dn1 and Dp1 in the forward-biased condition can perform high ESD protection for the output transistors.

III. EXPERIMENTAL RESULTS

A. Device I-V Characteristics

1) The Modified NTLSCR: One set of testkeys fabricated by a 0.6- μ m CMOS technology with LDD and polycide processes is measured and tested. The I-V characteristics of the modified NTLSCR and the output NMOS in the CMOS output buffer are independently measured by a TEKTRONIX Curve Tracers 370 A. The snapback I-V curve of the output NMOS with a channel length of 1.0 μ m is shown in Fig. 2(a). The snapback trigger voltage (current) of the output NMOS is 13.7 V (4.76 mA) and the snapback holding voltage (current) is 9.78 V (5.42 mA). The I-V curve of the modified NTLSCR is shown in Fig. 2(b). The channel length of the NMOS inserted into the modified NTLSCR is 0.8 μ m. The modified NTLSCR has two trigger points in its I-V characteristics. The first trigger point is due to the drain snapback breakdown of the inserted NMOS. The first trigger voltage (current) is 11.6 V (2.0 mA). Due to the presence of the bypass diode Dp2, there is a buffer region in the I-V characteristics [marked as "A" in Fig. 2(b)] before the lateral SCR in the modified NTLSCR is triggered on. This region A is the snapback region of the





(a)

(b)

Fig. 2. The snapback I–V characteristics of (a) the output NMOS device and (b) the modified NTLSCR device.

inserted NMOS. As the applied current is still increased, the lateral SCR in the modified NTLSCR will be finally triggered on. So, there is the second trigger point in the I–V curve of Fig. 2(b). The measured second trigger current (voltage) in the modified NTLSCR is as high as 218.5 mA (9.06 V). After the second trigger point, the I–V curve enters into the latchup holding region [marked as "B" in Fig. 2(b)], which is due to the latching action of the lateral SCR structure in the modified NTLSCR. The minimum holding voltage (current) of region B is as low as 1.34 V (12.5 mA). In the region A, the modified NTLSCR can be safely operated in this snapback region without causing any damage. With this buffer region A, the modified NTLSCR is not triggered on by the external noisy pulse, but it can be triggered on by the ESD pulse.

Comparing the I–V curves between Fig. 2(a) and (b), it can be guaranteed that the modified NTLSCR (with the first trigger voltage of 11.6 V) can be turned on before the output NMOS breaks down (with a breakdown voltage of 13.7 V) under the PS-mode ESD-stress condition. Thus, the modified NTLSCR can effectively protect the output NMOS against ESD damage. The holding voltage of the modified NTLSCR is still as low as that of an NTLSCR, but the trigger current (218.5 mA) of the modified NTLSCR is much higher than that (12.3 mA) of the NTLSCR [11].

2) The Modified PTLSCR: The turn-on characteristics of the modified PTLSCR and the output PMOS are also measured and compared. The snapback I-V curve of the output PMOS with a channel length of 1.0 μ m is shown in Fig. 3(a). The snapback trigger voltage (current) of the output PMOS is -15.62 V (-15.85 mA) and the snapback holding voltage (current) is -13.84 V (-13.9 mA). The I-V curve of the modified PTLSCR is shown in Fig. 3(b). The channel length of the PMOS inserted into the modified PTLSCR is 0.8 μ m. The modified PTLSCR also has two trigger points in its I-V characteristics. The first trigger point is due to the drain snapback breakdown of the inserted PMOS. The first trigger voltage (current) is -13.42 V (-15 mA). Due to the presence of the bypass diode Dn2, there is a buffer region in the I-V characteristics [marked as "C" in Fig. 3(b)] before the lateral SCR in the modified PTLSCR is triggered on. The presence of this region C is owing to the bypass diode Dn2 and the inserted PMOS in the device structure of the modified PTLSCR. As the applied negative current is still increased, the lateral SCR in the modified PTLSCR can be finally triggered on and cause a second trigger point in the I-V curve of Fig. 3(b). The second trigger current (voltage) in the modified PTLSCR is as high as -225.5 mA (-6.14 V). After the second trigger point, the I-V curve enters into the latchup holding region [marked as "D" in Fig. 3(b)], which is due to the latching action of the lateral SCR structure in the modified PTLSCR. The minimum holding voltage (current) in the region D is as low as -1.72 V (-13.5 mA).

In the region C of Fig. 3(b), the modified PTLSCR can be safely operated in this snapback region without causing any damage. With this buffer region C, the modified PTLSCR is not triggered on by the external noisy pulse, but it can be triggered on by the ESD pulse. Comparing the I–V curves between Fig. 3(a) and (b), it is guaranteed that the modified PTLSCR (with the first trigger voltage of -13.42 V) can be turned on before the output PMOS breaks down (with a breakdown voltage of -15.62 V) under the ND-mode ESD-stress condition. Thus, the modified PTLSCR can effectively protect the output PMOS against ESD damage. The holding voltage of the modified PTLSCR is still as low as that of an PTLSCR, but the trigger current (-225.5 mA) of the modified PTLSCR [11].

B. Noise Margin

To investigate the efficiency of the bypass diode Dp2 in the modified NTLSCR, a positive voltage pulse with a low-level voltage of 3 V generated from a pulse generator is used to simulate an overshooting noise on the output pad while the IC is in its normal operating condition with the power supply of 3-V VDD and 0-V VSS. The output NMOS is kept off







Fig. 3. The snapback I-V characteristics of (a) the output PMOS device and (b) the modified PTLSCR device.

but the output PMOS is on by its gate grounded to provide a 3-V voltage to the output pad. An overshooting voltage pulse generated from a pulse generator (HP8116A), which has a lowlevel voltage of 3 V and a high-level voltage of up to 15 V with a pulse width of 250 μ S, is applied to the output pad. The 15-V high-level voltage is clamped to about only 3.5 V by the diode Dp1. After the triggering of the 15-V overshooting voltage pulse on the output pad, the voltage waveform on the output pad is still kept at 3 V without any degradation. So, the modified NTLSCR still remains off.

Similarly, to investigate the efficiency of the bypass diode Dn2 in the modified PTLSCR, an undershooting voltage pulse with a high-level voltage of 0 V and a negative low-level voltage is applied to the output pad, while the output PMOS is off but the output NMOS is on to provide a 0-V voltage to the output pad. An undershooting voltage pulse generated from the pulse generator with the undershooting low-level voltage of -12 V is applied to the output pad. The low-level voltage of -12 V in the undershooting voltage pulse is clamped by the diode Dn1 to only about -0.72 V. After the transition of the undershooting voltage pulse, the voltage on the output pad

remains at 0 V. So, the modified PTLSCR is not triggered on by the applied -12 V undershooting voltage pulse.

Through above verification, this proposed output ESD protection circuit with the modified PTLSCR and NTLSCR has a noise margin more (less) than VDD + 12 V (VSS - 12 V)to avoid the accidental triggering due to the overshooting or undershooting voltage pulses on the output pad.

IV. CONCLUSION

An area-efficient output ESD protection design by using the modified PTLSCR and NTLSCR devices has been practically verified in a $0.6-\mu m$ CMOS process. The accidental triggering on the LVTSCR device, due to the overshooting or undershooting noise pulses on the output pad, has been successfully overcome by increasing the trigger current of the modified LVTSCR devices. With the high trigger current, these modified PTLSCR and NTLSCR devices have been experimentally confirmed with a noise margin more than ± 12 V against the accidental triggering due to the overshooting/undershooting noise pulses on the output pad in the normal operating conditions. Because of still remaining a lower trigger voltage, the modified PTLSCR and NTLSCR can be triggered on before the output transistors break down in the ESD-stress conditions. These modified PTLSCR and NTLSCR can effectively provide the CMOS output buffer with a 4000-V human-body model (HBM) ESD robustness in a small layout area of only $60 \times 37.6 \ \mu m^2$.

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