Briefs

ESD Protection for Output Pad with Well-Coupled Field-Oxide Device in 0.5-μm CMOS Technology

Chau-Neng Wu and Ming-Dou Ker

***Abstract*—A well-coupled field-oxide device (WCFOD) is first proposed to effectively improve Electrostatic Discharge (ESD) robustness of the output pad in a 0.5-μm CMOS process. ESD-transient voltage is coupled to the bulk of field-oxide device through a parasitic capacitor to trigger on the lateral bipolar action of the field-oxide device. This WCFOD has been practically implemented in a 256-K high-speed SRAM product to sustain HBM ESD stress up to 6500 V.**

I. Introduction

Electrostatic Discharge (ESD) robustness of CMOS IC's was reported to be much degraded by submicron or deep-submicron CMOS technologies [1], [2]. Especially, the drains of output transistors are often directly connected to the pad, so the output transistors are more sensitive to ESD stress. An output buffer with enough driving/sinking capability, higher ESD reliability, but smaller layout area is required by CMOS IC's in submicron CMOS technologies. Therefore, it is necessary to improve ESD protection for output pad through either process modification [3]–[5] or using extra ESD-protection elements [6]–[9]. In [10], a substrate-triggering technique was used to improve ESD performance of deep submicron CMOS processes.

In [6]–[9], an n-type field-oxide device (or lateral n-p-n bipolar junction transistor) was placed in parallel with the thin-oxide output NMOS from the output pad to VSS to improve ESD robustness of output buffer. But since the snapback-breakdown voltage of n-type field-oxide device is generally higher than that of short-channel output NMOS in submicron CMOS technology, the output NMOS could be damaged before the field-oxide device is turned on. If the turn-on voltage of the field-oxide device can be lowered below the breakdown voltage of output transistor, the field-oxide device can provide excellent ESD protection for output pad with a smaller layout area.

In this paper, a well-coupling technique is proposed to reduce the turn-on voltage of field-oxide device. With lower turn-on voltage, this well-coupled field-oxide device (WCFOD) can offer excellent ESD protection for output pad alone without any series resistor between the output transistor and the output pad.

II. WCFOD for Output ESD Protection

The proposed ESD protection with WCFOD for output buffer is shown in Fig. 1, and the corresponding schematic cross-sectional view of this WCFOD is shown in Fig. 2. In Fig. 2, the field-oxide device is formed by the N^+ diffusions which are close together in a separated P-well. This separated P-well is connected to VSS through a resistor R_p. A capacitor C_p is connected from the output pad to the separated P-well to perform the well-coupling action under the ESD stress. The output buffer includes a pull-up NMOS, MN1, and a pull-down NMOS, MN2. A resistor R_1 of 30 Ω connected between the drain of MN1 and VDD is used to limit the short-circuit transient current during logic transition.

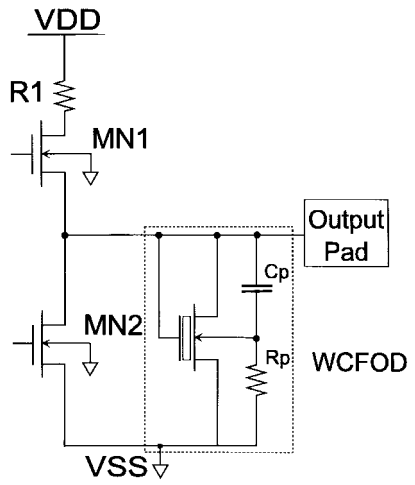

Fig. 1. Output ESD protection with the proposed WCFOD.

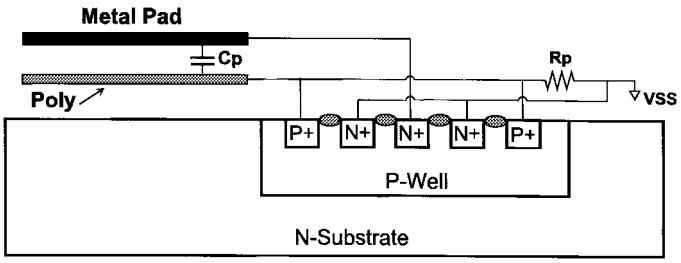

Fig. 2. Schematic cross-sectional view of the WCFOD structure.

There are four different modes of ESD stresses on a pin of an IC [11]. The PS-mode ESD stress, which has a positive ESD voltage on the pad with relatively grounded VSS but floating VDD, has been found to be the worst case of ESD stress on the output buffer due to the snapback breakdown of output NMOS with LDD structure. The PS-mode ESD failure voltage of output buffer in Fig. 1 without WCFOD is only around 1 KV in HBM (human-body model) ESD testing, but its NS-mode ESD failure voltage can go above 8 KV. The ESD failure threshold of a output pad is defined as the lowest ESD failure voltage of the four modes of ESD stresses, so the most important work of ESD protection for such an output pad is to improve the PS-mode ESD failure voltage.

Under PS-mode ESD stress, positive ESD-transient voltage is coupled to the separated P-well through the capacitor C_p. This coupled positive ESD-transient voltage in the separated P-well is sustained longer in time by R_p. Due to the positive voltage in the separated P-well, the bulk-to-source junction in the field-oxide device is forward biased. This leads to an earlier lateral bipolar action in the field-oxide device with much lower breakdown voltage. Thus, the WCFOD can be fully turned on to bypass ESD current before output

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C.-N. Wu is with the Winbond Electronics Corporation, Science-Based Industrial Park, Hsinchu 300, Taiwan, R.O.C.

M.-D. Ker is with the Integrated Circuits & Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

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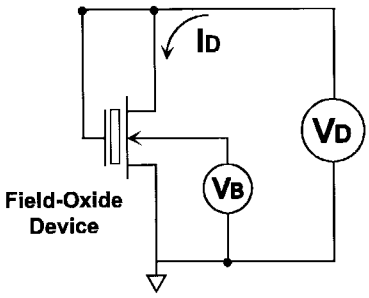
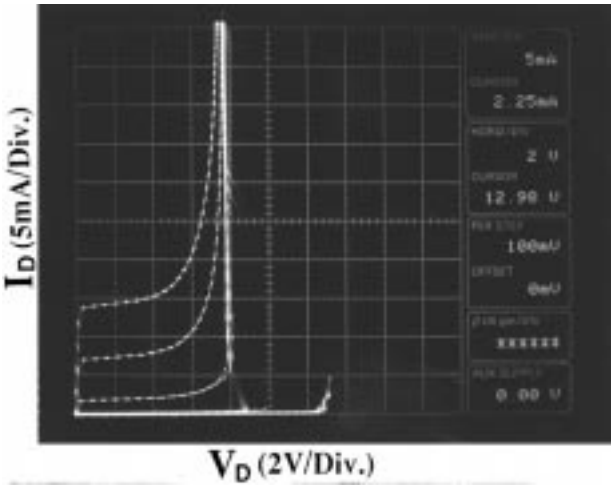


(a)



(b)

Fig. 3. (a) An experimental setup to measure the snapback-breakdown characteristics of a field-oxide device under different P-well biases. (b) The measured I–V curves of a field-oxide device with different P-well biases.

transistor is damaged. So, the output transistor can be effectively protected by the WCFOD.

The capacitor C_p in the WCFOD can be realized by inserting the poly layer right under the wire-bonding metal pad, as shown in Fig. 2, without increasing the output pad area. This layout of the coupling capacitor had been successfully verified in an input ESD protection circuit [12], [13]. The sustaining resistor R_p can be realized by a poly line around the output pad without increasing total layout area of the chip. C_p and R_p are designed to keep the WCFOD off in normal operating condition of IC with 5-V VDD and 0-V VSS bias, but to turn on the WCFOD in the PS-mode ESD-stress condition. Because the voltage level and the rise time between the normal output signal and the ESD pulse are quite different, the C_p and R_p can be easily selected.

III. Experimental Results

An SRAM IC was used to verify ESD-protection efficiency of this design in a 5-V 0.5-μm n-substrate/twin-well CMOS process with LDD structure. The WCFOD is realized in a strip-line-type layout with device dimension (width/length) of 173/0.9 (μm). A square-shape poly layer of 88 $\times$ 88 μm^2 is placed right under the metal pad to constitute the coupling capacitor C_p of 0.86 pF. A poly line with 400-μm length is drawn from the square-shape poly layer and surrounds the output pad to form the resistor R_p of about 24 KΩ. A single WCFOD device is also fabricated in the same wafer to find its device characteristics.

A. Device Characteristics of WCFOD

Fig. 3(a) shows the setup to measure the breakdown characteristics of field-oxide device with different P-well bias. The bulk (P-well) of the field-oxide device is biased with different voltages and the measured results are shown in Fig. 3(b). As the P-well bias is increased above 0.6 V, the snapback-trigger voltage is significantly reduced. If the P-well bias is increased above 0.8 V, the lateral bipolar action in the field-oxide device is first initiated when its drain bias is in the low voltage region. As the drain bias increases higher, the turned-on field-oxide device finally enters its snapback region. As the bias voltage is up to 0.8 V, the snapback-trigger voltage is lowed to only about 8 V. With such a low snapback-trigger voltage, the field-oxide device can become an effective ESD-protection device to protect the output pad.

B. ESD Testing Results

The 256-K high-speed SRAM IC with ESD protection of WCFOD was tested by ESD simulator in the human-body model (HBM) to investigate the efficiency of ESD protection. The ESD failure criterion is defined as the leakage current of the output pad with output buffer and ESD protection circuit in its high-impedance state being above 1 μA under VDD (VSS) bias of 6 V (0 V). The high-impedance state of each output pin can be controlled by a chip-selected pin of the 256-K high-speed SRAM IC.

The PS-mode ESD failure voltage of output buffer with this WCFOD is improved up to 6.5 KV in the SRAM test chip. The ESD failure voltage of the original output buffer without WCFOD is only 1 KV. Because the ESD-transient voltage is coupled to the P-well of the field-oxide device to trigger the lateral bipolar action, the WCFOD can be turned on with lower snapback-trigger voltage to bypass ESD current from the output pad to VSS. This verifies the excellent performance of WCFOD for output ESD protection.

C. Well-Coupling Efficiency

To verify the efficiency of well-coupling technique for output ESD protection with WCFOD, a voltage pulse generated from HP8116A with a pulse width of 400 nS is applied to the output pin of the test chip under a bias of 5-V VDD and 0-V VSS. An oscilloscope is used to monitor the voltage waveform on the pin. The chip-select pin is used to turn the output transistors off. If the output ESD protection circuit is not triggered on by the applied voltage pulse, the voltage waveform is not degraded on the pin. If enough transient voltage is coupled through the C_p to the P-well of WCFOD due to the rising edge of the applied pulse, the voltage waveform will be degraded by the turned-on WCFOD.

When the voltage peak of the applied voltage pulse is increased up to 7.1 V, the WCFOD is still not triggered on. So, there is no degradation on the pulse-type voltage waveform. If the voltage peak is increased beyond 7.1 V, the WCFOD can be triggered on and the voltage waveform on the pin is degraded. With practical verification, the WCFOD is not triggered on by the normal 5-V input/output signals. But, the pulse-type trigger voltage of the proposed WCFOD is lowered to only 7.1 V. Thus, the ESD voltage can be bypassed by the early turn-on of the WCFOD to effectively protect the output transistors. This verifies the excellent efficiency of the proposed well-coupling technique.

IV. Conclusion

A new ESD protection technique for output pad with well-coupled field-oxide device has been successfully verified and practically applied in a 0.5-μm 256-K high-speed SRAM product. This WCFOD has the benefits of lower snapback-trigger voltage and higher ESD protection capability, without adding series resistor into the drain of output NMOS transistor. The ESD reliability of output pad can be

effectively improved without causing any degradation in the circuit performance of the high-speed SRAM IC.

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High Field Stressing Effects on the Split N_2O Grown Thin Gate Dielectric by Rapid Thermal Processing

P. V. S. Subrahmanyam, A. Prabhakar, and J. Vasi

***Abstract*—Highly reliable thin oxynitride layers of very good Si/SiO_2 interface endurance were grown on silicon wafers with a split N_2O cycle ($N_2O/O_2/N_2O$) employing Rapid Thermal Processing (RTP). Excellent electrical characteristics with reduced positive charge generation, electron trapping and/or interface state generation were achieved under high field stressing compared to pure N_2O dielectric.**

I. INTRODUCTION

There is definite necessity to understand and address the reliability issue of gate oxide in thin regime due to the increased possibility of degradation and to improve its quality [1].

Nitridation of pre-grown SiO_2 resulting in oxynitride layers was observed to improve the quality and hence the reliability in thin regime [2]–[7]. Oxynitride layers grown on silicon by direct exposure to N_2O at elevated temperature also appear to be promising candidates as gate dielectrics [9]. But, the grown oxynitride layers suffer from uneven Si/SiO_2 interface resulting in the modification of breakdown voltage [5], [8], [10]. Hence, it is necessary to have a oxynitride growth process capable of providing defect free Si/SiO_2 interface and improved electrical characteristics.

During the current investigation we found that oxynitride layers with very good Si/SiO_2 interface and improved electrical performance can be grown on silicon with a split N_2O process. In this process, we divide the time needed to grow a dielectric of desired thickness in pure N_2O ambient into approximately two halves and introduce a short-duration reduced-temperature dry oxygen step.

The advantage of the split N_2O cycle is that there is no need to grow an initial oxide prior to N_2O exposure to obtain a defect free dielectric layer as already reported [5], [9], [11].

II. EXPERIMENTAL PROCEDURE

A. Sample Fabrication

MOS capacitors with n^+ doped polysilicon gate were fabricated on n $\langle 100 \rangle$, phosphorus doped, 4-in silicon wafers. The thin oxide layers were grown in electronic grade N_2O, using a Model 610 RTP furnace procured from M/S AG Associates. The wafers, prior to oxidation, were cleaned in piranha ($H_2SO_4 : H_2O_2 :: 5 : 1$) for about 10 min, followed by a thorough DI water rinse. The wafers received a Buffered Oxide Etch (BOE) just before loading into the RTP chamber in N_2O ambient. The pure N_2O and split N_2O cycles employed for oxidation are shown in Fig. 1, and the numerical values are presented in Table I. Polysilicon was deposited in a conventional LPCVD system and doped with phosphorus in a standard furnace. High pure Aluminum was used for contacts. The gate geometries with an area of 0.385 mm^2 were defined by standard optical lithography.

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P. V. S. Subrahmanyam is with ITI Ltd., Bangalore, India 560 016.

A. Prabhakar was with ITI Ltd. Bangalore, India 560 016. He is now with Datanet Corporation, Bangalore, India 560 016.

J. Vasi is with the Department of Electrical Engineering, Indian Institute of Technology, Powai, Bombay, India 400 076.

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