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ELECTROSTATIC DISCHARGE (ESD) PROTECTION FOR CMOS OUTPUT BUFFERS IN SCALED-DOWN VLSI TECHNOLOGY

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Abstract—To provide area-efficient output ESD protection for the scaled-down CMOS VLSI, a new output ESD protection is proposed. In the new output ESD protection circuit, there are two novel devices, the PTLSCR (PMOS-trigger lateral SCR) and the NTLSCR (NMOS-trigger lateral SCR). The PTLSCR is in parallel and merged with the output PMOS, and the NTLSCR (is in parallel and merged with the output PMOS, and the NTLSCR is in parallel and merged with the output PMOS, and the NTLSCR is in parallel and merged with the output PMOS, and the NTLSCR is in parallel and merged with the output PMOS, and the NTLSCR is in parallel and merged with the output NMOS, to provide area-efficient ESD protection for CMOS output buffers. The trigger voltages of PTLSCR and NTLSCR are lowered below the breakdown voltages of the output PMOS and NMOS in the CMOS output buffer. The PTLSCR and NTLSCR are guaranteed to be turned on first before the output PMOS or NMOS are broken down by the ESD voltage. Experimental results have shown that the PTLSCR and NTLSCR can sustain over 4000 V (700 V) of the human-body-model (machine-model) ESD stresses within a very small layout area in a 0.6 μ m CMOS technology with LDD and polycide processes. The noise margin of the proposed output ESD protection design is greater than 8 V (lower than -3.3 V) to avoid the undesired triggering on the NTLSCR (PTLSCR) due to the overshooting (undershooting) voltage pulse on the output pad when the IC is under normal operating conditions with 5 V VDD and 0 V VSS power supplies. © 1998 Elsevier Science Ltd. All rights reserved.

1. INTRODUCTION

One of the most negative impacts from the scaleddown CMOS VLSI technologies with shrinking device dimensions is the ESD (electrostatic discharge) issue. ESD protection has become one of main reliability concerns of scaled-down VLSI products. The voltage peak of an ESD event happening to the pin of an IC product could be as high as several thousand volts, or even up to several tens of thousands of volts. So it is necessary to make effective on-chip ESD protection circuits around each input and output pads of IC products; in particular, the drains of output NMOS and PMOS devices in the CMOS output buffer are often directly connected to the output pad to drive external load. This often leads to a low ESD level of the output buffer in the scaled-down CMOS technologies. To improve the ESD reliability of the CMOS output buffer and also to drive/sink currents to/from external heavy loads, the NMOS and PMOS in CMOS output buffers are generally designed with large device dimensions. Typically, in low-voltage applications (VDD = 3.3 V, 2.5 V, ...), the CMOS output buffer will be designed with much larger device dimensions to perform enough driving/sinking capability. Even with much large device dimensions, the ESD robustness of a CMOS output buffer has been reported to be seriously degraded by scaled-down CMOS VLSI technologies [1-4]. The advanced process technologies, such as thinner gate oxide, shorter channel length, shallower source/drain junction, LDD (lightly-doped drain) structure, and silicided diffusion, greatly degrade the ESD robustness of submicron CMOS VLSI.

In CMOS IC products, the ESD level of an IC is defined as the lowest ESD-sustained voltage of all the input and output pins. For example, the HBM (human-body model) ESD level of the input pins of a CMOS IC may be in the range of about 3-4 kV due to the input pins often having a series resistor to limit the ESD current. However, the HBM ESD level of the output pins is almost in the range of 1-2 kV if there is no extra ESD protection design added to the output buffer in the advanced CMOS processes. This leads to the overall ESD level of the IC product to be only 1-2 kV. The ESD robustness of CMOS output buffers has become the most important ESD reliability concern of IC products.

From another practical viewpoint of the highntegration CMOS VLSI/ULSI, the pin counts can be often more than 200. In such high-pin-count CMOS ICs, the pad pitch is reduced to around 100 μ m only. The layout area available for each output (or input) pad with the output buffer (or ESD protection circuit) including latchup guard rings is seriously limited to reduce chip size of the pad-limited VLSI products. Thus, a CMOS output buffer with enough driving/sinking capability, a higher ESD reliability, but a smaller layout area is much craved by the scaled-down CMOS VLSI/ULSI.

To improve the ESD robustness of scaled-down CMOS ICs, the lateral SCR device has been used as an ESD-protection element for input protection [5-8]. The lateral SCR device was found to produce the highest ESD protection capability in the smallest layout area as compared with other ESD protection elements such as the diode, thick-oxide device, gate-oxide device, and parasitic bipolar device in submicron CMOS ICs [9]. In this paper, an overview of output ESD protection for scaleddown CMOS technologies by using the nonconventional devices is presented in Section 2. In Section 3, a new ESD protection circuit for CMOS output buffers by using the PTLSCR and NTLSCR devices is proposed with the advantages of smallest layout area and highest ESD reliability [10]. Experimental verification of this new ESD protection circuit for CMOS output buffer in an advanced 0.6 µm CMOS technology is demonstrated in Section 4. Finally, a conclusion is drawn in Section 5.

2. OVERVIEW OF PREVIOUS WORKS ON OUTPUT ESD PROTECTION

2.1. ESD-implant process

The LDD structure of CMOS devices had become a standard process to overcome the issue of hot-carrier reliability in submicron CMOS technologies [11, 12]. However, this LDD structure causes serious degradation on ESD robustness of CMOS output buffer [2-4, 13]. To improve the ESD robustness of CMOS output buffer, some submicron CMOS technologies offer an additional "ESD implant" mask into the process flow to make a stronger device structure for output buffers or input ESD protection circuits [14-18]. The ESD-implant process produces a heavy-doping drain and source with a deeper junction depth for the output devices. The LDD structure in the ESD-implant device can become absent due to the lateral diffusion of the heavy-doping drain and source, or due to the ESD implantation before the formulation of the side-wall spacer around the gate oxide. The schematic crosssectional views of the NMOS devices with LDD structure and ESD-implant structure are shown in Fig. 1. Because of the lateral-diffusion effect in the heavy-doping drain and source regions, the channel length of the ESD-implant output devices has to be enlarged more than the original design. For example, the minimum channel length of the output NMOS device without the ESD-implant process in a $0.6 \,\mu m$ CMOS technology is specified by the design rules to be $0.8 \,\mu\text{m}$. However, if the output NMOS device is fabricated with the additional ESD-implant process in the same 0.6 µm CMOS



Fig. 1. Schematic cross-sectional view of thin-oxide NMOS device in: (a) an LDD structure; and (b) an ESD-implant structure.

technology, its channel length has to be longer than $1.2 \,\mu\text{m}$. Therefore, the ESD-implant output NMOS device has the device structure similar to that of the early long-channel CMOS technologies. Thus, it can provide better ESD robustness for submicron CMOS ICs. A typical experimental result about the improvement of ESD-implant process on ESD robustness of the output NMOS device has been reported in Ref. [14].

Using the ESD-implant process, the ESD reliability of the output buffer can be effectively improved, but the cost of IC fabrication is also increased by the additional mask and process steps. Besides, with the ESD-implant process, the channel length of output device has to be enlarged from 0.8 to $1.2 \,\mu\text{m}$ in the $0.6 \,\mu\text{m}$ CMOS technology. The device dimensions of a CMOS output buffer with the ESD-implant process have to be re-designed with one set of ESD-implant SPICE parameters to calculate the driving/sinking capability. For example, the output NMOS device with a device dimension of $W/L = 300/0.8 \ (\mu m/\mu m)$ in the 0.6 μm CMOS technology without the ESD-implant process can sink current of 119 mA from the output pad under the bias conditions of $V_{gs} = 5 \text{ V}$ and $V_{\rm ds} = 5$ V. If the output NMOS device is fabricated with the ESD-implant process in the same $0.6 \,\mu m$ CMOS technology, its device dimension (W/L) has to be enlarged to 313/1.2 in order to provide the same sinking current for the output buffer. Thus, the layout area of the output buffer with the ESD-implant process is also increased. Moreover,

620

additional testing devices for the extraction of ESDimplant SPICE parameters have to be included in the development of ESD-implant process. All of these extra efforts increase the cost and complexity to fabricate CMOS ICs in scaled-down CMOS technology with the ESD-implant process.

2.2. Additional ESD-protection devices

In some works [19-26], extra ESD-protection elements have been added to the output pad to improve ESD robustness of the output buffer. In Ref. [19], an N-well field-oxide device is placed in parallel with the thin-oxide NMOS device of output buffer from the output pad to VSS to improve the ESD robustness of the output buffer. But the punch-through voltage of an N-well field-oxide device is generally higher than that of the shortchannel thin-oxide NMOS device in scaled-down CMOS technologies and the output NMOS could first be damaged before the N-well field-oxide device is turned on when the ESD stress occurs on the output pad. Thus, the improvement of ESD protection by only adding such an N-well fieldoxide device may be inefficient.

In Ref. [20], a lateral *n-p-n* transistor (like a field-oxide device) is placed in parallel with the output NMOS to improve ESD robustness of the CMOS output buffer. In order to turn on the lateral *n-p-n* transistor before the snapback breakdown of the thin-oxide output NMOS under ESD-stress conditions, the P^+ diffusion for the Psubstrate bias is placed away from the lateral n-p-ntransistor to enhance the bipolar action of the lateral *n*-*p*-*n* transistor. Besides, some P^+ diffusion connected to ground is also placed into the source region of the output NMOS to eliminate the parasitic bipolar snapback action in the thin-oxide output NMOS device. The voltage difference of snapback breakdown between the lateral n-p-n transistor and the short-channel thin-oxide output NMOS device in scaled-down CMOS technology may be a little, so the output NMOS is still sensitive to ESD stress.

In Ref. [21], the CMOS output buffer is connected to the output pad by means of a series resistor and two ESD-protection diodes are disposed around the output pad. This series resistor can prevent ESD damages on the CMOS output buffer before the ESD current is bypassed by the diodes. In Ref. [22], a lateral n-p-n bipolar transistor is placed in parallel with the output NMOS and a series polysilicon resistor is connected between the output pad and the output buffer to improve the ESD reliability of the output buffer. The lateral n-p*n* bipolar transistor can perform effective ESD protection only if it can be turned on before the thinoxide output NMOS is broken down by the ESD voltage. In Ref. [23], the large-dimension output NMOS is separated as several small-dimension NMOS devices in parallel with each other from the output pad to ground. There is an extra series resistor inserted into the drain of each smalldimension NMOS device to improve its ESD robustness. In particular, the series resistor is formed by the N-well structure, which is merged into the drain structure of the output NMOS. In Ref. [24], a thick-oxide snapback device (field-oxide device) is placed in parallel with the output NMOS, and the drain of the output NMOS is modified with a series N-well resistor as that in Ref. [23] to improve the ESD reliability of the CMOS output buffer. In Refs [21-24], there are series resistors placed between the output buffer and the output pad. These series resistors can effectively limit the ESD-stress current toward the CMOS output buffer, but they also limit the driving/sinking current of the CMOS output buffer. The timing for output signal is also delayed by these series resistors. Thus, the output driving/sinking capability and output timing may become out of the original design specifications. To perform enough driving/sinking capability, the device dimensions of the CMOS output buffer have to be enlarged. The CMOS output buffer with enlarged device dimension and additional ESD-protection elements will occupy more layout area. This limits the applications of Refs [21-24] in high-speed (minimum delay for output/ input signal), high-density (smaller layout area for the output buffer), and heavy-loading (high driving/ sinking capability) CMOS ICs.

In Refs [25] and [26], a modified structure of lateral SCR device called as LVTSCR (low-voltage trigger SCR) had been reported to effectively protect the output NMOS in submicron CMOS technology. This LVTSCR device is placed in parallel with the output NMOS from the output pad to ground. The LVTSCR device is made by inserting a short-channel NMOS device into the lateral SCR device to lower its trigger voltage. As a positive ESD voltage occurs at the output pad, this ESD voltage is diverted to the drain of the short-channel NMOS device in the LVTSCR device and leads to snapback breakdown on the short-channel NMOS device. This snapback breakdown causes the selfregeneration turn-on action in the LVTSCR device. After the turn-on action, the LVTSCR is held at its low-impedance state to bypass the ESD current. The LVTSCR device can provide ESD protection for the output NMOS without adding any series resistor between the output buffer and the output pad.

By another method, a dynamic gate-coupled design [27–30] was reported to improve ESD reliability of large-dimension output NMOS in scaled-down CMOS technology by ensuring uniform ESD current flow among the multiple fingers of the output NMOS [31]. In Refs [27–29], a parasitic N-type field–oxide device is connected to the gate of the output NMOS to achieve uniform ESD power distribution on the whole output NMOS



Fig. 2. The four modes of ESD-stress conditions occurred at an output pin of a CMOS IC.

device. The experimental results showed the uniform turn-on phenomenon of the gate-coupled output NMOS with a much larger device dimension. To couple suitable ESD-transient voltage to the gate of the output NMOS, the capacitance ratio between the output NMOS and the field–oxide device has to be calculated in advance [29].

2.3. Unexpected ESD damages

Since ESD voltages happening to a pin may have positive or negative polarities with the relatively grounded VDD or VSS pins, there are four different ESD-stress conditions on an output pin as shown in Fig. 2:

- 1. PS-mode, a positive ESD voltage on a pin with the VSS pin relatively grounded, but the VDD pin and other pins are floating;
- 2. NS-mode, a negative ESD voltage on a pin with the VSS pin relatively grounded, but the VDD pin and other pins are floating;
- 3. PD-mode, a positive ESD voltage on a pin with the VDD pin relatively grounded, but the VSS pin and other pins are floating;
- 4. ND-mode, a negative ESD voltage on a pin with the VDD pin relatively grounded, but the VSS pin and other pins are floating.

The ESD failure threshold of a pin is defined as the lowest (in absolute value) ESD-sustaining voltage of the four-mode ESD stresses on the pin. For example, if an output pin can sustain even up to 4 kV ESD voltage in the PS-, NS-, and PD-mode ESD stresses, but can only sustain 1 kV ESD voltage in the ND-mode ESD stress, the ESD failure threshold for this output pin is defined as 1 kV only. In Refs [19, 20, 22–26, 28] and [29], the ESD protection is emphasized from the output pad to VSS (GND). The additional ESD-protection

elements are all placed from the output pad to ground in parallel with the output NMOS device. There is no additional ESD protection element arranged between the output pad and VDD. Under the ND- or PD-mode ESD stresses, the output PMOS (or the output device between VDD and the output pad) becomes more sensitive to ESD damage. The overall ESD failure threshold may be not effectively improved. Thus, an effective ESD protection circuit for an output buffer in scaleddown CMOS technologies should provide strong ESD discharging paths from the output pad to both VSS and VDD.

Moreover, if there is no effective ESD-protection element arranged between the pad and VDD, an unexpected ESD damage had been found to locate in the internal circuits beyond the CMOS output buffer under the ND-mode ESD stress [32]. Figure 3 shows a schematic diagram to explain the unexpected discharging paths from the output pad to the internal circuits of a CMOS IC under the ND-mode ESD-stress condition. The ND-mode ESD voltage between the output pad and VDD is first diverted to the floating VSS power line through the output NMOS before the output PMOS breaks down to bypass ESD current from the output pad to VDD. The diverted negative ESD voltage on the VSS power line will cause voltage stress across the VSS and VDD power lines. If this ESD voltage across the VSS and VDD power lines cannot be effectively and quickly bypassed through the VDDto-VSS clamp device; this ND-mode ESD voltage will cause some further unexpected ESD damages on the internal circuits. Due to the parasitic resistance $(R_{DD} \text{ and } R_{SS})$ and capacitance (C_{DD}) along the VSS and VDD power lines in the CMOS VLSI/ ULSI [33], as well as the voltage drop across the

622



Fig. 3. Schematic circuit diagram to show the unexpected ESD damages in the internal circuits beyond the output buffer due to the ND-mode ESD stress.

VDD-to-VSS ESD clamp device, such an ND-mode ESD stress had been reported to cause some unexpected ESD damages on the internal circuits beyond the output buffer and the ESD protection devices [32–35]. Thus, a CMOS output buffer for advanced scaled-down CMOS ICs has to provide effective and direct ESD discharging paths from the output pad to both VSS and VDD. This is especially necessary for the submicron CMOS VLSI/ ULSI with a larger die size and much longer VDD and VSS power lines which often surround the whole chip.

3. NEW OUTPUT ESD PROTECTION FOR CMOS OUTPUT BUFFER

To effectively improve ESD robustness of the CMOS output buffer in submicron CMOS technologies by using the advantages of the LVTSCR device, a new ESD protection circuit for CMOS output buffer is proposed in this section with the consideration of avoiding the unexpected ESD damages in the internal circuits.

3.1. Circuit configuration

The schematic circuit diagram of the proposed output ESD protection for the CMOS output buffer is shown in Fig. 4, where a PTLSCR device (PMOS-trigger lateral SCR) and an NTLSCR device (NMOS-trigger lateral SCR) are used to protect the CMOS output buffer against the fourmode ESD stresses. The PTLSCR (NTLSCR) is placed in parallel with the output PMOS (NMOS) from the output pad to VDD (VSS). This PTLSCR (NTLSCR) is designed to be turned on before the output PMOS (NMOS) is broken down by the NDmode (PS-mode) ESD voltage. Thus, the ESD failure threshold of the CMOS output buffer can be significantly improved without using any extra series resistor between the output buffer and the output pad. In the CMOS output buffer, there also exist two parasitic junction diodes, Dp and Dn, in the device structure (the junction between the drain and the bulk) of the output PMOS and NMOS. The Dp (Dn) diode is in parallel to the output PMOS (NMOS) with its anode connected to the output pad (VSS). In Fig. 4, the PTLSCR (NTLSCR) is arranged to bypass the ND-mode (PS-mode) ESD stress, and the Dp (Dn) diode is used to bypass the PD-mode (NS-mode) ESD stress.

The trigger voltage of PTLSCR (NTLSCR) is equivalent to the snapback breakdown voltage of the inserted short-channel PMOS (NMOS) device rather than the original switching voltage (about 30–50 V) of a lateral SCR device. The snapback breakdown voltage of the short-channel thin-oxide PMOS and NMOS devices is dependent on the CMOS technology and channel length, but generally it is lower than the gate–oxide breakdown voltage in the same CMOS technology. The shorter



Fig. 4. Schematic circuit diagram of the new proposed ESD protection for CMOS output buffer with the PTLSCR and NTLSCR devices.

channel length leads to a lower snapback breakdown voltage on the thin-oxide NMOS and PMOS devices. To protect the output NMOS and PMOS, the channel length of the thin-oxide PMOS (NMOS) which is inserted in the PTLSCR (NTLSCR) structure should be designed shorter than that of the output PMOS (NMOS). Thus, the trigger voltage of PTLSCR (NTLSCR) can be lower than the breakdown voltage of the output PMOS (NMOS) device. When the ND-mode (PSmode) ESD events occur on the output pad, the PTLSCR (NTLSCR) will be first turned on to bypass ESD current before the output PMOS (NMOS) is broken down by the ESD voltage. Thus, the PTLSCR and NTLSCR devices can effectively protect the CMOS output buffer without adding extra series resistors as those used in Refs

[21–24], and avoid the unexpected ESD damages in the internal circuits [32–35].

3.2. Device structures

The schematic cross-sectional view of the PTLSCR device merged with the output PMOS device to save layout area is shown in Fig. 5(a), where the P-substrate N-well CMOS process is used to demonstrate the merged device structure. The PTLSCR is formed by a lateral SCR device with an inserted short-channel thin-oxide PMOS device, which is used to lower the trigger voltage of the lateral SCR device as shown in the right-hand part of Fig. 5(a). The purpose of inserting a short-channel thin-oxide PMOS in its snapback–breakdown condition to trigger on the lateral



Fig. 5. Schematic cross-sectional views of: (a) the output PMOS and the merged PTLSCR device; and (b) the output NMOS and the merged NTLSCR device, realized in the P-substrate N-well CMOS process.

SCR structure during the ND-mode ESD stresses. The inserted PMOS in the PTLSCR is formed by a non-connection P⁺ diffusion across the N-well/Psubstrate junction as its drain, the N-well connected to VDD as its bulk, and a P^+ diffusion in the Nwell of bulk as its source. The gate of this inserted PMOS is connected to VDD to ensure that it is off in the normal operating conditions of CMOS ICs. The trigger voltage of the PTLSCR device is equivalent to the snapback-breakdown voltage of the inserted PMOS. The holding voltage of PTLSCR device is still the same as the original holding voltage (about 1-2 V) of a lateral SCR device with a very low turn-on resistance $(2-5 \Omega)$ to bypass the ESD current. A layout example of the PTLSCR merged with the output PMOS and latchup guard rings is shown in Fig. 6, where the A-A' line is drawn to indicate the corresponding cross-sectional view in Fig. 5(a). The output PMOS with three drain fingers is drawn in the left-hand part of Fig. 5(a).

The schematic cross-sectional view of the NTLSCR device merged with the output NMOS to save layout area is shown in Fig. 5(b) in the Psubstrate N-well CMOS process. The NTLSCR is formed by a lateral SCR device with an inserted short-channel thin-oxide NMOS device, which is used to lower the trigger voltage of the lateral SCR device, as shown in the right-hand part of Fig. 5(b). Under the PS-mode ESD-stress condition, the drain of the inserted NMOS is broken down to trigger on the lateral SCR structure. The inserted NMOS in the NTLSCR is formed by a non-connection \mathbf{N}^{+} diffusion across the N-well/P-substrate junction as its drain, the P-substrate connected to VSS as its bulk and an N⁺ diffusion in another adjacent Nwell as its source. The gate of the inserted NMOS is connected to VSS to ensure that it is off in the normal operating conditions of CMOS ICs. The trigger voltage of the NTLSCR device is equivalent to the snapback-breakdown voltage of the inserted NMOS. The holding voltage of NTLSCR device is kept the same as the original holding voltage (about 1-2 V) of a lateral SCR device with a very low turn-on resistance $(2-5 \Omega)$ to bypass the ESD current. A layout example of the NTLSCR merged with the output NMOS and latchup guard rings is also shown in Fig. 6, where the B-B' line is drawn to indicate the corresponding cross-sectional view in Fig. 5(b). The thin-oxide output NMOS with three drain fingers is drawn in the left-hand part of Fig. 5(b).

The Dp (Dn) diode is essentially formed by the p-n junction from the drain of the output PMOS (NMOS) to its bulk. This parasitic Dp (Dn) diode can offer an effective ESD discharging path to bypass the PD-mode (NS-mode) ESD stress and a voltage-clamping effect to limit the overshooting (undershooting) noise pulse on the output pad.

The PTLSCR and NTLSCR devices can be also realized by P-well/N-substrate CMOS technology. The cross-sectional views for the PTLSCR and NTLSCR realized in the N-substrate P-well CMOS process are shown in Fig. 7. Similarly, the inserted PMOS in the PTLSCR device of Fig. 7(a) is formed by a non-connection P^+ diffusion across the N-substrate/P-well junction as its drain, the Nsubstrate connected to VDD as its bulk, and a P⁺ diffusion in another adjacent P-well as its source. The inserted NMOS in the NTLSCR device of Fig. 7(b) is formed by a non-connection N^+ diffusion across the N-substrate/P-well junction as its drain, the P-well connected to VSS as its bulk, and an N^+ diffusion in the P-well of bulk as its source. The inserted PMOS and NMOS are kept off in the normal operating conditions of CMOS ICs. The layout style of the PTLSCR and NTLSCR devices merged with the CMOS output buffer in Fig. 7 by the N-substrate/P-well CMOS process can be as compact as that of Fig. 6 by a P-substrate/N-well CMOS process.

3.3. Circuit operating principles

3.3.1. In normal operating conditions. In the CMOS normal operations, the VDD is biased at 5 V (or 3 V in low-voltage application) and the VSS is grounded. Under this condition, the inserted PMOS and NMOS in the PTLSCR and NTLSCR structures are kept off due to their gates are connected to their sources. Thus, the PTLSCR and NTLSCR are kept off in the normal operating conditions of CMOS ICs. The CMOS output buffer works to drive/sink current to/from the external output load.

The diodes Dp and Dn also provide the voltagelevel clamping effect on the output signals. The diode Dp clamps the high-level voltage of output signals to about VDD + 0.6 V. The diode Dn clamps the low-level voltage of output signals to about VSS – 0.6 V. Thus, the voltage level of output signals even with overshooting or undershooting transition is clamped between about 5.6 and -0.6 V in the normal operations of CMOS ICs.

3.3.2. In ESD-stress conditions. When a PS-mode ESD event occurs, the ESD voltage is diverted to the anode of the NTLSCR, and then to the drain of the inserted NMOS due to the P⁺ diffusion/Nwell/ N^+ diffusion forward conducting path. The inserted NMOS in the NTLSCR is first turned on by means of drain snapback breakdown to clamp the positive ESD voltage on the pad. As the snapback breakdown occurs in the drain of the inserted NMOS, the ESD current is conducted from the Nwell, through the snapback-breakdown drain of the inserted NMOS to the P-substrate, and then to the N⁺ diffusion in the adjacent N-well. This conducting current from the N-well to the P-substrate due to the snapback-breakdown drain of the inserted NMOS leads to the self-regeneration of latchup







Fig. 7. Schematic cross-sectional views of: (a) the output PMOS and the merged PTLSCR device; and (b) the output NMOS and the merged NTLSCR device, realized in the N-substrate P-well CMOS process.

happening in the NTLSCR device. Once the latchup happens in the NTLSCR, a path with very low impedance from the output pad to VSS (GND) is created. Then, the ESD current is mainly discharged through the lateral SCR structure of the NTLSCR device. The ESD voltage on the output pad becomes clamped by the holding voltage of the turn-on lateral SCR structure to about 1–2 V. This NTLSCR device can effectively protect the CMOS output buffer against the PS-mode ESD damages alone without adding any extra series resistor. Due to the high capability of power delivery in the SCR device, the NTLSCR with a lower trigger voltage can sustain a higher ESD-stress current in a small layout area.

In the NS-mode (PD-mode) ESD event, the ESD stress with negative (positive) voltage occurs at the

output pad and the VSS (VDD) is grounded but the VDD (VSS) is floating. The negative (positive) ESD voltage is diverted to the drain of the output NMOS (PMOS). The parasitic diode Dn (Dp) in the output NMOS (PMOS) is forward biased and turned on to bypass ESD current. The negative (positive) ESD voltage on the output pad is clamped by the turn-on diode Dn (Dp) to about -0.6 V (+0.6 V) so as to protect the output buffer. The diode Dn (Dp) in its forward-conducting condition can sustain very high ESD current.

When the ND-mode ESD event occurs at the output pad with negative polarity to the grounded VDD, but the VSS is floating, the ESD voltage is diverted to the cathode of the PTLSCR, and then to the drain of the inserted PMOS through the P^+ diffusion/P-substrate/N-well/N⁺ diffusion forward-



Fig. 8. The schematic cross-sectional view of a CMOS output buffer with the N-well resistor [23].

conducting path. The inserted PMOS in the PTLSCR is first turned on by means of drain snapback-breakdown to clamp the negative ESD voltage on the output pad. As the snapbackbreakdown occurs in the drain of the inserted PMOS, the ESD current is conducted from the P^+ diffusion (the anode of PTLSCR, connected to VDD), through the snapback-breakdown drain of the inserted PMOS to the P-substrate, and then to the N⁺ diffusion in the adjacent N-well connected to the output pad. This conducting current from the N-well to the P-substrate due to the snapbackbreakdown drain of the inserted PMOS leads to the self-regeneration of latchup happening in the PTLSCR device. Once the latchup happens in the PTLSCR, a path with very low impedance from VDD to the output pad is created. Then, the ESD current is mainly discharged through the lateral SCR structure of the PTLSCR device. The ESD voltage on the output pad becomes clamped by the holding voltage of the turn-on lateral SCR structure to about 1 to 2 V. This PTLSCR can effectively protect the CMOS output buffer against ND-mode ESD damages alone without adding any extra series resistor. Due to the high capability of power delivery in SCR device, the PTLSCR with a lower trigger voltage can sustain a high ESD-stress current in a small layout area.

4. EXPERIMENTAL RESULTS

4.1. ESD reliability

One set of test-keys is fabricated by a $0.6 \,\mu\text{m}$ single-poly three-metal CMOS technology with LDD and polycide processes to verify this output ESD protection design, in which a modified CMOS

output buffer with the N-well resistor [23] is also fabricated as a comparing reference. The device's width and length in the output PMOS (NMOS) of the modified CMOS output buffer are 300 and 1.0 (200 and 1.0) μ m, respectively. The schematic crosssectional view of the modified CMOS output buffer with the N-well resistor is shown in Fig. 8, where the drain of the output NMOS is connected to the output pad through an N-well structure. The layout area of the output PMOS (NMOS) including the latchup guard rings in the modified CMOS output buffer is 112.6×52 (136.2×52) μ m².

Corresponding to the layout in Fig. 6, the output buffer protected by the PTLSCR and NTLSCR has a device W/L of 312/1.0 (300/1.0) for the output PMOS (NMOS), whereas the inserted PMOS (NMOS) to trigger on the PTLSCR (NTLSCR) has a device W/L of 60/0.8 (60/0.8). The total layout area for the output PMOS (NMOS) with the merged PTLSCR (NTLSCR) including latchup guard rings is 107.4×86 (111.4 × 86) μm^2 . However, the PTLSCR (NTLSCR) only occupies a layout area of 60×37 (60×38) μm^2 in Fig. 6. As expected by this design, the PTLSCR (NTLSCR) can be turned on to protect the output PMOS (NMOS) in the ND-mode (PS-mode) ESD-stress conditions. The PTLSCR (NTLSCR) can provide high ESD protection level to the CMOS output buffer, but it only occupies very small layout area. The typical ESD testing results are shown in Table 1.

The ESD-stress voltage is set to begin with an initial voltage of 1000 V and increase up to 8000 V with an increase step of 250 V in the human-body-model (HBM) ESD testing. The machine-model (MM) ESD stress with faster ESD-transient conditions is also used to investigate the ESD





Fig. 9. The equivalent circuit of the industrial ESD-testing standards in: (a) the human-body-model; and (b) the machine-model.

robustness of the fabricated CMOS output buffer. The equivalent circuit diagrams for these two industrial ESD testing standards are shown in Fig. 9. The ESD tester used in this measurement is the ZAPMASTER produced by the KeyTeck Instrument Corp. [36] The four modes of ESD stresses are applied to the test-chip. The failure criterion is defined as the leakage current of the CMOS output buffer in the off state becoming above 1 μ A under 5 V voltage bias after the ESD stress. The lowest (in absolute values) ESD failure voltage among the four modes of ESD stresses at the same output pin is defined as the ESD failure threshold of the output pin. The results in Table 1 show that the CMOS output buffer protected by the PTLSCR and NTLSCR can perform ESD failure threshold up to above 4250 V (750 V) in HBM (MM) ESD testing within a very small layout area. The modified CMOS output buffer, even with the N-well resistor, the 5 μ m spacing from the drain contact to the poly-gate edge, and a larger layout area, can sustain an ESD level of only 1250 V (100 V) in the HBM (MM) ESD stresses. This verifies the excellent ESD-protection capability of the proposed PTLSCR and NTLSCR devices for the CMOS output buffer in scaled-down CMOS technologies.

4.2. Device I-V characteristics

The turn-on characteristics of the PTLSCR and the output PMOS are also measured and shown in Fig. 10. Figure 10(a) shows the normal I-V curves

Ming-Dou Ker







Fig. 10. Device I-V characteristics of: (a) the output PMOS in the CMOS output buffer; (b) the PTLSCR in the CMOS output buffer; and (c) snapback breakdown in a separated output PMOS device without the merged PTLSCR.







Fig. 11. Device *I–V* characteristics of: (a) the output NMOS in the CMOS output buffer; (b) the NTLSCR in the CMOS output buffer; and (c) snapback breakdown in a separated output NMOS device without the merged NTLSCR.

of the output PMOS under different V_{gs} biases in the CMOS output buffer of Fig. 5(a) with the PTLSCR. With a $V_{\rm ds}$ of up to -10 V applied to the drain of the output PMOS, the I-V curves of PMOS as shown in Fig. 10(a) are still not affected by the PTLSCR. Thus, the PMOS device in the CMOS output buffer can normally perform the driving current to the output pad without any degradation by the PTLSCR. If the gate of the output PMOS is connected to its source and an ND-mode voltage is applied to the output pad, the I-V curves of the PTLSCR can be measured and are shown in Fig. 10(b). This means that the PTLSCR is triggered on before the breakdown of the output PMOS. The trigger voltage (current) of the PTLSCR is -12.92 V (-4.7 mA), and its holding voltage (current) is -1.24 V (-7.5 mA). The channel length of the inserted PMOS in the PTLSCR is $0.8 \,\mu\text{m}$. To verify that the PTLSCR is indeed triggered on before the output PMOS breaks down, a separated PMOS device without the PTLSCR has to be also fabricated in the same testchip to find the snapback-breakdown characteristics of the pure output PMOS. The snapbackbreakdown I-V curve of the pure PMOS device with a channel length of $1.0 \,\mu\text{m}$ is shown in Fig. 10(c), which is measured by applying a negative voltage to the drain of the PMOS device with its gate and source connected to ground. The trigger voltage (current) of the snapback breakdown in the output PMOS is -15.62 V (-15.85 mA). The holding voltage (current) of the output PMOS in its snapback region is -13.84 V (-13.9 mA). Because the trigger voltage and current of the output PMOS into its snapback region is greater than that of the PTLSCR into its latching state, the PTLSCR has been confirmed to be turned on before the output PMOS breaks down. Thus, under the ND-mode ESD-stress condition, the PTLSCR is guaranteed to be first turned on to protect the CMOS output buffer.

The turn-on characteristics of the NTLSCR and the output NMOS devices in the CMOS output buffer are also measured and are shown in Fig. 11. The I-V curves of the output NMOS in the CMOS output buffer with the NTLSCR under the normal operation conditions are shown in Fig. 11(a). The I-V curve of the NTLSCR in the CMOS output buffer is shown in Fig. 11(b). The channel length of the inserted NMOS in the NTLSCR is 0.8 μ m. The trigger voltage (current) of the NTLSCR is 12.94 V (12.3 mA) and its holding voltage (current) is 1.1 V (6.9 mA). The snapback-breakdown characteristics of a pure NMOS device with the channel length of $1.0 \,\mu\text{m}$ in the CMOS output buffer is shown in Fig. 11(c). The trigger voltage (current) of the snapback breakdown in the output NMOS is 13.7 V (4.76 mA). The holding voltage (current) of the output NMOS in its snapback region is 9.78 V (5.42 mA). Comparing the I-V curves between Fig. 11(b) and (c), it can be guaranteed that the NTLSCR can be first turned on before the output NMOS is broken down under the PS-mode ESD-stress condition. The holding voltage of the NTLSCR is also much smaller than the snapback voltage of the NMOS in the CMOS output buffer. Thus, the NTLSCR can effectively protect the CMOS output buffer against ESD damage.

4.3. Pulse-type triggering characteristics

To verify the PTLSCR and NTLSCR being first triggered on to protect the CMOS output buffer in the ESD-stress conditions, an experimental set-up is shown in Fig. 12 and used to find the pulse-type trigger voltage of the PTLSCR and NTLSCR. In Fig. 12(a), it is used to simulate the ND-mode ESD-stress condition, where the VDD is relatively grounded and the VSS is floating. A negative voltage pulse generated from the HP8116A (pulse generator) is applied to the output pad. If the PTLSCR is triggered on by the applied voltage pulse, the voltage waveform on the output pad will be seriously degraded due to the very low turn-on





Fig. 12. The experimental set-up to find the pulse-type trigger voltage of: (a) the PTLSCR in the ND-mode ESD-stress condition; and (b) the NTLSCR in the PS-mode ESD-stress condition.

Electrostatic discharge protection



(a)



Fig. 13. Voltage waveforms of: (a) a -13 V negative voltage pulse applied on the output pad without causing any waveform degradation; and (b) a -13.7 V negative voltage pulse applied on the output pad with serious waveform degradation.

resistance of the PTLSCR and the voltage level on the output pad will be clamped near to the holding voltage (~ -2 V) of the PTLSCR. If the output PMOS is first triggered on, the voltage on the output pad will be clamped by the snapback voltage (about ~ -14 V) of the output PMOS. However, if neither the PTLSCR nor the output PMOS is triggered on, the voltage waveform on the output pad will remain the same. The measured results are shown in Fig. 13. In Fig. 13(a), the voltage pulse with a pulse height of -13.0 V, a fall time about 7–10 ns, and a pulse width of 2 μ s is applied to the output pad, but the voltage waveform still remains in its original pulse-type waveform without any degradation. Thus, such a -13 V voltage pulse cannot trigger on the PTLSCR and the output PMOS. If the pulse height of the applied voltage pulse is increased to -13.7 V, the voltage waveform

on the output pad is measured and shown in Fig. 13(b), where the voltage waveform is seriously degraded. As shown in Fig. 13(b), the falling edge of the applied negative voltage pulse triggers on the PTLSCR and causes a voltage clamp about -2.438 V on the output pad. Thus, the PTLSCR has been further verified to be triggered on before the output PMOS breaks down in the ND-mode ESD-stress condition. With such a low clamping

voltage, the CMOS output buffer can be fully protected by the PTLSCR.

Similarly, in Fig. 12(b), a positive voltage pulse is applied to the output pad to investigate the pulsetype triggering behavior of the NTLSCR. The VDD is floating and the VSS is grounded to simulate the PS-mode ESD-stress condition. A positive voltage pulse as shown in Fig. 14(a) with a pulse height of 13.0 V, a rise time about 7–10 ns, and a







(b)

Fig. 14. Voltage waveforms of: (a) a +13 V voltage pulse applied on the output pad without causing any waveform degradation; and (b) a +13.5 V voltage pulse applied on the output pad with serious waveform degradation.

pulse width of 2 μ s is applied to the output pad, but the voltage waveform still remains in its original pulse-type waveform without any degradation. So, such a 13 V voltage pulse cannot trigger on the NTLSCR and the output NMOS. If the pulse height of the applied voltage pulse is increased to 13.5 V, the voltage waveform on the output pad is measured and shown in Fig. 14(b), where the voltage waveform is seriously degraded. The rising edge of the positive voltage pulse triggers on the NTLSCR and clamps the voltage level on the output pad at 2.375 V. Thus, the NTLSCR has been further verified to be triggered on before the output NMOS breaks down in the PS-mode ESD-stress condition. With such a low clamping voltage, the CMOS output buffer can be fully protected by the NTLSCR.

4.4. Noise margin in the normal operating conditions

The PTLSCR and NTLSCR are designed to be triggered on only in the ESD-stress conditions, but to be kept off in the normal operating conditions of the CMOS IC with 5 V VDD and 0 V VSS power supplies. However, in practical applications, there may be some overshooting or undershooting noise pulses attaching to the output pad. Therefore, the PTLSCR and NTLSCR should have a suitable noise margin to the output overshooting or undershooting noise pulses that is dependent on the application environment of the IC. To investigate the noise margin of the PTLSCR and NTLSCR in the CMOS output buffer, an experimental set-up is shown in Fig. 15.

In Fig. 15(a), the VDD is biased at 5 V and the VSS is biased at 0 V. The gates of both the output PMOS and NMOS are connected to VSS to provide a 5V output voltage on the output pad. An overshooting noise pulse is simulated by a voltage pulse generated from the pulse generator with a low-voltage level of 5 V and an adjustable highvoltage level of $V_{\rm p}$. If the NTLSCR is triggered on by the overshooting noise pulse, the voltage level on the output pad will be dropped down to below 5 V due to the very low turn-on resistance of the NTLSCR. On the contrary, if the NTLSCR is not triggered on by the overshooting noise pulse, the voltage level on the output pad should remain at 5 V. An overshooting noise pulse with a pulse height of 8 V and a pulse width of 2 μ s is generated and shown in Fig. 16(a). The rise time of such a simulated overshooting noise pulse is about 7-10 ns. This simulated overshooting noise pulse is directly applied to the output pad as shown in Fig. 15(a), and the voltage waveform on the output pad is monitored and shown in Fig. 16(b). As seen in Fig. 16(b), the high-voltage level is clamped to 5.937 V by the diode Dp and the low-voltage level still remains at 5 V, so the NTLSCR is not triggered on by the 8 V overshooting noise pulse. The parasitic diode Dp in the output PMOS provides a



Fig. 15. The experimental set-up to find the noise margin of: (a) the NTLSCR in the overshooting condition; and (b) the PTLSCR in the undershooting condition.

high-voltage clamping effect to limit the overshooting voltage pulse on the output pad, so the NTLSCR is not triggered on by the overshooting noise pulse in the normal CMOS operating conditions. The rising edge of the voltage waveform in Fig. 16(b) is shown in Fig. 16(c) to clearly show the clamping transition.

In Fig. 15(b), the gates of both the output PMOS and NMOS are connected to VDD to provide a 0 V output voltage on the output pad. An undershooting noise pulse is simulated by a voltage pulse generated from the pulse generator with a highvoltage level of 0 V and an adjustable low-voltage level of $-V_p$. If the PTLSCR is triggered on by the undershooting noise pulse, the voltage level on the output pad will rise up to be above 0 V due to the very low turn-on resistance of the PTLSCR. On the contrary, if the PTLSCR is not triggered on by the undershooting noise pulse, the voltage level on the output pad should remain at 0 V. An undershooting noise pulse with a negative pulse height of -3.3 V and a pulse width of 2 μ s is shown in Fig. 17(a). The fall time of such a simulated undershooting noise pulse is about 7-10 ns. This simulated undershooting noise pulse is directly applied to the output pad as shown in Fig. 15(b), and the voltage waveform on the output pad is monitored and shown in Fig. 17(b). As seen in Fig. 17(b), the low-voltage level is



Fig. 16. Voltage waveforms of: (a) an overshooting voltage pulse generated from the HP8116A pulse generator with a pulse height of 8 V; and (b) the clamped overshooting voltage pulse on the output pad; and (c) the rising edge of the clamped overshooting voltage pulse in (b).

Electrostatic discharge protection







(b)

Fig. 17. Voltage waveforms of: (a) an undershooting voltage pulse generated from the HP8116A pulse generator with a negative pulse height of -3.3 V; and (b) the clamped undershooting voltage pulse on the output pad.

clamped to -0.92 V by the diode Dn and the highvoltage level still remains at 0 V, so the PTLSCR is not triggered on by the -3.3 V undershooting noise pulse. The parasitic diode Dn in the output NMOS provides a low-voltage clamping effect to limit the undershooting voltage pulse on the output pad, so the PTLSCR is not triggered on by the overshooting noise pulse in the normal CMOS operating condition. With the voltage clamping effect of the parasitic Dp and Dn diodes, the PTLSCR and NTLSCR have been practically verified to have a noise voltage level of greater than +8 V (lower than -3.3 V) to the overshooting (undershooting) noise pulse on the output pad. The noise margin can be further increased if the diode clamping effect is enhanced. But how much the noise margin is adequate is dependent on the application environment of the

IC. In the most applications of CMOS ICs with a 5 V power supply, a voltage margin of +8 V (-3.3 V) to the overshooting (undershooting) noise pulse has been a reasonable design.

4.5. Discussion on layout spacing in the output buffer

For better ESD robustness consideration, the layout spacing "d" from the drain contact to the poly-gate edge is often drawn as 5 μ m in the output NMOS and PMOS [14, 37]. Suitably spaced d can help the uniform current distribution among the drain contacts of the fingers in the finger-type layout to improve the ESD level of the output buffer. But a wider layout spacing d causes the output buffer to occupy a larger layout area.

Because the channel length of the inserted NMOS/PMOS in the NTLSCR/PTLSCR is shorter than that of the output buffer, the NTLSCR/ PTLSCR can be triggered on to protect the output buffer before the output buffer is damaged by the ESD pulse. The turn-on speed of the PTLSCR/ NTLSCR has been practically verified in Figs 13 and 14 in the ND- and PS-mode ESD-stress conditions, respectively. As shown in Fig. 13(b) and 14(b), the PTLSCR (NTLSCR) can be immediately triggered on by the applied negative (positive) voltage pulse. Therefore, the spacing *d* in the output buffer which is protected by such PTLSCR/ NTLSCR can be reasonably reduced from 5 μ m to about 1 μ m to further save the layout area.

5. CONCLUSION

A robust output ESD protection has been designed and verified in an advanced $0.6 \,\mu\text{m}$ CMOS process. The trigger voltage of PTLSCR (NTLSCR) is lowered to the snapback-trigger voltage of a short-channel thin-oxide PMOS (NMOS) device inserted into the SCR structure. However, the holding voltage of PTLSCR and NTLSCR devices is still the same as that of a lateral SCR device. The PTLSCR and NTLSCR devices with enough lower trigger voltage can effectively protect the CMOS output buffer within a small layout area than other output ESD protection circuits in submicron CMOS ICs. The PTLSCR and NTLSCR provide the CMOS output buffer with direct ESD discharging paths and low clamping voltage levels from the output pad to both VDD and VSS, so the unexpected ESD damages in the internal circuits can be avoided. This ESD protection circuit can be also free to the VDD-to-VSS latchup problem in 5 V CMOS ICs. Under the 5 V CMOS operating conditions, the CMOS output buffer has a noise margin greater than +8 V (lower than -3.3 V) to the overshooting (undershooting) noise pulse for practical applications without the undesired triggering on the PTLSCR and NTLSCR. One set of area-efficient CMOS output buffers with different driving specifications has been designed with this ESD protection circuit and included into a 0.6 μ m CMOS standard cell library for chip synthesis. It has been successfully used in some ASICs to provide the output function with an operating frequency of up to 50 MHz.

With a high ESD failure threshold in a small layout area and without adding any extra series resistor between the output pad and the output buffer, this proposed output ESD protection design provides an effective ESD protection to the CMOS output buffer without causing any degradation on the circuit performance or the output voltage level and timing specifications. Thus, this proposed output ESD protection design is very suitable for the scaled-down CMOS VLSI in high-reliability, highdensity and high-speed applications.

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