

Lateral SCR Devices with Low-Voltage High-Current Triggering Characteristics for Output ESD Protection in Submicron CMOS Technology

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Abstract— A high-current PMOS-trigger lateral SCR (HIPTSCR) device and a high-current NMOS-trigger lateral SCR (HINTSCR) device with a lower trigger voltage but a higher trigger current are proposed to improve ESD robustness of CMOS output buffer in submicron CMOS technology. The lower trigger voltage is achieved by inserting a short-channel thin-oxide PMOS or NMOS devices into the lateral SCR structures. The higher trigger current is achieved by inserting the bypass diodes into the structures of the HIPTSCR and HINTSCR devices. These HIPTSCR and HINTSCR devices have a lower trigger voltage to effectively protect the output transistors in the ESD-stress conditions, but they also have a higher trigger current to avoid the unexpected triggering due to the electrical noise on the output pad when the CMOS IC's are in the normal operating conditions. Experimental results have verified that the trigger current of the proposed HIPTSCR (HINTSCR) is increased up to 225.5 mA (218.5 mA). But, the trigger voltage of the HIPTSCR (HINTSCR) is still remained at a lower value of 13.4 V (11.6 V). The noise margin against the overshooting (undershooting) voltage pulse on the output pad, without accidentally triggering on the HINTSCR (HIPTSCR), can be greater than $V_{DD}+12$ V ($V_{SS}-12$ V). These HIPTSCR and HINTSCR devices have been practically used to protect CMOS output buffers with a 4000-V (700-V) HBM (MM) ESD robustness but only within a small layout area of $37.6 \times 60 \mu\text{m}^2$ in a standard $0.6\text{-}\mu\text{m}$ CMOS technology without extra process modification.

I. INTRODUCTION

ELECTROSTATIC discharge (ESD) protection has become a main concern on the reliability of IC products in submicron CMOS technologies. To improve ESD robustness of CMOS output buffer and also to drive/sink current to/from the external heavy load, the output NMOS and PMOS devices are often designed with large device dimensions. Even with such large device dimensions, the ESD robustness of the CMOS output buffer had been still reported to be seriously degraded by the advanced submicron CMOS technologies [1]–[4].

Recently, the lateral SCR device had been used as an ESD-protection element for input protection in submicron CMOS IC's [5]–[8]. The trigger voltage (current) of the lateral

SCR device (LSCR) in the CMOS technology is about ~ 50 V (~ 10 mA) [5]. With such a high trigger voltage, the LSCR needs a large series resistor and a gate-grounded NMOS in the secondary protection circuit to perform the overall input ESD protection function. But, this large series resistor also causes a longer time delay for the input signal and often occupies a larger layout area. To reduce the trigger voltage of the LSCR, a modified lateral SCR device (MLSCR) was reported for input ESD protection. The trigger voltage (current) of the MLSCR in the CMOS technology is about ~ 25 V (~ 10 mA) [6]. The lateral SCR device had been found to provide the highest ESD protection capability in a smallest layout area, as compared to other ESD protection elements such as the diode, the thick-oxide device, the gate-oxide device, and the parasitic bipolar device in submicron CMOS IC's [9]. But the trigger voltages of the LSCR and MLSCR are still greater than the breakdown voltages of the output transistors in the CMOS output buffers. Therefore, they can not provide efficient output ESD protection alone.

To effectively protect the CMOS output buffer, the LVTSCR (low-voltage triggering SCR) device has been invented with a much lower trigger voltage [10]–[13]. The trigger voltage of the LVTSCR device is equivalent to the snapback-trigger voltage of the short-channel NMOS (or PMOS) device, which is inserted into the lateral SCR structure, rather than the original switching voltage (about 30–50 V) of the lateral SCR device. The shorter channel length of the inserted NMOS (or PMOS) leads to a lower snapback-trigger voltage of the LVTSCR device [10]–[13]. The trigger voltage (current) of the LVTSCR device in the CMOS technology had been lowered about ~ 10 V (~ 10 mA) [10]. In [14], a circuit technique was used to achieve bi-modal triggering for the LVTSCR device. The bi-modal LVTSCR was designed to be turned on with a much lower trigger voltage in the ESD stress condition. In the normal operating condition with the V_{DD} and V_{SS} power supplies, the gate of the bi-modal LVTSCR was biased at ground to keep itself off through the circuit technique. The trigger voltage (current) of the bi-modal LVTSCR in the off state with a 0-V gate voltage was shown as low as ~ 8 V (~ 15 mA) [14].

With such a low trigger voltage of the LVTSCR, the LVTSCR can provide effective ESD protection for the CMOS output buffers, but the lower trigger current may cause the LVTSCR being accidentally triggered on by the external

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overshooting or undershooting noise pulses on the output pin while the CMOS IC is operating in the noisy environments. Practically, due to the request of the “CE” mark from the European Community, an ESD gun with the ESD voltage of 8 kV or even up to 15 kV is used to test the electromagnetic compatibility (EMC) of the electronic products. The international standard of the electromagnetic-compatibility testing had been specified as “IEC 801-2” by the International Electron-technical Commission in 1991 [15]. Such an electromagnetic-compatibility testing by the ESD gun is the system-level ESD testing through the air-discharge or contact-discharge methods [15]. This system-level ESD event can not only cause the electronic system to “freeze” or “upset,” but also can actually “blow out” some of the integrated circuits in the electronic systems [16]–[18]. Such a system-level ESD event often causes the transient-induced noise pulses on the pins of the CMOS IC’s [19]–[21]. The LVTSCR with a low trigger voltage and a low trigger current is easily triggered on by this system-level EMC/ESD testing. If the LVTSCR attached to the input or output pins is triggered on by the unexpected overshooting or undershooting noise pulses, the signal level at the input or output pins will be held at “0” due to the very low turn-on resistance of the LVTSCR device. This leads to malfunction or operation error in the CMOS IC’s. So, for using the LVTSCR device to protect the input or output pins, the LVTSCR must have an enough noise margin against the overshooting or undershooting noise pulses when the CMOS IC’s are in the normal operating conditions.

There are two possible methods to avoid the LVTSCR being triggered on by the noise pulses when the IC is in the normal operating conditions. One possible method is to increase the holding voltage of the LVTSCR to be greater than the voltage of VDD. But, increasing the holding voltage of LVTSCR leads to more power dissipation ($\text{Power} \cong I_{\text{ESD}} \times V_{\text{hold}}$) located on the LVTSCR device during the ESD transition. This therefore causes a much lower ESD robustness of the LVTSCR. Moreover, to increase the holding voltage of the LVTSCR greater than VDD in the bulk CMOS process is difficult and often needs to occupy much wider layout spacings and more latchup guardrings. Another method is to only increase the trigger current of the LVTSCR device, but the trigger voltage and the holding voltage are kept the same. With a higher trigger current, the LVTSCR can have enough noise margin against the overshooting or undershooting noise pulses without either degrading its ESD protection performance or occupying large layout area.

In this paper, a high-current PMOS-trigger lateral SCR (HIPTSCR) and a high-current NMOS-trigger lateral SCR (HINTSCR) with lower trigger voltage but higher trigger current are proposed to safely protect the CMOS output buffer without the accidental triggering on by the electrical noisy pulses [22]. With a lower trigger voltage, the HIPTSCR and HINTSCR can effectively clamp the ESD voltage on the output pad to protect the output transistors in the ESD stress conditions. With a higher trigger current, the HIPTSCR and HINTSCR therefore have enough noise margin against the external noisy pulses without accidental triggering when the CMOS IC’s are in the normal operating conditions.

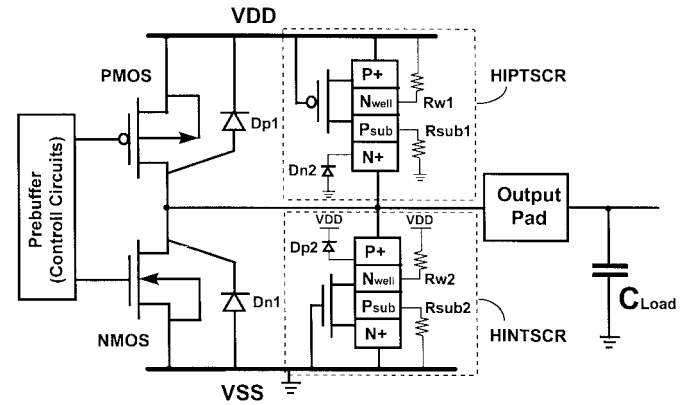


Fig. 1. A schematic circuit diagram of a CMOS output buffer protected by the proposed HIPTSCR and HINTSCR devices.

II. HIPTSCR AND HINTSCR DEVICES FOR OUTPUT ESD PROTECTION

A. Circuit Configuration

The schematic circuit diagram of a CMOS output buffer with the HIPTSCR and HINTSCR devices is shown in Fig. 1. The HIPTSCR (HINTSCR) is placed in parallel with the output PMOS (NMOS) device from the output pad to VDD (VSS). The anode of the HIPTSCR (HINTSCR) is connected to VDD (the output pad) and its cathode is connected to the output pad (VSS). This HIPTSCR (HINTSCR) device is designed to be turned on to bypass the ESD current before the output PMOS (NMOS) is damaged by the ND-mode (PS-mode) [13] ESD voltage. Since the HIPTSCR and HINTSCR can provide high ESD protection capability within a smaller layout area, the ESD robustness of the CMOS output buffer can be significantly improved. With suitable design on the channel length of the PMOS (NMOS) which is inserted into the HIPTSCR (HINTSCR) structure, the trigger voltage of the HIPTSCR (HINTSCR) can be below the snapback-trigger voltage of the output PMOS (NMOS) [10]–[12]. So, the HIPTSCR and HINTSCR can effectively protect the CMOS output buffer without adding any extra series resistor to the output buffer as those used in [23]–[25].

In the CMOS output buffer, there also exist two parasitic junction diodes, $Dp1$ and $Dn1$, in the device structure (the p-n junction between the drain and bulk) of the output PMOS and NMOS. The $Dp1$ ($Dn1$) is forward biased in the PD-mode (NS-mode) [13] ESD-stress condition. The diode in its forward-biased condition can sustain high ESD voltage. So, the CMOS output buffer often has a much higher ESD robustness in the PD-mode and NS-mode ESD stresses than it in the PS-mode and ND-mode ESD stresses. The HIPTSCR and HINTSCR are therefore used to improve the PS-mode and ND-mode ESD robustness of the CMOS output buffer.

The four modes of ESD stresses on the output pad are one-by-one protected by the HIPTSCR, the HINTSCR, the $Dp1$, and the $Dn1$. The low holding voltage (about 1–2 V) of the HIPTSCR and HINTSCR can effectively clamp the ESD voltage on the output pad. Especially in the ND-mode ESD-stress condition, the HIPTSCR with a low holding voltage can

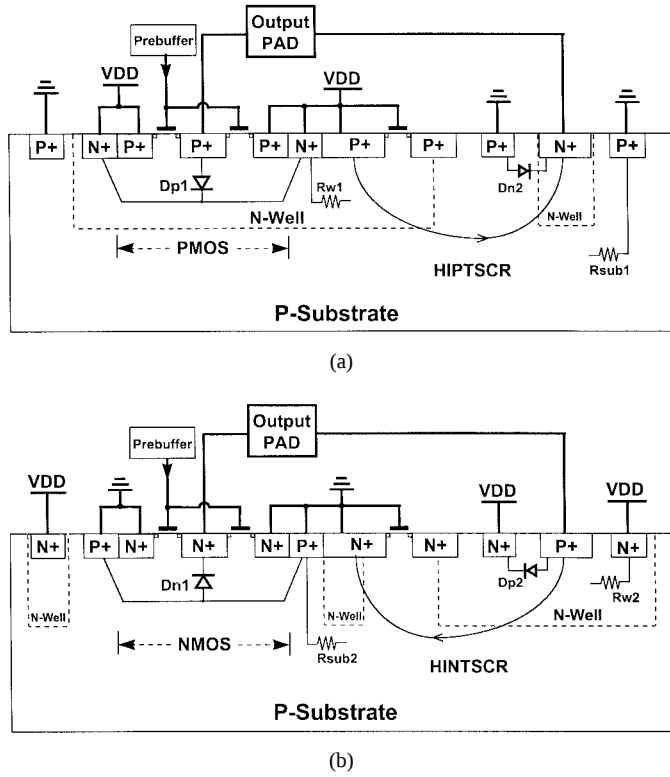


Fig. 2. Schematic cross-sectional views of (a) the output PMOS and the HIPTSCR device, and (b) the output NMOS and the HINTSCR device, in a P-substrate N-well CMOS process.

effectively bypass the ND-mode ESD current from the output pad to VDD without causing the unexpected ESD damages on the internal circuits.

B. Device Structures

The schematic cross-sectional views of the HIPTSCR and HINTSCR in a P-substrate N-well CMOS process are shown in Fig. 2(a) and (b), respectively. The HIPTSCR is formed by inserting a bypass diode $Dn2$ into a PMOS-trigger LVTSCR structure as shown in Fig. 2(a). The HINTSCR is formed by inserting a bypass diode $Dp2$ into an NMOS-trigger LVTSCR structure as shown in Fig. 2(b). This $Dn2$ ($Dp2$) has to be located into the latching path of the HIPTSCR (HINTSCR). This $Dn2$ ($Dp2$) has an effect of reducing the equivalent substrate resistor R_{sub1} (N-well resistor $Rw2$) and an effect of bypassing the latchup trigger current in the P-substrate (the N-well), so the trigger current to initiate the positive-feedback regenerative process of latchup in the HIPTSCR (HINTSCR) can be significantly increased [26], [27]. The trigger voltage of this HIPTSCR (HINTSCR) is kept the same as the snapback-trigger voltage of the short-channel PMOS (NMOS) which is inserted in the HIPTSCR (HINTSCR) structure. So, by adding this bypass diode $Dn2$ ($Dp2$), the trigger voltage of the HIPTSCR (HINTSCR) is still the same as that of the PMOS-trigger (NMOS-trigger) LVTSCR [13], but the trigger current of the HIPTSCR (HINTSCR) can be significantly increased to avoid the accidental triggering by the external noisy pulses.

By increasing the trigger current of the HIPTSCR and HINTSCR but without increasing their trigger voltage and

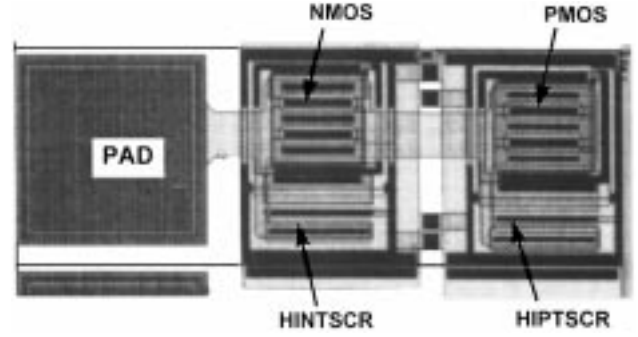


Fig. 3. A layout example of the CMOS output buffer with the HIPTSCR and HINTSCR devices.

holding voltage, these HIPTSCR and HINTSCR can still provide excellent ESD protection to the CMOS output buffer. With the higher trigger current of the HIPTSCR and HINTSCR, as well as the voltage-clamping effect of the forward-biased diodes $Dp1$ and $Dn1$, the HIPTSCR and HINTSCR can be guaranteed to be off when the CMOS IC is in its normal operating conditions even if there are the overshooting or undershooting noisy pulses attaching to the output pin.

This HIPTSCR (HINTSCR) can be merged with the output PMOS (NMOS) in the layout to save layout area as shown in Fig. 2(a) and (b). A merged layout example of the CMOS output buffer with the HIPTSCR and HINTSCR including latchup guard rings in a $0.6\text{-}\mu\text{m}$ CMOS process is shown in Fig. 3. In Fig. 3, the output PMOS has a dimension (W/L) of $312/1.0$ ($\mu\text{m}/\mu\text{m}$) and the output NMOS has a dimension of $300/1.0$. The device dimension of the short-channel PMOS (NMOS) inserted in the HIPTSCR (HINTSCR) is $60/0.8$. The layout area of the HIPTSCR (HINTSCR) is only $60 \times 37.6 \mu\text{m}^2$.

C. Circuit Operating Principles

1) *CMOS Normal-Operating Conditions:* In CMOS normal operations, the VDD is biased at 3 V for low-voltage application and the VSS is grounded. Under this condition, the HIPTSCR and HINTSCR are kept off due to the gates of the inserted short-channel PMOS and NMOS are connected to their sources. The CMOS output buffer is controlled by the pre-buffer circuits to drive/sink current to/from the external output load.

The diodes $Dp1$ and $Dn1$ contribute a voltage-level clamping effect on the output pad. The $Dp1$ ($Dn1$) clamps the high-level (low-level) voltage of the output signal to about $VDD+0.6\text{ V}$ ($VSS-0.6\text{ V}$). Thus, the voltage level of output signals on the output pad is clamped between about 3.6 and -0.6 V in the normal CMOS operations with 3-V VDD and 0-V VSS. If an unexpected noisy pulse happens to the output pad, the overshooting or undershooting voltage/current can be first clamped by the diodes $Dp1$ and $Dn1$. The HIPTSCR and HINTSCR with the higher trigger current have an enough noise margin, so they are not triggered on by the external noisy pulse under the clamping guard of the diodes $Dp1$ and $Dn1$.

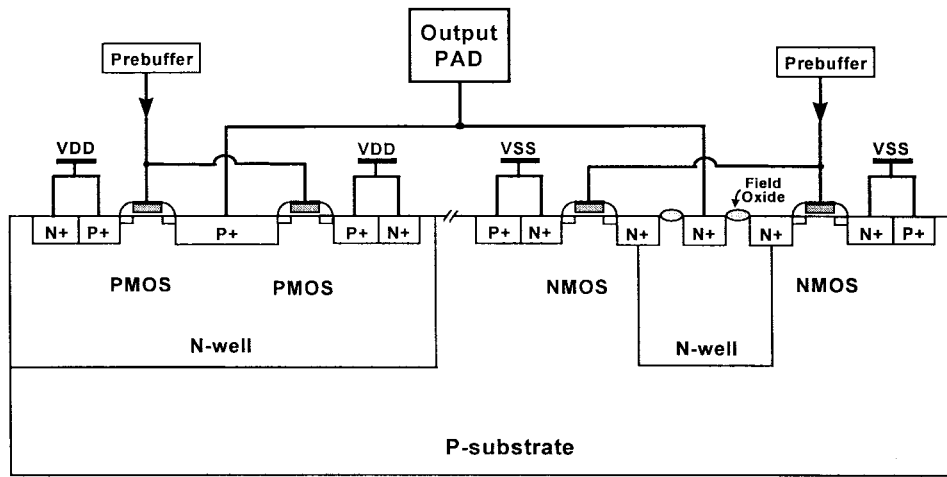


Fig. 4. The schematic cross-sectional view of a modified CMOS output buffer with the N-well resistor for ESD protection [23].

2) *ESD-Stress Conditions*: When a PS-mode (ND-mode) ESD event occurs at the output pad with the relatively grounded VSS (VDD) pin, the positive (negative) ESD voltage is diverted to the anode (cathode) of the HINTSCR (HIPTSCR), and then to the drain of the inserted short-channel NMOS (PMOS). As the drain voltage is high (low) enough, the inserted short-channel NMOS (PMOS) is first turned on by means of drain snapback breakdown and leads to the self-regeneration of latchup in the HINTSCR (HIPTSCR) [13]. Once latchup happens in the HINTSCR (HIPTSCR), a path with very low impedance from the output pad to VSS (VDD) is created. Then, the ESD current is mainly discharged through the HINTSCR (HIPTSCR). The positive (negative) ESD voltage on the output pad is clamped to near the holding voltage about 1–2 V (–1–2 V) of the HINTSCR (HIPTSCR), so the output transistors can be effectively protected. To guarantee that the HINTSCR (HIPTSCR) is turned on before the output NMOS (PMOS) breaks down, the channel length of the inserted NMOS (PMOS) is designed shorter than that of the output NMOS (PMOS) [10]–[13].

In the NS-mode (PD-mode) ESD event, the parasitic diode D_{n1} (D_{p1}) in the output NMOS (PMOS) is forward turned on to bypass ESD current. The negative (positive) ESD voltage on the pad is clamped by the forward-biased D_{n1} (D_{p1}) to about –0.6 V (+0.6 V). The diodes D_{n1} and D_{p1} in the forward-biased condition can perform high ESD protection for the output transistors.

III. EXPERIMENTAL RESULTS

One set of testkeys fabricated by a 0.6- μm CMOS technology with LDD and polycide processes is measured and tested. The layout spacing from the drain contact to the poly-gate edge in the output transistors of CMOS output buffers is kept as 5 μm for better ESD consideration. A modified CMOS output buffer with the N-well resistor to improve ESD protection, as reported in [23], is also fabricated as a comparing reference. The device width/length in the output PMOS (NMOS) of the modified CMOS output buffer is 300/1.0 (200/1.0) $\mu\text{m}/\mu\text{m}$. The schematic cross-sectional view of the modified CMOS output buffer with the N-well resistor is shown in Fig. 4, where

the drain of the output NMOS is connected to the output pad through an N-well structure [23].

A. Device I – V Characteristics

1) *The HINTSCR*: The I – V characteristics of the HINTSCR and the output NMOS in the CMOS output buffer are independently measured by a TEKTRONIX Curve Tracers 370A. The snapback I – V curve of the output NMOS with a channel length of 1.0 μm is measured in Fig. 5(a) by applying a positive voltage to the drain of the output NMOS while its gate and source are grounded. In Fig. 5(a), the snapback trigger voltage (current) of the output NMOS is 13.7 V (4.76 mA) and the snapback holding voltage (current) is 9.78 V (5.42 mA). The I – V curve of the NMOS-trigger LVTSCR without the bypass diode D_{p2} is shown in Fig. 5(b). The NMOS-trigger LVTSCR in Fig. 5(b) has only one trigger point, where the trigger voltage (current) is 12.94 V (12.3 mA). The I – V curve of the HINTSCR with the bypass diode D_{p2} is shown in Fig. 5(c). The channel length of the NMOS inserted into the HINTSCR (or the NMOS-trigger LVTSCR) is 0.8 μm . In Fig. 5(c), the HINTSCR has two trigger points in its I – V characteristics. The first trigger point is due to the drain snapback breakdown of the inserted NMOS. The first trigger voltage (current) is 11.6 V (2.0 mA). Due to the presence of the bypass diode D_{p2} , there is a buffer region in the I – V characteristics [marked as “A” in Fig. 5(c)] before the lateral SCR in the HINTSCR is triggered on. The presence of this region A is due to the snapback region of the inserted NMOS and the bypass diode D_{p2} . As the applied current is still increased, the lateral SCR in the HINTSCR will be finally triggered on. So, there is the second trigger point in the I – V curve of Fig. 5(c). The measured second trigger current (voltage) in the HINTSCR is as high as 218.5 mA (9.06 V). After the second trigger point, the I – V curve enters into the latchup holding region [marked as “B” in Fig. 5(c)], which is due to the latching action of the lateral SCR structure in the HINTSCR. The minimum holding voltage (current) of the region B is as low as 1.34 V (12.5 mA). In the region A, the HINTSCR can be safely operated in this snapback region without causing any damage. With this buffer region A, the

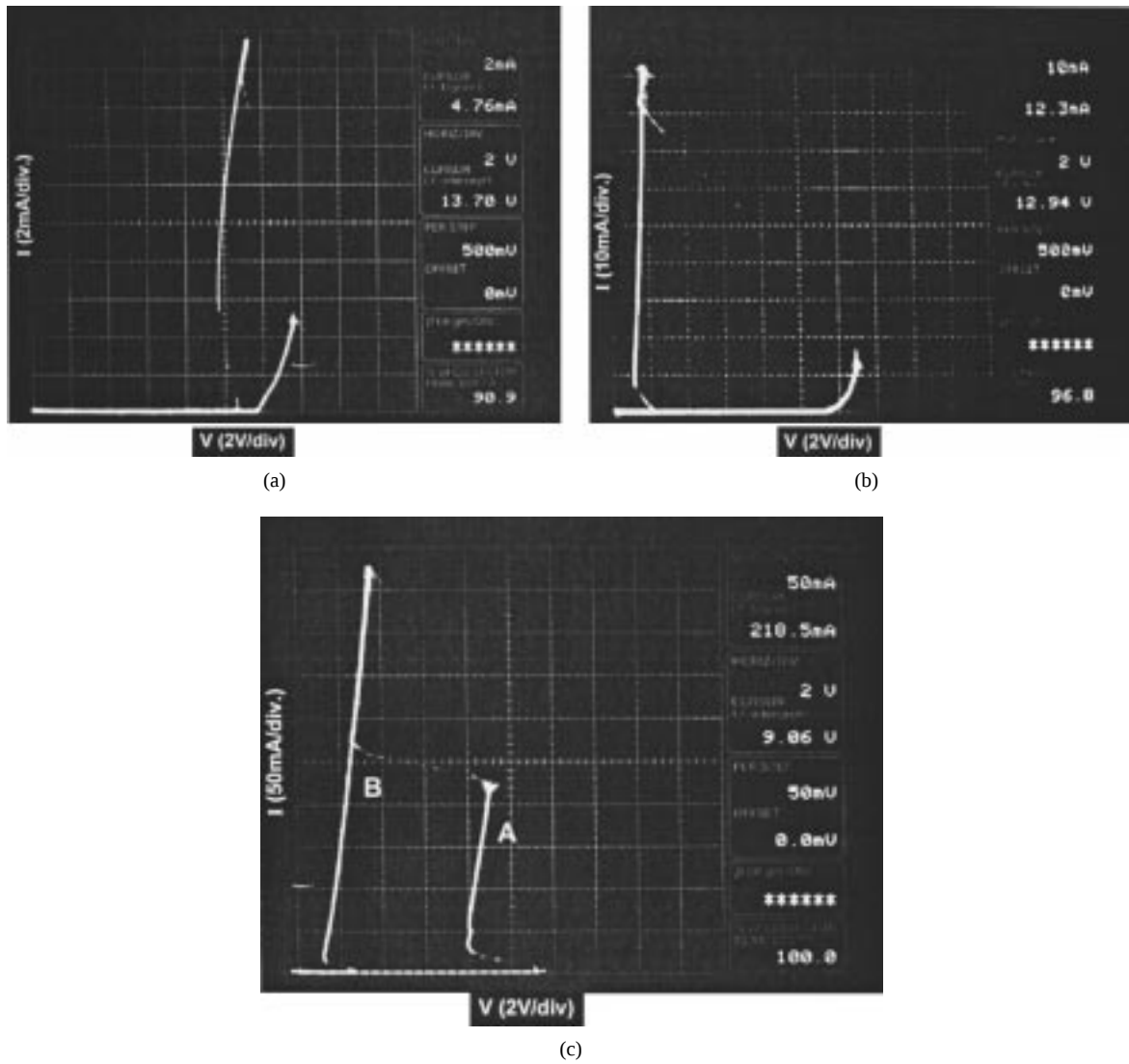


Fig. 5. The snapback I - V characteristics of (a) the output NMOS device; (b) the NMOS-trigger LVTSCR device without the bypass diode D_{p2} ; (c) the HINTSCR device with the bypass diode D_{p2} .

HINTSCR is not triggered on by the external noisy pulses, but it can be triggered on by the ESD pulses.

Comparing the I - V curves between Fig. 5(a) and (c), it can be guaranteed that the HINTSCR (with the first trigger voltage of 11.6 V) can be turned on before the output NMOS breaks down (with a breakdown voltage of 13.7 V) under the PS-mode ESD-stress condition. Thus, the HINTSCR can effectively protect the output NMOS against ESD damage. The holding voltage of the HINTSCR is still as low as that of an LVTSCR, but the trigger current (218.5 mA) of the HINTSCR with the bypass diode D_{p2} is much higher than that (12.3 mA) of the LVTSCR without the bypass diode D_{p2} . By this modified design on the device structure in Fig. 2(b), the HINTSCR can provide the CMOS output buffer with the same ESD protection as that of an LVTSCR. But, it is not triggered on by the external noisy pulses on the output pad when the CMOS output buffer is under its normal operating conditions.

2) *The HIPTSCR*: The turn-on characteristics of the HIPTSCR and the output PMOS are also measured and compared. The snapback I - V curve of the output PMOS

with a channel length of $1.0\ \mu\text{m}$ is measured in Fig. 6(a) by applying a negative voltage to the drain of the output PMOS while its gate and source are grounded. In Fig. 6(a), the snapback trigger voltage (current) of the output PMOS is $-15.62\ \text{V}$ ($-15.85\ \text{mA}$) and the snapback holding voltage (current) is $-13.84\ \text{V}$ ($-13.9\ \text{mA}$). The I - V curve of the a PMOS-trigger LVTSCR without the bypass diode D_{n2} is shown in Fig. 6(b). The PMOS-trigger LVTSCR in Fig. 6(b) has only one trigger point, where the trigger voltage (current) is $-12.92\ \text{V}$ ($-4.7\ \text{mA}$). The I - V curve of the HIPTSCR with the bypass diode D_{n2} is shown in Fig. 6(c). The channel length of the PMOS inserted into the HIPTSCR (or the PMOS-trigger LVTSCR) is $0.8\ \mu\text{m}$. In Fig. 6(c), the HIPTSCR also has two trigger points in its I - V characteristics. The first trigger point is due to the drain snapback breakdown of the inserted PMOS. The first trigger voltage (current) is $-13.42\ \text{V}$ ($-15\ \text{mA}$). Due to the presence of the bypass diode D_{n2} , there is a buffer region in the I - V characteristics [marked as “C” in Fig. 6(c)] before the lateral SCR in the HIPTSCR is triggered on. The presence of this region C is

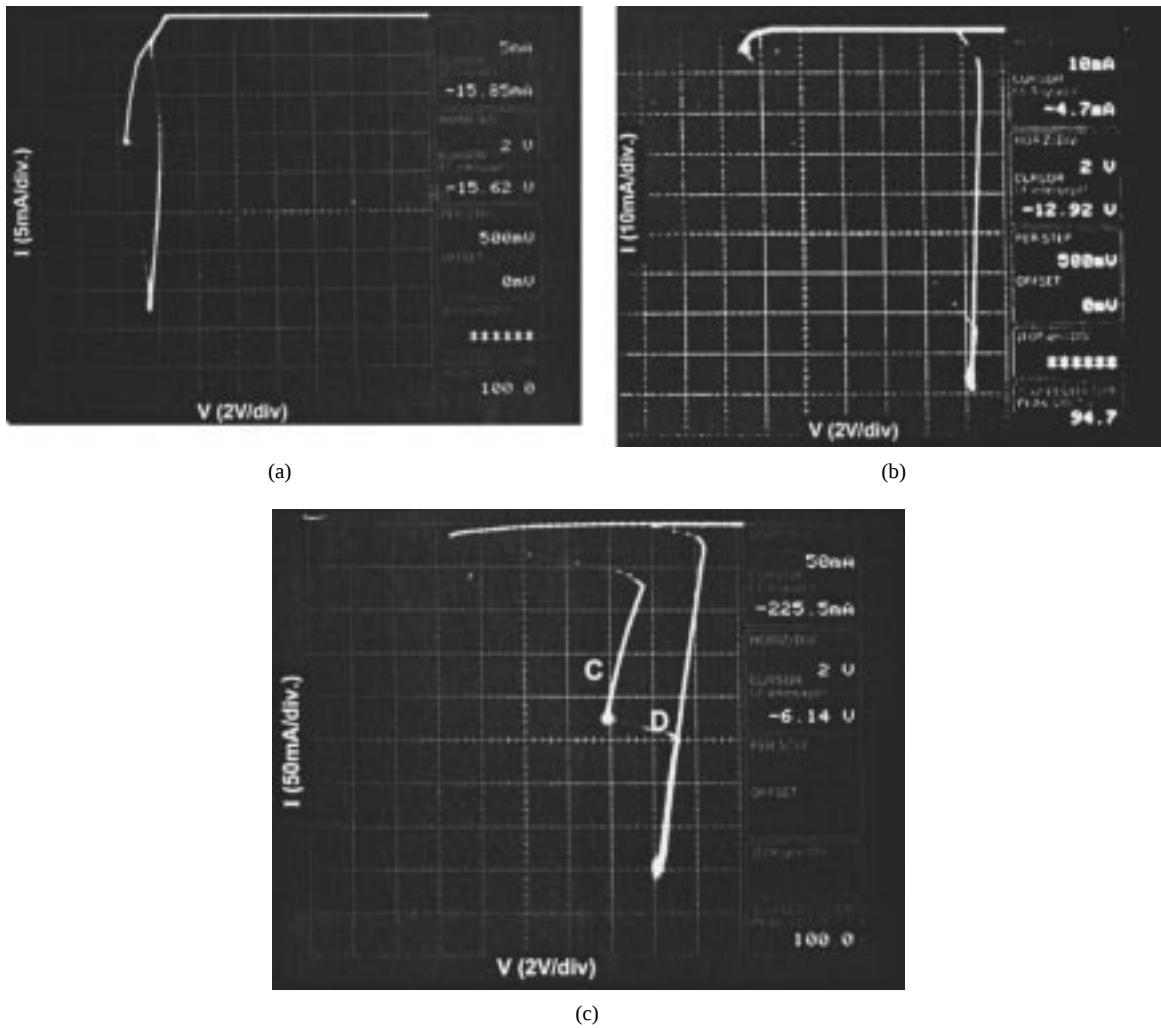


Fig. 6. The snapback I - V characteristics of (a) the output PMOS device; (b) the PMOS-trigger LVTSCR device without the bypass diode $Dn2$; (c) the HIPTSCR device with the bypass diode $Dn2$.

owing to the bypass diode $Dn2$ and the inserted PMOS in the HIPTSCR device structure. As the applied negative current is still increased, the lateral SCR in the HIPTSCR can be finally triggered on and cause a second trigger point in the I - V curve of Fig. 6(c). The second trigger current (voltage) of the HIPTSCR is as high as -225.5 mA (-6.14 V). After the second trigger point, the I - V curve enters into the latchup holding region [marked as "D" in Fig. 6(c)], which is due to the latching action of the lateral SCR structure in the HIPTSCR. The minimum holding voltage (current) in the region D is as low as -1.72 V (-13.5 mA).

In the region C of Fig. 6(c), the HIPTSCR can be safely operated in this snapback region without causing any damage. With this buffer region C, the HIPTSCR is not triggered on by the external noisy pulses, but it can be triggered on by the ESD pulses. Comparing the I - V curves between Fig. 6(a) and (c), it is guaranteed that the HIPTSCR (with the first trigger voltage of -13.42 V) can be turned on before the output PMOS breaks down (with a breakdown voltage of -15.62 V) under the ND-mode ESD-stress condition. Thus, the HIPTSCR can effectively protect the output PMOS against ESD damage. The holding voltage of the HIPTSCR

is still as low as that of an LVTSCR, but the trigger current (-225.5 mA) of the HIPTSCR with the bypass diode $Dn2$ is much higher, in the magnitude, than that (-4.7 mA) of the PMOS-trigger LVTSCR without the bypass diode $Dn2$. By using this modified design on the device structure in Fig. 2(a), the HIPTSCR can provide the CMOS output buffer with the same ESD protection as that of an LVTSCR. But, it has a much safe margin against the accidental triggering due to the external noisy pulse on the output pad while the CMOS output buffer is under its normal operating conditions.

B. Pulse-Trigger Testing

To verify the exact protection function of the HIPTSCR and HINTSCR, a voltage pulse is applied to the output pad to investigate their trigger-on behavior in the ESD-stress conditions. The experimental setup to verify the ESD-protection function of the HINTSCR is shown in Fig. 7, which is to simulate the PS-mode ESD-stress condition. A pulse generator (Hp8116A) with a rise time around 6–7 ns is applied to the output pad while the gate of the output NMOS is grounded. The gate of the output PMOS is connected to VDD, where the VDD node is floating in the PS-mode ESD-stress condition.

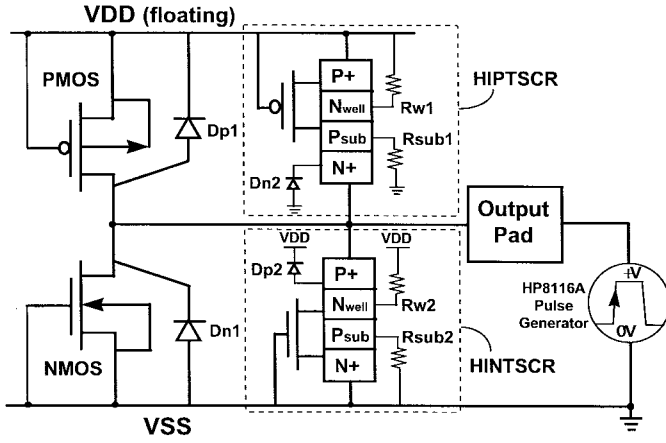


Fig. 7. An experimental setup to simulate the PS-mode ESD-stress condition and to verify the protection function of the HINTSCR.

The experimental results are shown in Fig. 8. In Fig. 8(a), a pulse-type voltage with a peak voltage of 11.6 V is applied to the output pad, but neither the output NMOS nor the HINTSCR is triggered on by such a voltage pulse. So, the voltage waveform on the output pad is not degraded as shown in Fig. 8(a). As the peak voltage of the voltage pulse is increased above 11.6 V, the HINTSCR is triggered into the operating region A of Fig. 5(c). In Fig. 8(b), it shows a degraded voltage waveform due to the turn-on of the HINTSCR in the region A. With a voltage peak of 12.25 V, the rising edge of the voltage pulse triggers the HINTSCR into its operating region A. After the rising-edge triggering, the peak voltage is clamped at about 8.3 V due to the operating region A in Fig. 5(c). In this condition, the lateral SCR in the HINTSCR is still not triggered on. If the peak voltage of the applied voltage pulse is more increased, the HINTSCR will be triggered into its operating region B. When a voltage pulse with a peak voltage of 13.5 V is applied to the output pad, the lateral SCR structure in the HINTSCR can be triggered on and causes a very low impedance path between the output pad and the ground. This very low impedance path due to the turn on of the lateral SCR causes a serious degradation on the voltage waveform of the applied voltage pulse. The degraded voltage waveform is shown in Fig. 8(c), where the voltage peak is clamped at as low as 2.37 V which is close to the holding voltage of the lateral SCR in the HINTSCR. The sharp variation of the rising edge in Fig. 8(c) is zoomed in Fig. 8(d). In Fig. 8(d), the rising peak is not as high as the peak voltage of 13.5 V, which is due to the turn on of the HINTSCR and the finite bandwidth of the oscilloscope. In summary, when a voltage pulse with a peak voltage higher than 11.6 V attaches the output pad, the HINTSCR is first triggered into its operating region A to clamp the voltage pulse. If the voltage peak has a much higher voltage peak such as higher than 13.5 V, the HINTSCR is triggered into its operating region B to clamp the voltage level on the output pad as low as its holding voltage. Thus, the output buffer can be effectively protected by this HINTSCR.

The experimental setup to verify the ESD-protection function of the HIPTSCR is shown in Fig. 9, which is to simulate

the ND-mode ESD-stress condition. A pulse generator with a fall time around 6–7 ns is applied to the output pad and the VDD is grounded. The experimental results are shown in Fig. 10. In Fig. 10(a), a negative voltage pulse with a negative peak voltage of -13.0 V is applied to the output pad, but neither the output PMOS nor the HIPTSCR is triggered on by such a voltage pulse. So, the voltage waveform on the output pad is not degraded as shown in Fig. 10(a). As the peak voltage of the applied voltage pulse is lowered than -13 V, the HIPTSCR is triggered on to clamp the negative voltage peak on the output pad. As the HIPTSCR is triggered on, the voltage waveform on the output pad will be degraded. A typical degraded voltage waveform due to the turn-on of the HIPTSCR is shown in Fig. 10(b), in which a negative voltage pulse with the voltage peak of -14 V is applied to the output pad. Due to the different operating regions C and D in the I - V characteristics of the HIPTSCR, there are two states in the degraded voltage waveform in Fig. 10(b). The first state with a voltage level about -6.2 V is corresponding to the operating region C of Fig. 6(c). The second state with a voltage level about -2.7 V is corresponding to the operating region D of Fig. 6(c). This verifies the protection function of the HIPTSCR to effectively protect the output buffer in the ND-mode ESD stress condition.

C. Noise Margin

The bypass diode $Dn2$ ($Dp2$), inserted into the HIPTSCR (HINTSCR) device structure, is used to increase the noise margin against the accidental triggering while the noisy pulse attaches to the output pin. To investigate the efficiency of the bypass diode $Dp2$ in the HINTSCR, an experimental setup is shown in Fig. 11. A positive voltage pulse with a low-level voltage of 3 V generated from a pulse generator is used to simulate an overshooting noise on the output pad while the IC is in its normal operating conditions with the power supply of 3-V VDD and 0-V VSS. In Fig. 11, the output NMOS is off but the output PMOS is on by its gate grounded to provide a 3-V voltage to the output pad. If the HINTSCR is triggered on by the overshooting noise, the voltage level on the output pad will be dropped down to VSS due to the very low turn-on resistance of the HINTSCR. But, if the HINTSCR is not triggered on by the overshooting noise, the voltage on the output pad will be remained at 3 V after the transition of the overshooting noise. The diode $Dp1$ is expected to clamp the overshooting voltage on the output pad, and the diode $Dp2$ is expected to avoid the HINTSCR being triggered on by the overshooting voltage pulse. The measured results are shown in Fig. 12. The voltage waveform in Fig. 12(a) is the original overshooting voltage pulse generated from a pulse generator, which has a low-level voltage of 3 V and a high-level voltage of up to 15 V with a pulse width of 250 μ s. As this overshooting voltage pulse is applied to the output pad as shown in Fig. 11, the voltage waveform on the output pad is monitored and shown in Fig. 12(b). In Fig. 12(b), the 15-V high-level voltage is clamped to about only 3.5 V by the diode $Dp1$. After the triggering of the 15-V overshooting

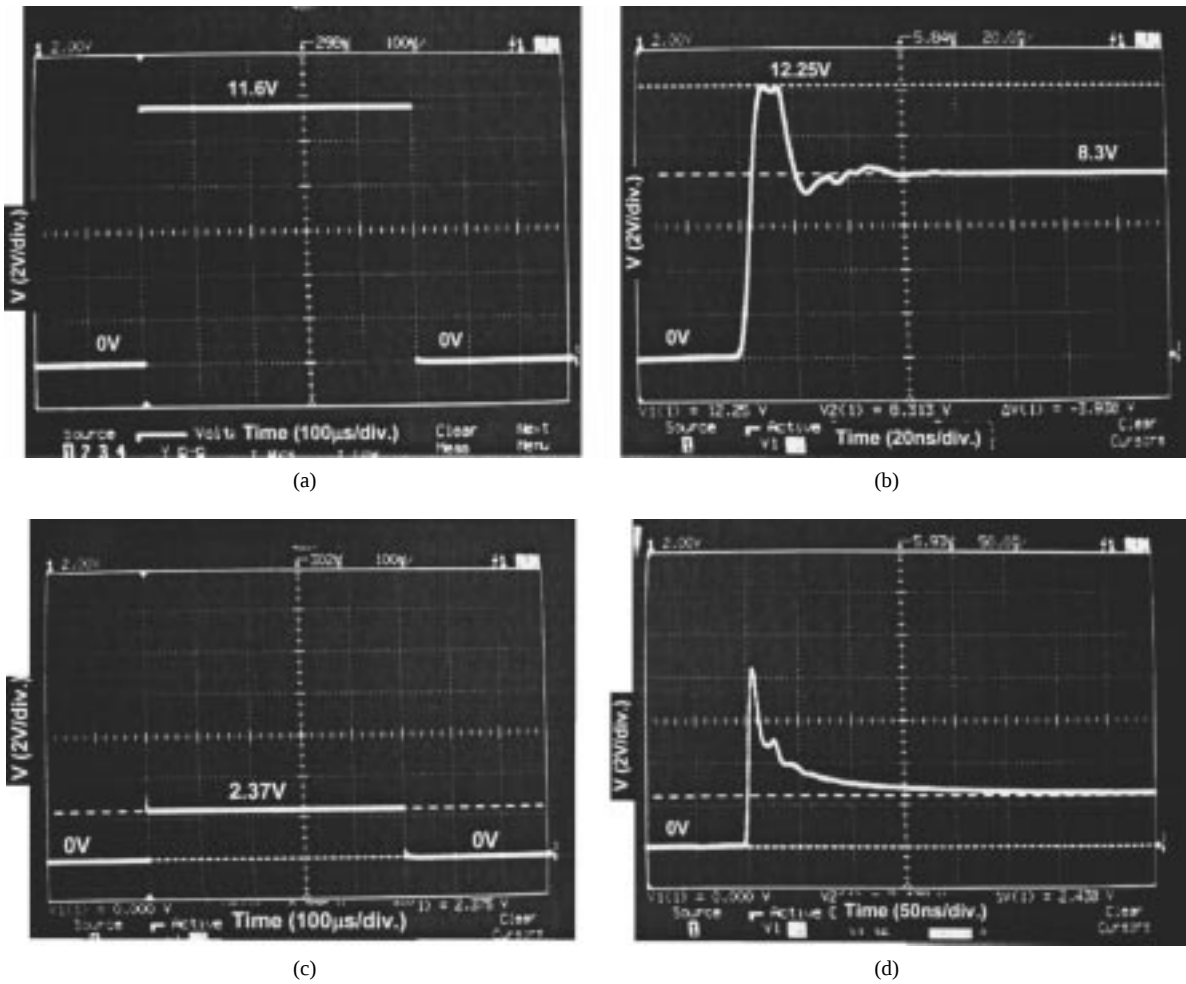


Fig. 8. The voltage waveform on the output pad due to the triggering of a positive voltage pulse with a peak voltage of (a) 11.6 V; (b) 12.25 V; and (c) 13.5 V. (d) The zoomed-in rising edge of the positive voltage pulse in (c).

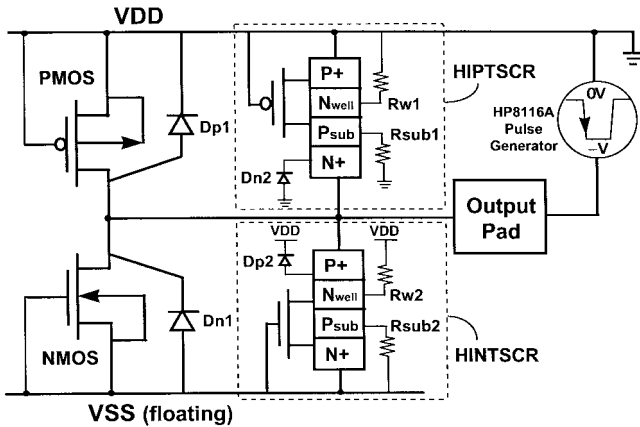
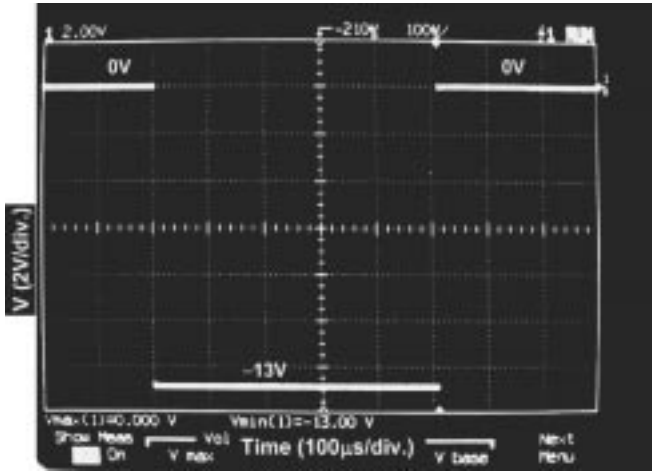


Fig. 9. An experimental setup to simulate the ND-mode ESD-stress condition and to verify the protection function of the HIPTSCR.

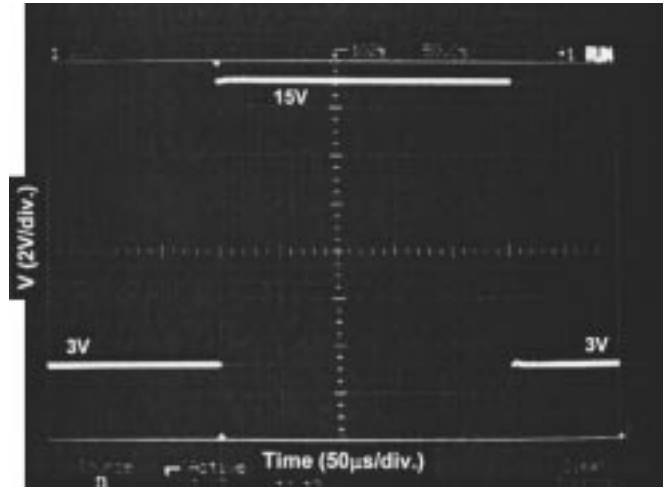
voltage pulse on the output pad, the voltage waveform on the output pad is still kept at 3 V without any degradation. The HIPTSCR has been verified to still remain off because the bypass diode D_{p2} in the HIPTSCR provides a high noise margin to the overshooting noisy pulse.

Similarly, to investigate the efficiency of the bypass diode D_{n2} in the HIPTSCR, an experimental setup is shown in

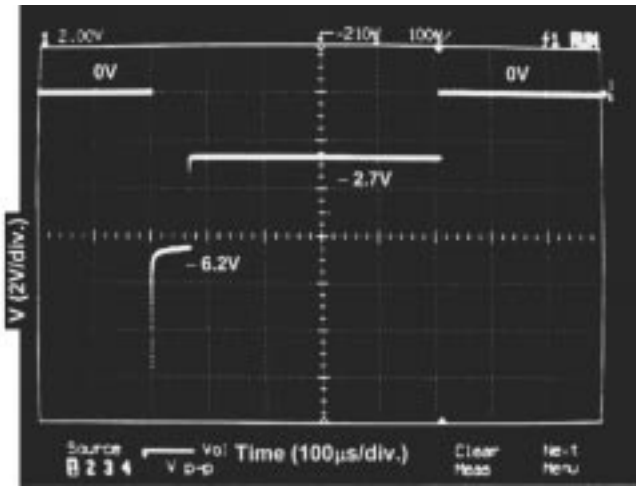
Fig. 13. An undershooting voltage pulse with a high-level voltage of 0 V and a negative low-level voltage is applied to the output pad, while the output PMOS is off but the output NMOS is on to provide a 0-V voltage to the output pad. If this undershooting voltage pulse can accidentally trigger on the HIPTSCR, the voltage on the output pad will be raised up to VDD due to the very low turn-on resistance of the HIPTSCR. By monitoring the voltage waveform on the output pad, we can verify whether the HIPTSCR is triggered on by the undershooting voltage pulse or not. The measured results are shown in Fig. 14. The original undershooting voltage pulse generated from the pulse generator is shown in Fig. 14(a), where the undershooting voltage pulse has a low-level voltage of -12 V. As this -12 V undershooting voltage pulse is applied to the output pad as shown in Fig. 13, the voltage waveform on the output pad is degraded as shown in Fig. 14(b). The low-level voltage of -12 V in the undershooting voltage pulse is clamped by the diode D_{n1} to only about -0.72 V. After the transition of the undershooting voltage pulse, the voltage on the output pad is remained at 0 V. So, the HIPTSCR is not triggered on by the applied -12 V undershooting voltage pulse. This has verified the efficiency of the diode D_{n2} in the HIPTSCR with a high noise margin to the negative noisy pulse.



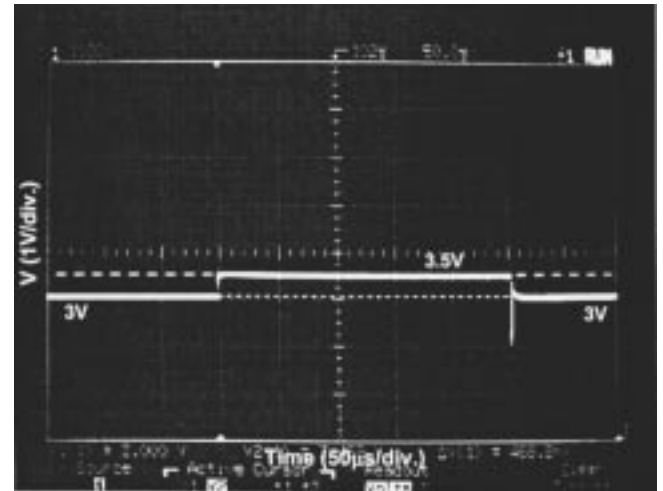
(a)



(a)



(b)



(b)

Fig. 10. The voltage waveform on the output pad due to the triggering of a negative voltage pulse with a peak voltage of (a) -13 V; (b) -14 V.

Fig. 12. (a) The applied voltage pulse (generated from a pulse generator) with a peak voltage of 15 V and a pulse width of 250 μ s to simulate an overshooting noise pulse on the output pad. (b) The clamped voltage waveform on the output pad while the overshooting voltage pulse in (a) is applied to the output pad.

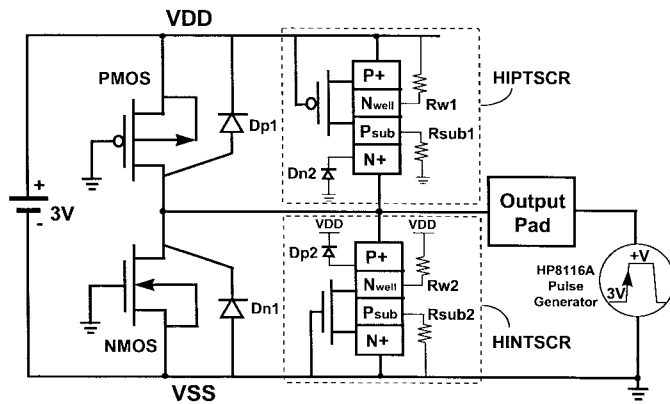


Fig. 11. An experimental setup to investigate the noise margin of the HIPTSCR in the output overshooting condition with a 3 -V V_{DD} and a 0 -V V_{SS} .

Through above verification, the proposed HIPTSCR and HINTSCR have the noise margin greater than $V_{DD}+12$ V and $V_{SS}-12$ V to avoid the accidental triggering due to the overshooting or undershooting voltage pulses on the output pad. If the area of the diode $Dn2$ ($Dp2$) in the HIPTSCR (HINTSCR) device is increased, the second trigger

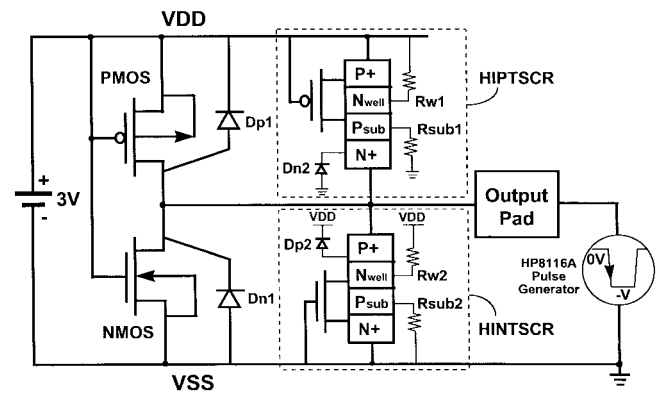


Fig. 13. An experimental setup to investigate the noise margin of the HIPTSCR in the output undershooting condition with a 3 -V V_{DD} and a 0 -V V_{SS} .

current and the noise margin of the HIPTSCR (HINTSCR) can be further increased. A CMOS output buffer protected by both the NMOS-trigger LVTSCR and the PMOS-trigger

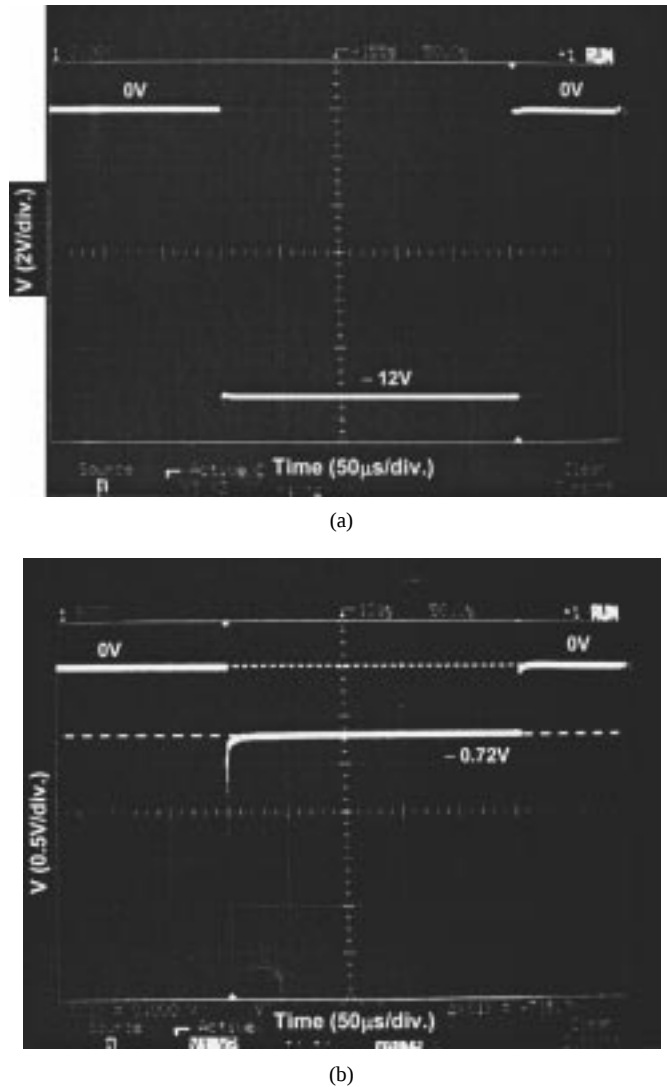


Fig. 14. (a) The applied voltage pulse (generated from a pulse generator) with a peak voltage of -12 V and a pulse width of $250\text{ }\mu\text{s}$ to simulate an undershooting noise pulse on the output pad. (b) The clamped voltage waveform on the output pad while the undershooting voltage pulse in (a) is applied to the output pad.

LVTSCR [12] is also fabricated in the same process. The same experimental setup in Fig. 11 (Fig. 13) is also used to investigate the noise margin of the NMOS-trigger (PMOS-trigger) LVTSCR. Without the bypass diode $Dp2$ ($Dn2$), the NMOS-trigger (PMOS-trigger) LVTSCR has a noise margin of only $VDD+3V$ ($VSS-3V$). With such low noise margin, the NMOS-trigger (PMOS-trigger) LVTSCR is sensitive to the overshooting or undershooting noisy pulses when the IC is operated in the noisy environment. How much the noise margin is needed which is strongly dependent on the application environments of the CMOS IC's. However, the CMOS output buffer protected by the HIPTSCR and HINTSCR has been shown in this paper with an enough noise margin against the overshooting and undershooting noise pulses for general applications.

D. ESD Testing

The ESD-stress voltage is set to begin with the initial voltage of 1000 V and increase up to 8000 V in an Human-

Body-Model (HBM) ESD testing. The ESD tester used in this investigation is the ZAPMASTER produced by KeyTek Instrument Corp. [28]. The four modes of ESD stresses are applied to the testchip, and the testing results are listed in Table I. The CMOS output buffer with the N-well resistor [23] is tested as a reference. The testchip is also investigated in the Machine-Model (MM) ESD events, and the results are also listed in Table I. The failure criterion is defined as the leakage current of the CMOS output buffer in its off state becomes above $1\text{ }\mu\text{A}$ under 5-V voltage bias after ESD stress. The lowest (in absolute value) ESD sustaining voltage among the four modes of ESD stresses on the same output pin is defined as the ESD failure threshold of the output pin. The results in Table I show that the CMOS output buffer with the HIPTSCR and HINTSCR can provide an ESD failure threshold of 4000 (700) V in the HBM (MM) ESD testing. The layout area for the HIPTSCR and HINTSCR are both $60 \times 37.6\text{ }\mu\text{m}^2$ only. The modified CMOS output buffer, even with the N-well resistor and a larger layout area, can sustain the HBM (MM) ESD level of only 1250 (100) V . This verifies the excellent ESD protection performance of the HIPTSCR and HINTSCR devices in submicron CMOS technologies.

The ESD testing results, as shown in Table I, are the worst-case physical limitation of the ESD sustaining level of the CMOS output buffer which is protected by the N-well resistor or the HIPTSCR/HINTSCR. The VDD (VSS) pad for each CMOS output buffer in this testchip is drawn with a separated pad, which is not shared by other CMOS output buffers in the same testchip. Because of the presence of the $Dp1$ ($Dn1$) diode in the output PMOS (NMOS), the PS-mode (ND-mode) ESD energy on the output pad may be shared into the VDD (VSS) line. In the VLSI chip, the VDD and VSS power lines surrounding the whole chip can generate a large parasitic capacitor between the VDD and VSS lines. This VDD-to-VSS parasitic capacitor will absorb some (dependent on the capacitance of the capacitor) of the ESD energy from the output pad to the VDD (VSS) line in the PS-mode (ND-mode) ESD-stress condition. If the VDD and VSS pads are all commonly connected together for all the CMOS output buffers in the testchip, the VDD-to-VSS parasitic capacitor will absorb the ESD energy and cause an ESD sustaining level higher than the physical limitation. By using the separated VDD and VSS pads for each CMOS output buffer in the especially designed testchip, the ESD robustness of the CMOS output buffer protected by the HIPTSCR/ HINTSCR or the N-well resistor can be actually investigated and listed in Table I.

E. Temperature Effect

The temperature dependence on the first trigger point (voltage/current) and the holding voltage/current of the HIPTSCR (HINTSCR) is similar to that of the LVTSCR1 (LVTSCR2) in [13]. The first trigger voltage/current are less dependent to the temperature because the trigger is owing to the drain breakdown on the inserted PMOS (NMOS) in the HIPTSCR (HINTSCR). The temperature dependence on the VDD-to-VSS latchup issue in the CMOS output buffer protected by the HIPTSCR and HINTSCR is still the same as that in [13]. The higher temperature leads to a higher holding voltage which

TABLE I
COMPARISON OF THE PHYSICAL LIMITATION OF ESD ROBUSTNESS WITH A MODIFIED CMOS OUTPUT BUFFER

	Modified CMOS Output Buffer with N-well Resistor [23]				This Work			
	PMOS (300/1.0)		NMOS (200/1.0)		HIPTSCR + PMOS (312/1.0)		HINTSCR + NMOS (300/1.0)	
Layout Area ($\mu\text{m} \times \mu\text{m}$)	112.6 X 52		136.2 X 52		114.4 X 86 (60 X 37.6 for HIPTSCR)		117.4 X 86 (60 X 37.6 for HINTSCR)	
ESD-Stress Condition	PD-Mode	ND-Mode	PS-Mode	NS-Mode	PD-Mode	ND-Mode	PS-Mode	NS-Mode
HBM ESD Sustain Voltage (V)	7250	-1750	1250	-4500	above 8000	-5500	4000	above -8000
MM ESD Sustain Voltage (V)	600	-150	100	-400	above 1000	-900	700	above -1000

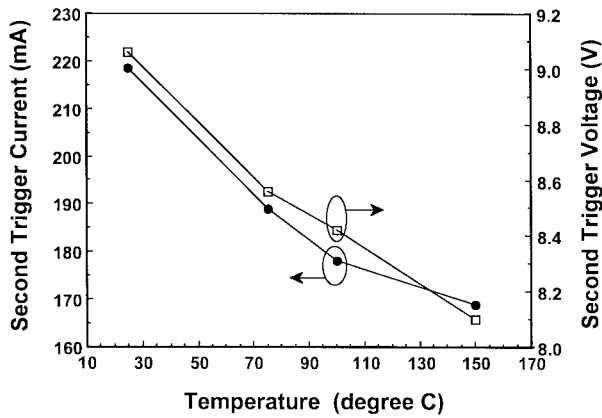


Fig. 15. The temperature dependence on the second trigger current and voltage of the HINTSCR device.

is much greater than VDD, because the de-coupling effect among the latchup guardrings is increased by the temperature [13]. The CMOS output buffer protected by the HIPTSCR and HINTSCR is guaranteed to be free from the VDD-to-VSS latchup issue, because the VDD-to-VSS holding voltage in the output circuit is greater than VDD.

But the second trigger voltage/current of the HIPTSCR and HINTSCR are slightly dependent on the temperature. A *ThermoChuck* system [29] with a high temperature range up to 200 °C and a temperature accuracy of ± 0.5 °C is used to find the temperature dependence of the second trigger point in the HIPTSCR and HINTSCR. The temperature dependence on the second trigger current and voltage of the HINTSCR is measured and shown in Fig. 15, whereas the HIPTSCR has similar temperature characteristics. As shown in Fig. 15, the second trigger current (voltage) in the HINTSCR is degraded to 169 mA (8.1 V) while the temperature is increased up to 150 °C. With a 169-mA trigger current at the temperature of 150 °C, the HINTSCR device still has an enough noise margin to the overshooting or undershooting noise pulses, because the diode $Dp1$ ($Dn1$) in the output PMOS (NMOS) takes more of the overshooting/undershooting current away from the output pad.

IV. CONCLUSION

An area-efficient output ESD protection design by using the HIPTSCR and HINTSCR devices has been practically verified

in a 0.6- μm CMOS process. The accidental triggering on the LVTSCR device, due to the overshooting or undershooting noise pulses on the output pad, has been successfully overcome by increasing the trigger current of the LVTSCR device. A bypass diode is inserted into the device structure of an NMOS-trigger lateral SCR to form an HINTSCR device with a trigger current of up to 218.5 mA. A bypass diode is also inserted into the device structure of a PMOS-trigger lateral SCR to form an HIPTSCR device with a trigger current of up to 225.5 mA. With such a high trigger current, these HIPTSCR and HINTSCR devices have been experimentally confirmed with a noise margin greater than ± 12 V against the accidental triggering due to the overshooting/undershooting noise pulses in the normal operating conditions. Because the trigger voltage of the HINTSCR (HIPTSCR) is still remained as low as that of an LVTSCR, the HIPTSCR and HINTSCR can be triggered on before the output transistors break down in the ESD-stress conditions. From the experimental results, these HIPTSCR and HINTSCR can effectively provide the CMOS output buffer with a 4000-V (700-V) HBM (MM) ESD robustness in a small layout area of only $60 \times 37.6 \mu\text{m}^2$. So, a practical solution has been proposed and verified in this paper to safely apply the advantages of the LVTSCR device for ESD protection in submicron CMOS IC's. The trigger current and the noise margin of the HIPTSCR (HINTSCR) can be also adjusted by changing the layout area of the inserted bypass diode in the HIPTSCR (HINTSCR) device structure. Without any extra process modification, the design and fabrication of the HIPTSCR and HINTSCR devices can be fully process-compatible to general CMOS and BiCMOS technologies.

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