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How to safely apply the LVTSCR for CMOS whole-chip ESD protection without being accidentally triggered on☆

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Abstract

In this paper, the lateral SCR devices used in CMOS on-chip ESD protection circuits are reviewed. Such SCR devices have been found to be accidentally triggered on by noise pulses when IC's are operated in the normal operating condition. A stacked design is therefore proposed to safely apply the LVTSCR devices for whole-chip ESD protection in CMOS IC's without causing unexpected operation errors or latchup danger. Such stacked LVTSCR's with a holding voltage greater than VDD of IC's can provide CMOS IC's with effective component-level ESD protection but without being accidentally triggered on by system-level overshooting or undershooting noise pulses. © 1999 Elsevier Science B.V. All rights reserved.

Keywords: Electrostatic discharge protection; CMOS; LVTSCR; Cascode; Stacked SCRs; Latch-up

1. Introduction

Due to the low holding voltage (~ 1 V) of the lateral SCR device, the power dissipation (Power $\cong I_{ESD} \times V_{hold}$) of the SCR device during the electrostatic discharge

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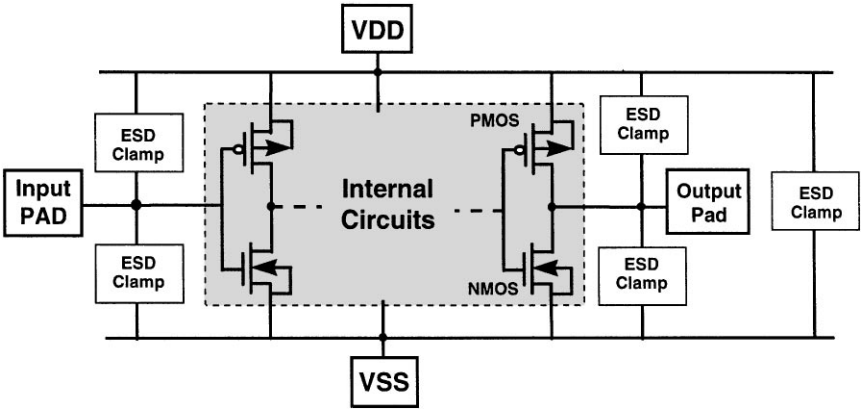


Fig. 1. General schematic for CMOS whole-chip ESD protection.

(ESD) transition is less than that of other ESD protection devices (such as the field-oxide device, thin-oxide NMOS, or diode) in CMOS technologies. Thus, the lateral SCR device can withstand very high ESD stress as compared to other ESD protection devices in CMOS technologies. For example, the holding voltage of an SCR device in a 0.35-μm bulk CMOS process is about 1 V, but the snapback holding voltage of an NMOS device in the same process is about 6 V. Therefore, the SCR device can withstand about six-times more ESD current per unit layout area than an NMOS device. Because the SCR device can sustain a much higher ESD stress within a smaller layout area, the lateral SCR devices had been used in the on-chip ESD protection circuits to protect CMOS IC's against ESD damage [1–20].

To provide effective ESD protection for a whole CMOS IC, on-chip ESD protection circuits are added around the input, output, and power pads of a CMOS IC. Because some ESD damage has been found on the internal circuits beyond the input or output ESD protection circuits [21–24], the ESD clamp circuit also has to be placed between the VDD and VSS power lines to provide whole-chip ESD protection [25–29]. The location of ESD clamp circuits in a CMOS IC to achieve whole-chip ESD protection is illustrated in Fig. 1. The lateral SCR devices had been used in input/output ESD protection circuits [1–16,18–20] and VDD-to-VSS ESD clamp circuits [17,29] to effectively protect CMOS IC's against ESD damage.

In this paper, the lateral SCR devices used in CMOS on-chip ESD protection circuits are reviewed. In addition, the latchup danger of using SCR devices in CMOS on-chip ESD protection circuits is discussed. Such SCR devices have been found to be accidentally triggered on by the noise pulses when the IC's are operated in the normal operating conditions. To overcome this problem, a stacked configuration has been proposed to apply safely the SCR devices for effective ESD protection in CMOS technology.

2. The SCR devices used in CMOS on-chip ESD protection circuits

2.1. The lateral SCR (LSCR)

The lateral SCR (LSCR) device has been used as an effective ESD protection element for input pins in submicron CMOS IC's [1–3]. The typical application example of the LSCR device in an input ESD protection circuit is shown in Fig. 2a. The device structure of the LSCR is illustrated in Fig. 2b and the I–V characteristics of the LSCR is illustrated in Fig. 2c. The LSCR has a high trigger voltage (30–50 V), which is much greater than the gate-oxide breakdown voltage of the input stages in submicron CMOS IC's. Therefore, the LSCR must be used in conjunction with the secondary protection circuit (the series resistor and the gate-grounded NMOS in Fig. 2a) to perform the overall ESD protection function to protect the input stages.

The secondary protection circuit must sustain the ESD stress before the LSCR is triggered on to bypass ESD current on the input pad. Because the LSCR is slow in triggering, the secondary protection circuit was found to be damaged by the ESD energy [3]. Therefore, the secondary protection circuit was designed with a

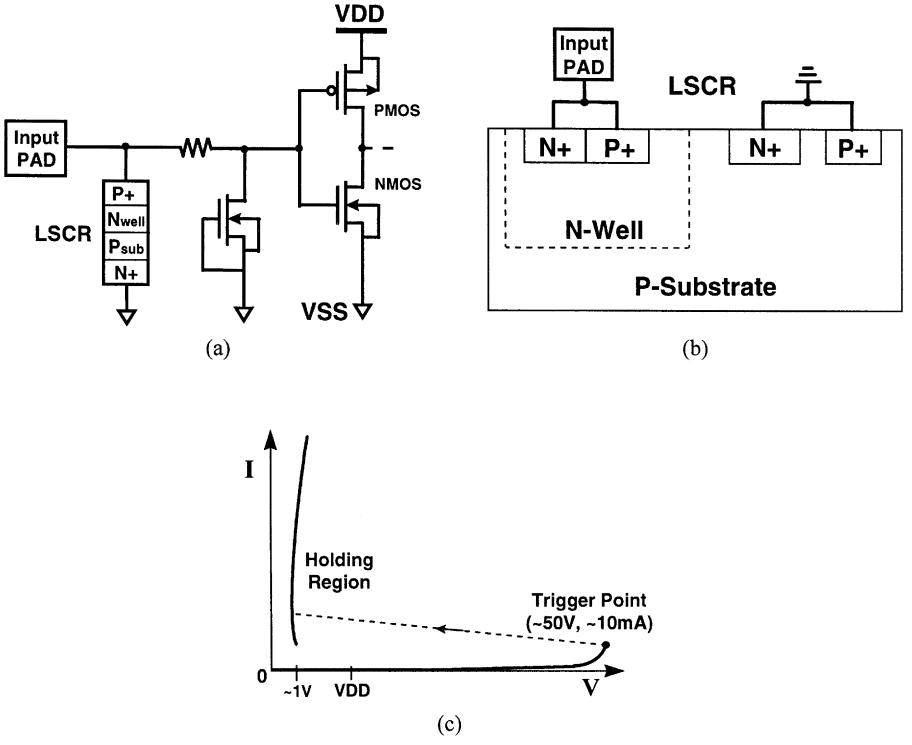


Fig. 2. (a) The input ESD protection circuit with the LSCR device, (b) the device structure of the LSCR in CMOS process, (c) the I–V characteristics of the LSCR in a 1.2-μm CMOS process [2].

considerably larger device dimension and a large series resistor to protect themselves. This secondary protection circuit with large device dimensions often occupies more layout area. If the secondary protection circuit were not properly designed, it would have caused a failure window in the ESD test, scanning from the low voltage to the high voltage. Such input ESD protection circuit was found to pass the ESD stress with low- or high-voltage level, but it failed when the ESD stress was with a middle voltage level [3]. So, the design of the secondary protection circuit with the LSCR for the overall input ESD protection circuit is somewhat critical in CMOS IC's.

2.2. The modified lateral SCR (MLSCR)

To provide more effective ESD protection for the input stages, the modified lateral SCR (MLSCR) was invented to reduce the trigger voltage of the lateral SCR [4]. With a lower trigger voltage in the MLSCR, the secondary protection circuit could have smaller device dimensions to save total layout area. An example of using the MLSCR device in an input ESD protection circuit is shown in Fig. 3a. The device structure of the MLSCR is illustrated in Fig. 3b and the I–V characteristics of the MLSCR is

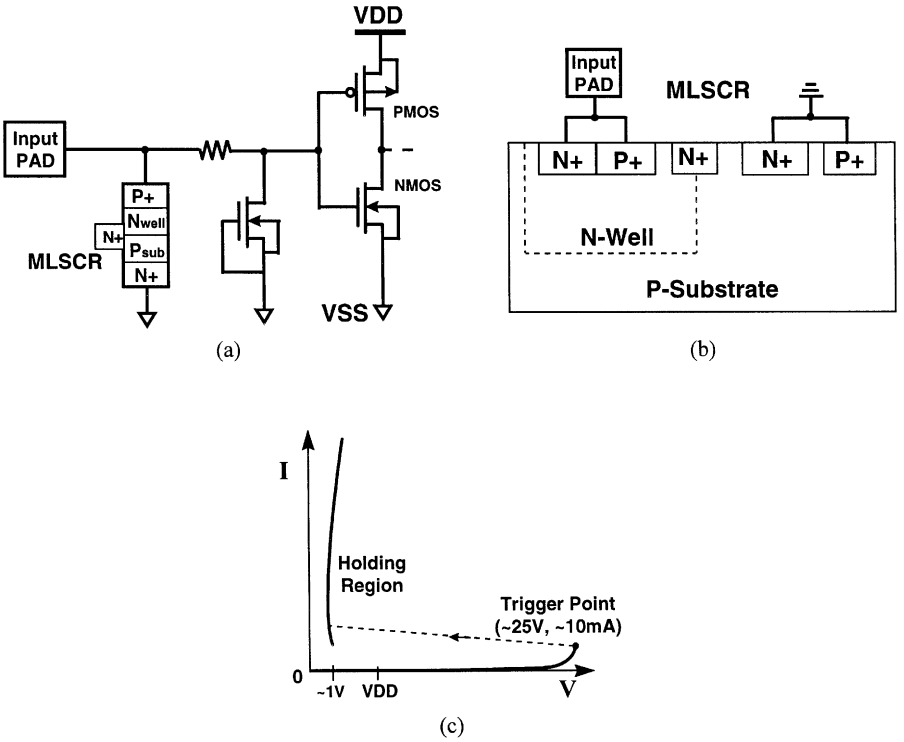


Fig. 3. (a) The input ESD protection circuit with the MLSCR device, (b) the device structure of the MLSCR in CMOS process, (c) the I–V characteristics of the MLSCR in a 1.2-μm CMOS process [4].

illustrated in Fig. 3c. The MLSCR is made by adding an N^+ diffusion across the well-substrate junction to lower the trigger voltage of the SCR device. Because the N^+ diffusion has a much higher doping concentration than the N-well, the trigger voltage of the MLSCR can be significantly lower than that of the LSCR in the same CMOS process. The trigger voltage of the MLSCR is determined by the breakdown voltage of the N^+ diffusion, which is dependent on the process technology. The LSCR was reported to have a trigger voltage of about $\sim$25 V in a 1.2-μm CMOS process [4], which is still greater than the gate-oxide breakdown voltage of the input stages in submicron CMOS IC's. Thus, the MLSCR must still be supported by a secondary protection circuit to perform the overall ESD protection function for the input stages. An unsuitable design or layout on the secondary protection circuit can still cause the ESD damage located on the secondary protection circuit rather than the MLSCR device [4].

To lower the trigger voltage of SCR device, the transient-triggering effect on the SCR device has also been studied and used to design the on-chip ESD protection circuit with multiple SCR structures [5–9].

2.3. The low-voltage triggering SCR (LVTSCR)

To effectively protect the input stages and even the output buffers in submicron CMOS IC's, the LVTSCR (low-voltage triggering SCR) device has been invented with a much lower trigger voltage [10–16]. An example of using the LVTSCR device as the output ESD protection circuit is shown in Fig. 4a. The device structure of the LVTSCR is drawn in Fig. 4b and the I–V characteristics of the LVTSCR is illustrated in Fig. 4c.

The trigger voltage of the LVTSCR is equivalent to the snapback-trigger voltage of the short-channel NMOS device, which is inserted into the lateral SCR structure, rather than the original switching voltage (about 30–50 V) of the lateral SCR device. By a suitable design, the trigger voltage of the LVTSCR can be lowered below the breakdown voltage of the output NMOS [11–16]. The trigger voltage (current) of the LVTSCR in a 0.6-μm CMOS technology is about $\sim$10 V ($\sim$10 mA). With such a low trigger voltage, the LVTSCR can provide effective ESD protection for both the input stages and the output buffers of CMOS IC's without the support of a secondary protection circuit. Therefore, the total layout area of the ESD protection circuits with the LVTSCR can be significantly reduced.

By using another method, the hot-carrier effect in the short-channel NMOS device was also applied to reduce the trigger voltage of the SCR device [17].

2.4. The gate-coupled LVTSCR

To effectively protect the thinner gate oxide in deep-submicron low-voltage CMOS IC's, the gate-coupled technique was applied to further reduce the trigger voltage of the LVTSCR [18,19]. The gate-coupled LVTSCR ESD protection circuit for input or output pads is shown in Fig. 5a. The device structure of the gate-coupled LVTSCR is illustrated in Fig. 5b and the I–V characteristics of the gate-coupled NTLSCR

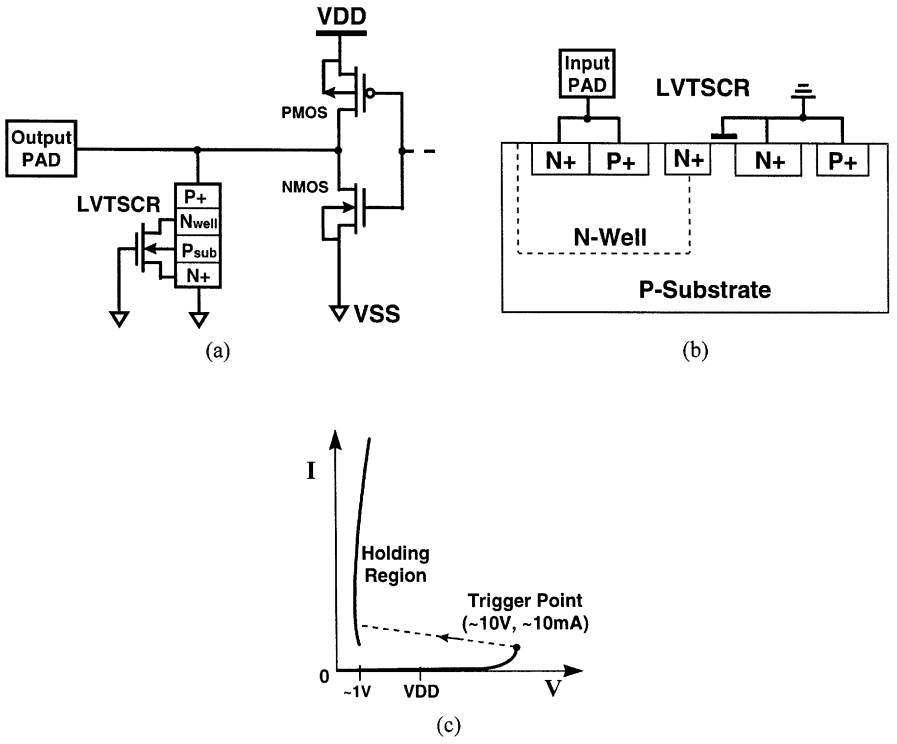


Fig. 4. (a) The output ESD protection circuit with the LVTSCR device, (b) the device structure of the LVTSCR in CMOS process, (c) the I–V characteristics of the LVTSCR in a 0.6-μm CMOS process [16].

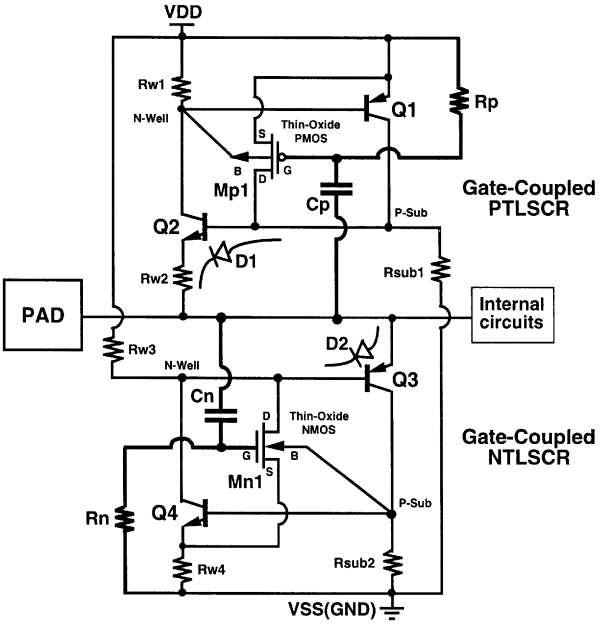
(NMOS-trigger lateral SCR) in a 0.6-μm CMOS process is shown in Fig. 5c [19]. In Fig. 5c, the I–V curves of the gate-biased NTLSCR are measured under different gate voltages, which is swept from 0 to 1 V at the gate with a step of 0.1 V. As shown in Fig. 5c, the trigger voltage of the NTLSCR can be reduced while the gate bias is increased. The trigger voltage of the gate-coupled LVTSCR can be significantly lowered by the coupled voltage on the gate of the short-channel NMOS in the LVTSCR device. Thus, the thinner gate oxide of the input stages in deep-submicron low-voltage CMOS IC's can be effectively protected by the gate-coupled LVTSCR.

An alternative design by using a circuit technique, rather than by using snapback breakdown, to turn on the LVTSCR device for ESD protection is also reported in Ref. [20].

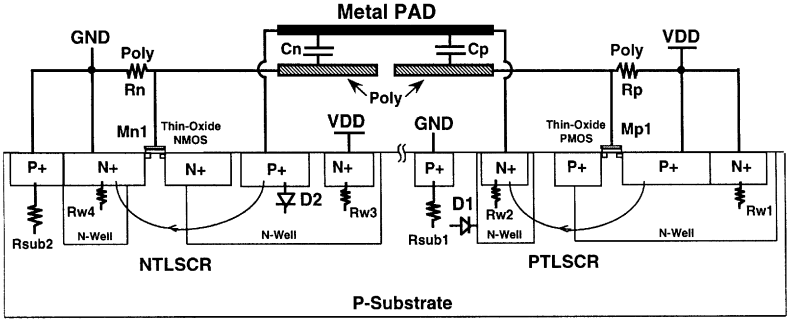
3. Issue of the LVTSCR devices in CMOS IC's

Due to the low trigger voltage ($\sim$10 V), the LVTSCR device can perform excellent on-chip ESD protection without the support of the secondary protection circuit.

But, its low trigger current ($\sim$10 mA) may cause the LVTSCR to be accidentally triggered on by the external noise pulses while the CMOS IC is operated in the normal operating condition. In order to apply safely the LVTSCR for on-chip ESD protection, the LVTSCR in CMOS IC's must have enough noise margin to the noise glitches in the application environments.

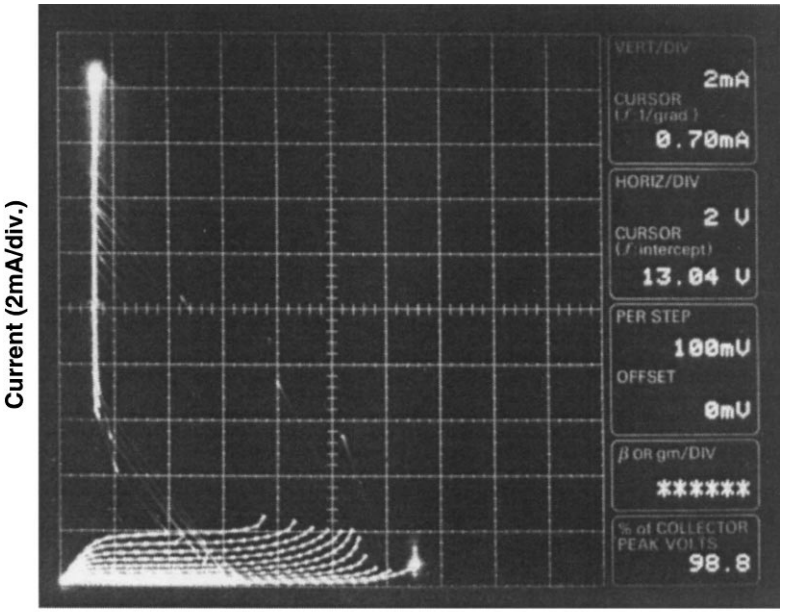


(a)



(b)

Fig. 5. (a) The ESD protection circuit with the gate-coupled LVTSCR devices, (b) the device structure of the gate-coupled LVTSCR in CMOS process, (c) the measured *I–V* characteristics of the gate-coupled NTLSCR in a 0.6-μm CMOS process with different gate biases [19].

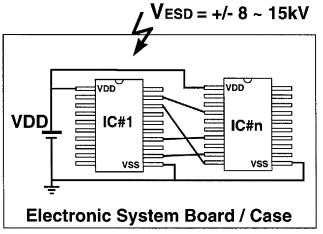


(c)

Fig. 5. (*continued*).

Recently, due to the request of the "*CE*" mark from the *European Community*, an ESD gun with the ESD voltage of 8–15 kV is used to test the electromagnetic compatibility (EMC) of the electronic products [30–32]. The system-level EMC/ESD test is illustrated in Fig. 6a. Such EMC/ESD test can cause a heavily overshooting or undershooting voltage transition on the VDD pins of the IC's in the system board, as shown in Fig. 6b. During such a system-level EMC/ESD test, the power lines of IC's in the system board can be coupled with an overstress voltage of up to several hundreds volts. Such a system-level EMC/ESD event easily causes the transient-induced latchup failure in CMOS IC's [33–35]. If the lateral SCR or the LVTSCR devices are used as ESD clamp devices between the VDD and VSS power lines of CMOS IC's [17,29], such ESD-protection SCR devices are easily triggered on by the system-level EMC/ESD transient pulses to cause very serious latchup problem in CMOS IC's.

The LVTSCR devices in the input or output ESD protection circuits are also susceptible to such system-level noise pulses. Because the holding voltage of the LVTSCR is only $\sim$1 V, the voltage levels of the input or output signals can be destroyed if the LVTSCR in the ESD protection circuits is accidentally turned on when the IC is in the normal operating condition [36]. For example, in Fig. 7a, the output buffer of Chip 1 is used to drive the input pad of Chip 2, where the input ESD



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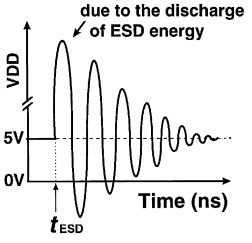


(b)

Fig. 6. (a) The schematic diagram to show system-level electromagnetic comparability (EMC) ESD test, (b) the transient overshooting/undershooting voltage waveform on the VDD pin of the IC's during system-level EMC/ESD test.

protection circuit in Chip 2 is formed by the LVTSCR. While the output buffer in Chip 1 sends an output signal of logic "1" to the input pad of Chip 2, the output PMOS in Chip 1 is turned on by the pre-buffer circuit with a logic "0". Therefore, the voltage level on the input pad of Chip 2 is charged up to VDD, and the LVTSCR is initially kept off. But, if there is a board-level noise pulse coupled to the interconnection line between the output pad of Chip 1 and the input pad of Chip 2, the LVTSCR in Chip 2 may be triggered on by the overshooting noise pulse and the voltage level on the input pad will drop to only $\sim$1 V. If the LVTSCR device is used in the output ESD protection circuit, as shown in Fig. 7b, the LVTSCR could also be triggered on by the noise pulse coupled to the output pad.

Because the output PMOS often has a large device dimension to drive an external heavy load, the load line of the output PMOS has a stable intercept point on the I–V curve of the LVTSCR. The intercept point in Fig. 7c is the operating point of the LVTSCR, where there is a current I_L flowing from VDD through the output PMOS and LVTSCR to VSS. Due to the triggering of noise pulses, the turned-on LVTSCR clamps the voltage level on the input pad of Chip 2 (the output pad of Chip 3) from VDD to $\sim$1 V. This changes the logic state from "1" to "0" on the pad and causes an operation error in the application systems. Moreover, the board-level leakage current I_L from VDD to VSS will increase significantly. The amount of increase will depend on the device dimension of the output PMOS device.

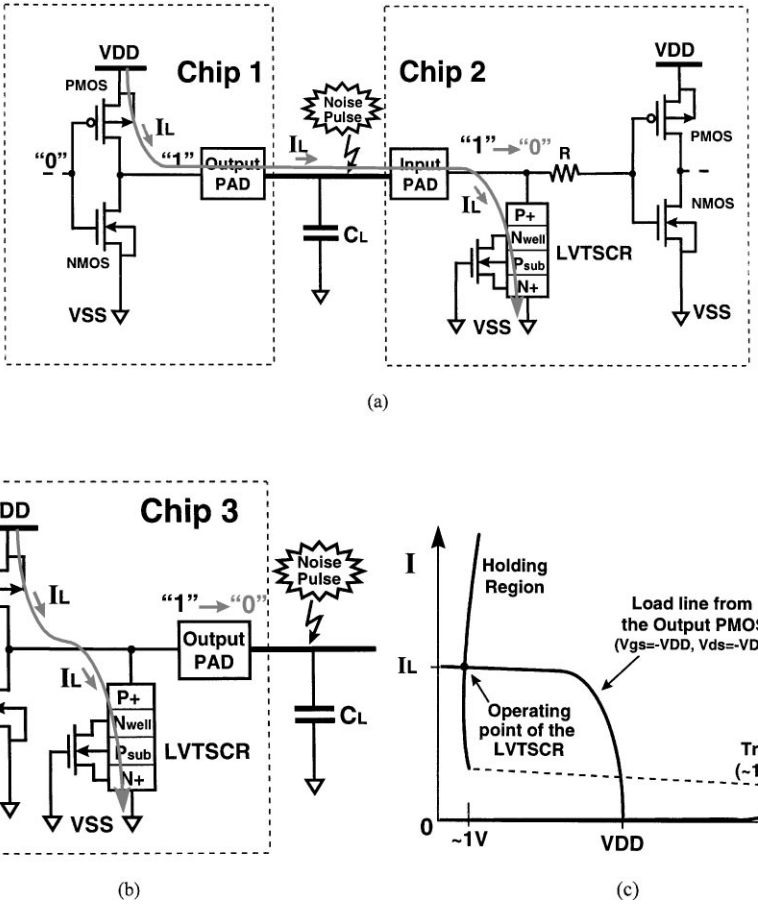


Fig. 7. The schematic diagram to show the LVTSCR in (a) an input ESD protection circuit in Chip 2, (b) an output ESD protection circuit in Chip 3, being accidentally triggered on by the system-level overshooting noise pulses. (c) The intercepted point between the I–V curves of the output PMOS and the LVTSCR decides the voltage level on the pad and the leakage current I_L from VDD to VSS.

4. Solutions to apply safely LVTSCR devices for on-chip ESD protection

There are two solutions to avoid the LVTSCR being accidentally triggered on by the noise pulses when IC's are operated in the normal operating condition. As shown in Fig. 8a, the first is to only increase the trigger current of the LVTSCR, but the trigger voltage and the holding voltage are kept the same. With a higher trigger current, the LVTSCR has enough noise margin against the overshooting or undershooting noise pulses on the pads. An HINTSCR (high-current NMOS-trigger lateral SCR) device has been successfully designed by adding a bypass diode into the LVTSCR device structure to increase its trigger current from $\sim$10 to $\sim$200 mA in

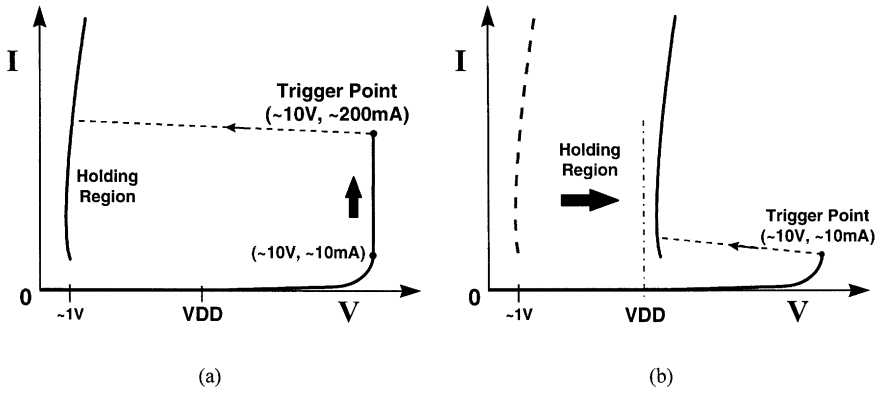
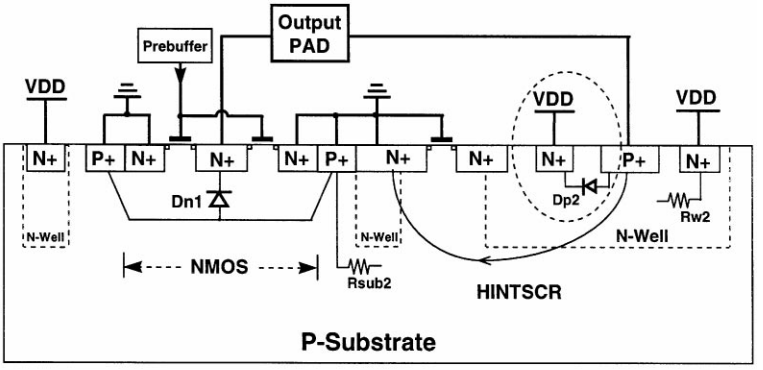


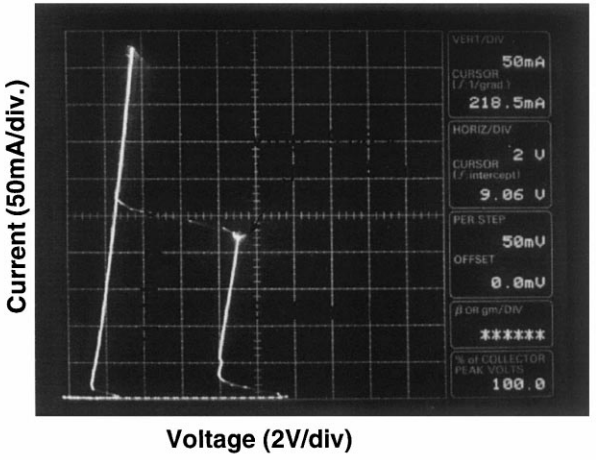
Fig. 8. Two solutions, (a) by increasing the trigger current; (b) by increasing the holding voltage, to avoid the LVTSCR being accidentally triggered on by the noise pulses.

a 0.6-μm bulk CMOS process [37–39]. The cross-sectional view of the HINTSCR merged with the output NMOS in the layout is drawn in Fig. 9a. The measured I–V curves of the HINTSCR in a 0.6-μm bulk CMOS process is shown in Fig. 9b, where the trigger current (voltage) to initiate the HINTSCR into its latching state is 218.5 mA (9.06 V) [39]. With a trigger current of above 200 mA, the HINTSCR has a much higher immunity against the board-level noise pulses or the system-level EMC/ESD tests in the application systems.

The second method is to increase the holding voltage of the LVTSCR greater than the voltage level of VDD in CMOS IC's, as shown in Fig. 8b. This method maintains the trigger voltage and current as low as that of an LVTSCR. In a CMOS process with an epitaxial substrate, the holding voltage of an SCR device can be easily increased greater than VDD by extending the anode-to-cathode distance in the SCR structure or by reducing the thickness of the epitaxial layer [40,41]. However, increasing the holding voltage of an LVTSCR leads to more power dissipation (Power $\cong I_{ESD} \times V_{hold}$) of the LVTSCR during an ESD transient. This will cause a lower ESD robustness on the LVTSCR. The dependence of layout spacing on ESD performance of an LVTSCR device with a holding voltage greater than VDD has been investigated in a CMOS process with epitaxial substrate [42]. The LVTSCR device realized in an epitaxial substrate is drawn in Fig. 10a, where the layout spacing S of drain N^+ diffusion of the inserted NMOS in the LVTSCR structure has an effect on the holding voltage of LVTSCR device in the epitaxial substrate. The dependence of the holding voltage and human-body-model (HBM) ESD level of an LVTSCR on the layout spacing S in an epitaxial p-substrate CMOS process is redrawn in Fig. 10b, where a layout spacing S of 3–4 μm can increase the holding voltage but still not degrade its ESD robustness [42]. With a wider layout spacing S, the LVTSCR in the epitaxial p-substrate CMOS process has a higher holding voltage, but its ESD robustness degrades sharply. For the CMOS process with different thickness of the



(a)



(b)

Fig. 9. (a) The schematic cross-sectional view of the high-current NMOS-trigger lateral SCR (HINTSCR) device merged with the output NMOS device in a p-substrate bulk CMOS process. (b) The measured I–V curve of the HINTSCR device fabricated in a 0.6-μm bulk CMOS process [39].

epitaxial layer and different doping concentration, the suitable layout spacing to increase the holding voltage must be investigated in detail with the consideration on reasonable process variations.

However, most CMOS IC's (especially the consumer IC's) are still fabricated in the low-cost bulk CMOS processes without using the epitaxial substrate. It is difficult to increase the holding voltage of an SCR device greater than VDD in such bulk CMOS processes. Using the double guard rings to surround both the anode and the cathode of an SCR device can break the latching path and increase its holding voltage. But, the

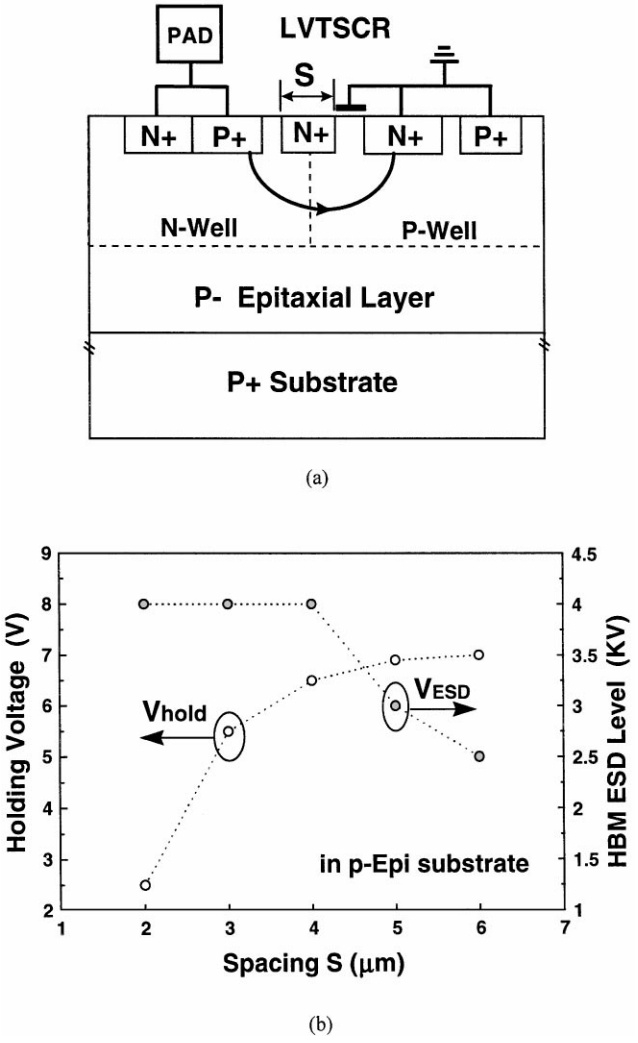


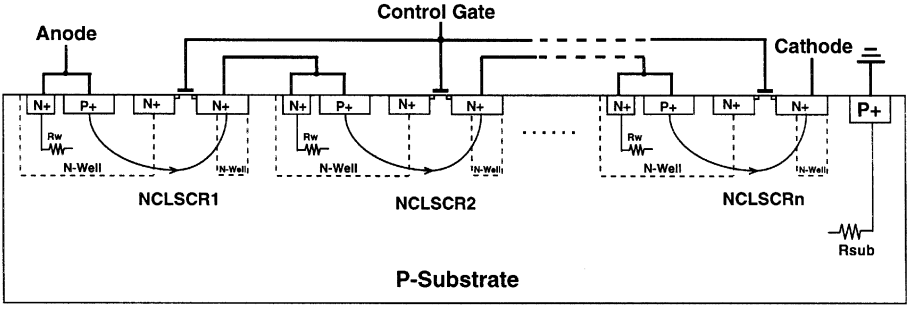
Fig. 10. (a) The device structure of the LVTSCR in a p-epitaxial CMOS process with different layout spacing *S*. (b) The dependence of the holding voltage and ESD level of the LVTSCR on the layout spacing *S* [42].

latchup guard rings often occupy much more layout area and wider layout spacing in the bulk CMOS process. Moreover, such SCR devices with double guard rings in the bulk CMOS process take more time to turn on, so they cannot be triggered on in time to bypass a fast-transient ESD current.

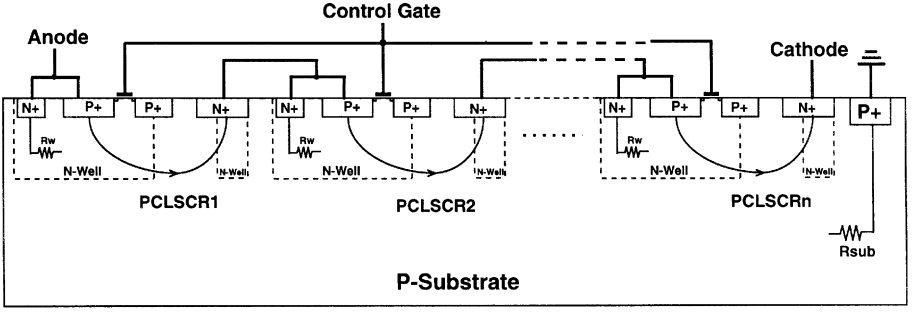
To overcome this issue, a novel stacked-LVTSCR structure is designed in this paper to increase its holding voltage ($>$VDD) without much degrading its ESD robustness in a 0.35-μm silicide bulk CMOS process [43].

5. Design of the stacked LVTSCR's

To increase the holding voltage of an LVTSCR without increasing the power dissipation in the LVTSCR, a novel stacked configuration is proposed to achieve both high component-level ESD robustness and safe application without the latchup problem during system-level EMC/ESD tests. The device structures of the proposed stacked NCLSCR's (NMOS-controlled lateral SCR's) and stacked PCLSCR's (PMOS-controlled lateral SCR's) are shown in Figs. 11a and b, respectively, in a p-substrate bulk CMOS process. In Fig. 11, the cathode of the NCLSCR1 (PCLSCR1) is connected to the anode of the NCLSCR2 (PCLSCR2), and the cathode of the NCLSCR2 is connected to the anode of the next NCLSCR (PCLSCR) device to configure the stacked NCLSCR's (PCLSCR's). All the gates of the NCLSCR's (PCLSCR's) are connected together and controlled by a control gate. To save more



(a)



(b)

Fig. 11. The schematic cross-sectional view of (a) the stacked NCLSCR's, and (b) the stacked PCLSCR's in a p-substrate bulk CMOS process.

layout area, the N-well of the cathode in NCLSCR1 (PCLSCR1) can be merged with the N-well of the anode in NCLSCR2 (PCLSCR2), and so on between every two adjacent NCLSCR (PCLSCR) devices. The N^+ diffusion of the cathode in NCLSCR1 (PCLSCR1) can also be merged with the N^+ diffusion of the N-well bias (Rw) in the anode N-well of NCLSCR2 (PCLSCR2) to further reduce the total area of the stacked NCLSCR's (PCLSCR's) devices.

By using the stacked configuration, the total voltage drop across the stacked NCLSCR's (PCLSCR's) is the sum of the voltage drop across every NCLSCR (PCLSCR) device. Therefore, the total holding voltage of the stacked NCLSCR's (PCLSCR's) becomes tunable by changing the number of the NCLSCR's (PCLSCR's) in the stacked configuration. If the stacked NCLSCR's include 3 NCLSCR devices, its total holding voltage can be greater than the 3-V VDD. Each NCLSCR device still has a holding voltage of $\sim$1 V, but the stacked NCLSCR's have a holding voltage greater than 3-V VDD. So, the stacked NCLSCR's (PCLSCR's) can be safely applied for effective ESD protection without causing accidental trigger-on operation errors or latchup in CMOS IC's. To provide a quick turn-on response in such stacked NCLSCR's (PCLSCR's) to bypass the fast-transient ESD current, a suitable control circuit must be designed to simultaneously trigger on every NCLSCR (PCLSCR) device in the stacked configuration during the ESD-stress condition. The design examples are demonstrated in Section 7 with practical turn-on verification in a 0.35-μm bulk CMOS technology.

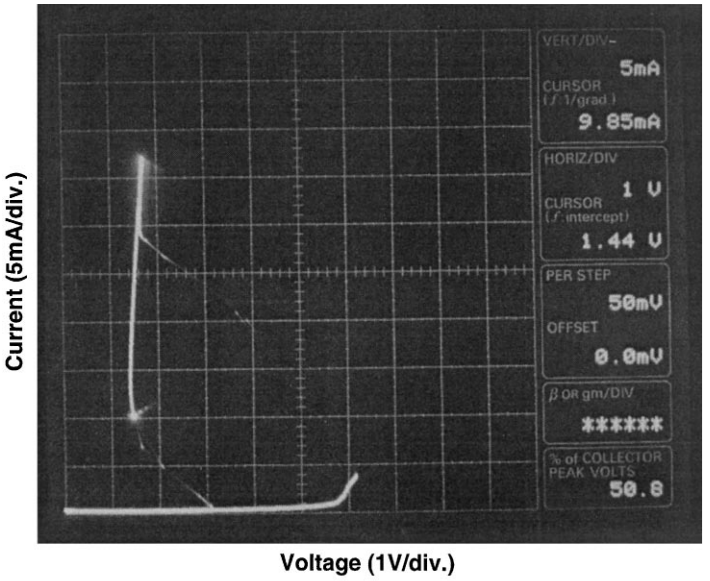
6. Characteristics of the stacked LVTSCR's

The stacked NCLSCR's and PCLSCR's with different number of LVTSCR devices have been fabricated in a 0.35-μm bulk CMOS process with both silicide diffusion and LDD structure. The device characteristics, especially the temperature effects, has been measured and investigated in more detail.

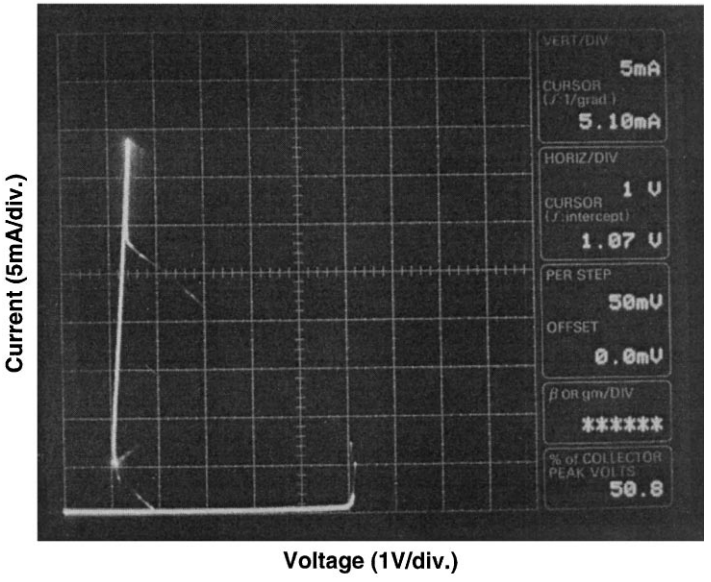
6.1. The stacked NCLSCR's

The *I–V* curves of a single NCLSCR with 0-V gate bias are shown in Figs. 12a and b at the temperature of 25 and 150°C, respectively. The holding voltage of a single NCLSCR is reduced from the 1.44 V at 25°C to only 1.07 V at 150°C, which is much lower than VDD of CMOS IC's. Such a single NCLSCR in the ESD protection circuit is easily triggered on by system-level EMC/ESD tests or by high-temperature high-voltage reliability tests which often cause failures or malfunctions in the application systems.

The *I–V* curves of the stacked NCLSCR's with three and five NCLSCR's at 125°C are shown in Figs. 13a and b, respectively, under different gate biases. The trigger voltage of the NCLSCR can be significantly reduced as its gate voltage is increased. With a positive gate voltage, the stacked NCLSCR's are easily triggered into the holding region. The dependence of the trigger voltage of the stacked 3-NCLSCR's and a single NCLSCR on the control-gate voltage at a temperature of 125°C is shown



(a)



(b)

Fig. 12. The I–V curves of a single NCLSCR device in a 0.35-μm bulk CMOS process at the temperature of (a) 25°C, and (b) 150°C.

in Fig. 14. A higher gate voltage leads to a lower trigger voltage to turn on the stacked NCLSCR's.

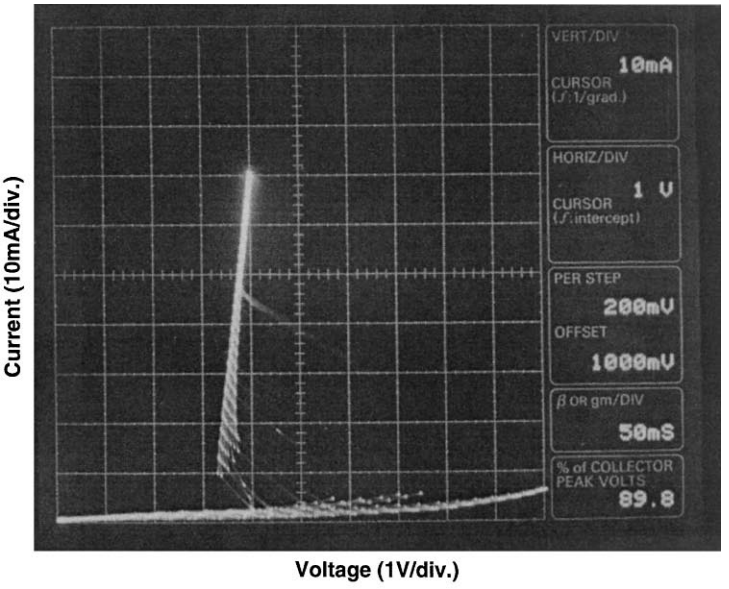
In Fig. 13, the holding voltage of the 3-NCLSCR's is 3.82 V, whereas the holding voltage of the 5-NCLSCR's is 6.36 V. The temperature dependence of the total holding voltage in the stacked NCLSCR's with different number of NCLSCR devices is shown in Fig. 15. The dependence of the holding voltage of the stacked NCLSCR's on the number of the NCLSCR devices at different temperatures is shown in Fig. 16. The holding voltage of the stacked NCLSCR's is almost linearly increased as the number of the stacked NCLSCR devices is increased. By adjusting the number of the stacked NCLSCR devices, the holding voltage of the stacked NCLSCR's becomes tunable for different applications. For example, to safely apply the stacked NCLSCR's for ESD protection in 3-V CMOS IC's without causing potential latchup, three stacked NCLSCR's must be used. This provides a practical and useful solution to safely apply the LVTSCR for effective ESD protection, especially in bulk CMOS processes.

6.2. The stacked PCLSCR's

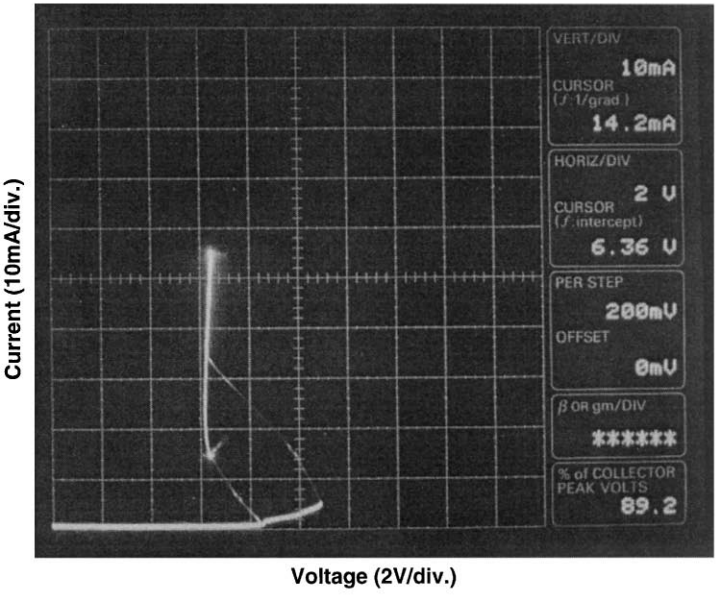
The I–V curves of the stacked PCLSCR's with two and five PCLSCR's at 150°C are shown in Figs. 17a and b, respectively, under 0-V gate bias. The holding voltage of the 2-PCLSCR's is -2.4 V, whereas the holding voltage of the 5-PCLSCR's is -6.7 V. The temperature dependence of the holding voltage of the stacked PCLSCR's is shown in Fig. 18. The dependence of the holding voltage of the stacked PCLSCR's on the number of PCLSCR devices at different temperatures is shown in Fig. 19. The holding voltage of the stacked PCLSCR's is almost linearly increased as the number of PCLSCR devices in the stacked configuration is increased. By adjusting the number of the stacked PCLSCR devices, the holding voltage of the stacked PCLSCR's becomes tunable for different applications. For example, to safely apply the stacked PCLSCR's for ESD protection in 3-V CMOS IC's without causing potential latchup, three PCLSCR's must be used in the stacked PCLSCR's.

6.3. Turn-on resistance

The slope ($\Delta V/\Delta I$) of the measured I–V curves of the stacked NCLSCR's and PCLSCR's devices can be defined as the turn-on resistance of the stacked LVTSCR's in their holding regions. The turn-on resistance in the holding region changes slightly while the operating point is moving along the I–V curves in the holding region. For a simple comparison, the slope ($\Delta V/\Delta I$) between two operating points at the operating currents of 20 and 200 mA in the holding region is defined as the turn-on resistance of the stacked LVTSCR's. The relations between the turn-on resistance and the number of stacked LVTSCR's are shown in Fig. 20. All the stacked LVTSCR's devices have the same device width of 30 μm only. With a device width of 30 μm, the stacked 3-NCLSCR's have a turn-on resistance of 9.8 Ω, but the stacked 3-PCLSCR's have a turn-on resistance of 12.7 Ω. A larger device width can lead to a lower turn-on



(a)



(b)

Fig. 13. The I–V curves of (a) the stacked 3-NCLSCR's with different gate biases, and (b) the stacked 5-NCLSCR's with 0-V gate bias, at the temperature of 125°C.

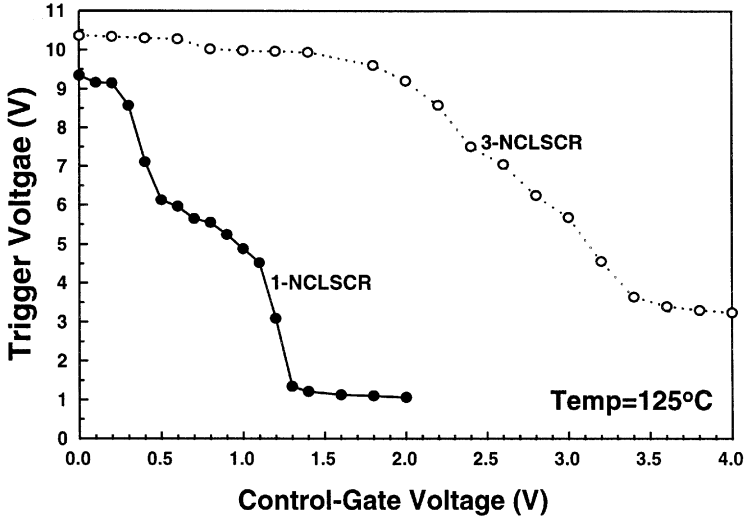


Fig. 14. Dependence of the trigger voltage of the stacked 3-NCLSCR's and a single NCLSCR on the control-gate voltage at the temperature of 125°C.

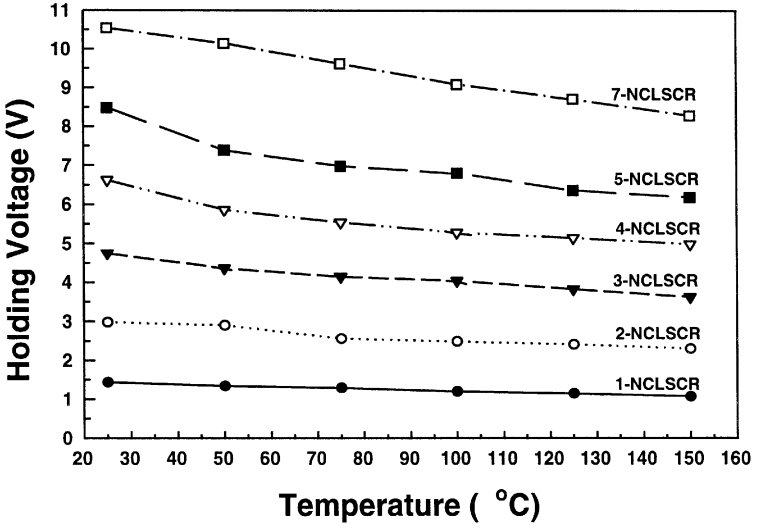


Fig. 15. The temperature dependence of the total holding voltage in the stacked NCLSCR's with different number of NCLSCR devices.

resistance in the stacked LVTSCR's. More NCLSCR's or PCLSCR's used in the stacked configuration cause a corresponding higher turn-on resistance in the stacked LVTSCR's. To reduce the turn-on resistance, the stacked LVTSCR's can be designed with wider device widths.

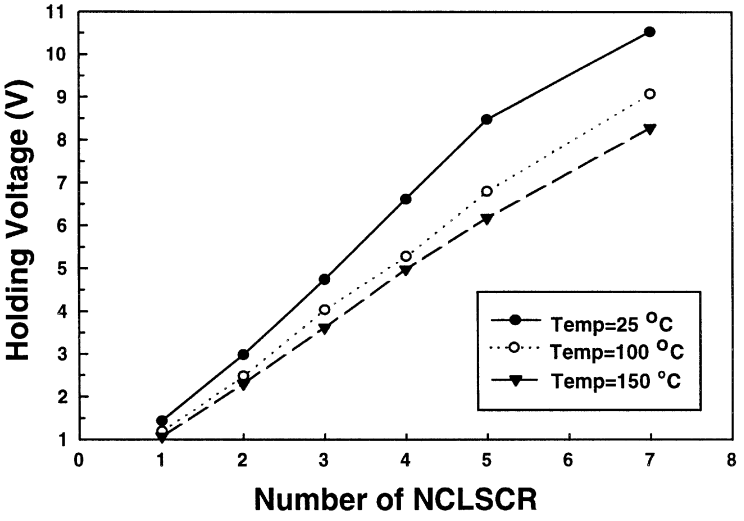


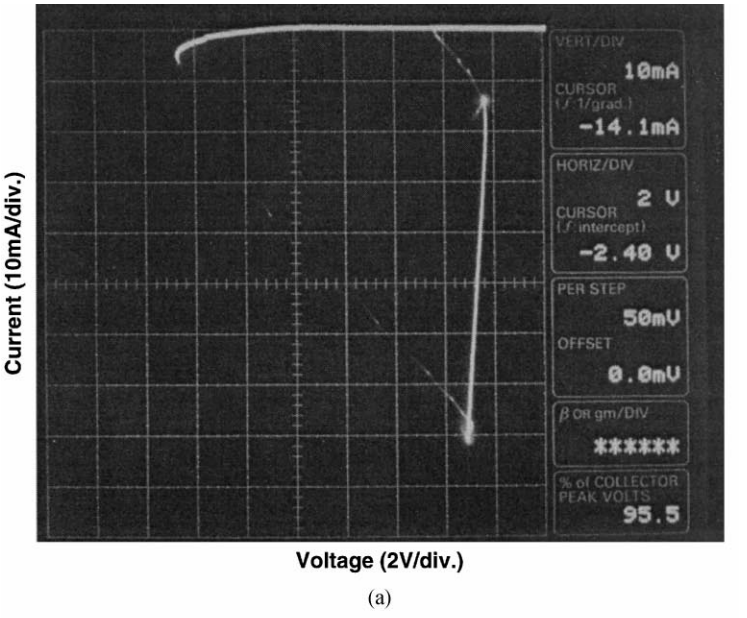
Fig. 16. Dependence of the holding voltage of the stacked NCLSCR's on the number of the NCLSCR devices.

7. Safe applications for whole-chip ESD protection

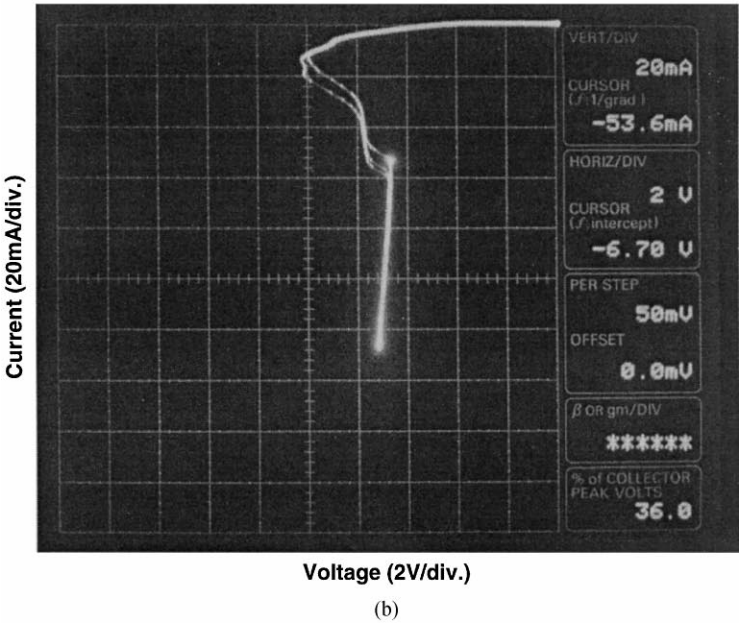
7.1. ESD protection circuits

A detailed investigation of the device characteristics including the temperature dependence revealed that the stacked LVTSCR's with three NCLSCR's (PCLSCR's) in a 0.35-μm bulk CMOS process have a holding voltage of 4.74 V (− 4.96 V) at 25°C and 3.62 V (− 3.66 V) at 150°C. To safely apply the LVTSCR's for ESD protection in 3-V CMOS IC's, three NCLSCR's or PCLSCR's in the stacked configuration are enough. The typical input and output ESD protection circuits using both stacked 3-NCLSCR's and stacked 3-PCLSCR's with the gate-coupled technique [18,19] for 3-V CMOS IC's are shown in Figs. 21a and b, respectively. The gate-coupled technique is used to generate the bias on the control gate of the stacked NCLSCR's (PCLSCR's), therefore the stacked NCLSCR's (PCLSCR's) can be quickly triggered on to bypass ESD current. With a holding voltage greater than VDD, such stacked NCLSCR's and PCLSCR's in the input/output ESD protection circuits can help to clamp the overshooting or undershooting noise pulses on the input/output pads, but do not cause potential latchup to destroy the normal input/output signals when the IC's are in the normal operating condition.

Such stacked NCLSCR's (or PCLSCR's) can also be applied to the VDD-to-VSS ESD clamp circuits to avoid ESD failures located in the internal circuits. To simultaneously turn on every NCLSCR (or PCLSCR) device in the stacked configuration, an ESD-detection circuit should be designed to bias the control gate. VDD-to-VSS ESD clamp circuits using the stacked 3-NCLSCR's or stacked 3-PCLSCR's with



(a)



(b)

Fig. 17. The I–V curves of the stacked PCLSCR's with (a) two PCLSCR devices, (b) five PCLSCR devices, at the temperature of 150°C.

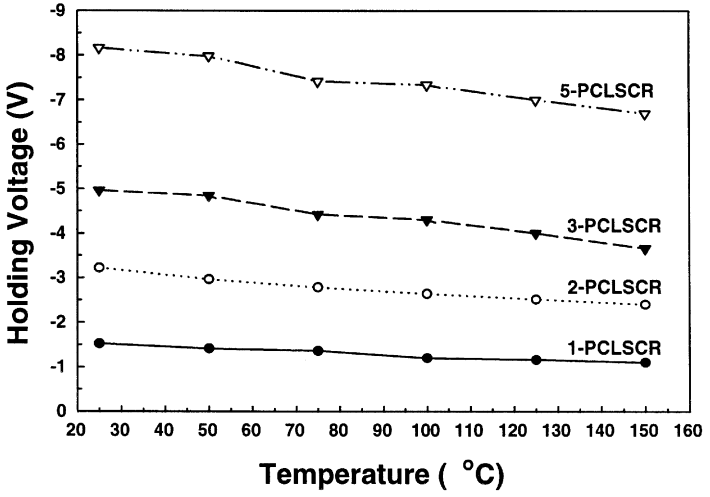


Fig. 18. The temperature dependence of the holding voltage of the stacked PCLSCR's with different number of PCLSCR devices.

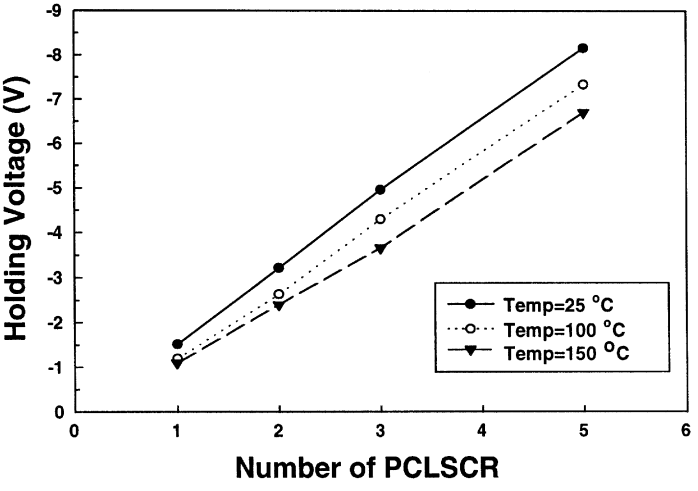


Fig. 19. Dependence of the holding voltage of the stacked PCLSCR's on the number of PCLSCR devices.

an *RC*-based control circuit [25–28] are shown in Figs. 22a and b, respectively. The *RC* time constant in the *RC*-based control circuit is designed around 0.1–1 μs to perform the correct ESD-detection function [28] to trigger on the stacked NCLSCR's (PCLSCR's) during the ESD-stress condition. The number of the NCLSCR or PCLSCR devices used in the stacked configuration is dependent on the voltage level of VDD in the CMOS IC. For 5-V CMOS IC's, 5-NCLSCR's (5-PCLSCR's) must be

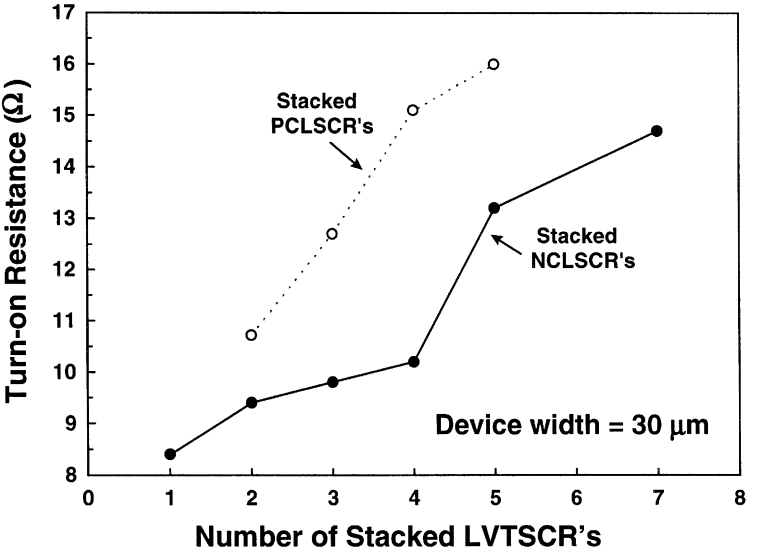


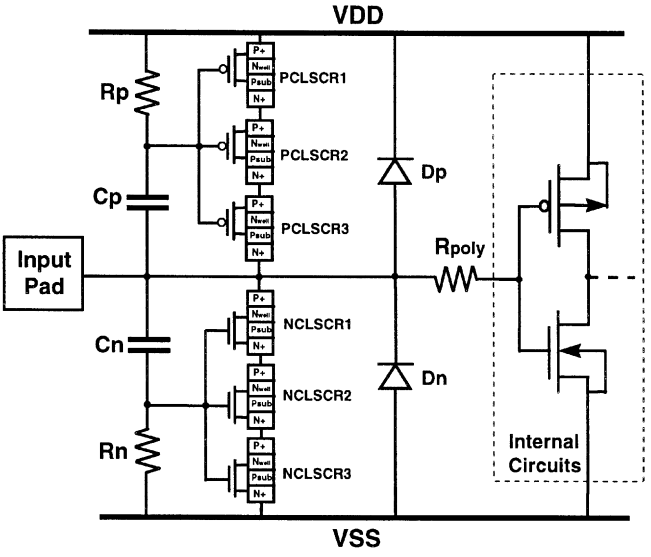
Fig. 20. The relations between the turn-on resistance and the number of stacked LVTSCR's.

used in the VDD-to-VSS ESD clamp circuit to effectively clamp the ESD voltage across the VDD and VSS power lines without causing a VDD-to-VSS latchup problem.

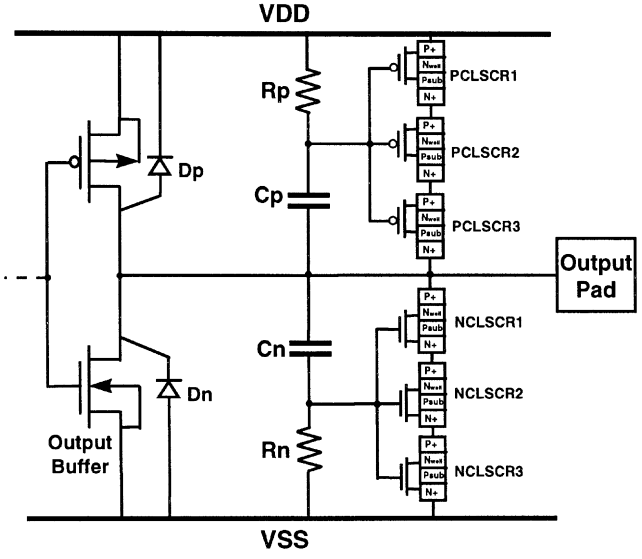
By applying such stcaked NCLSCR's (PCLSCR's) in both the input/output ESD protection circuits and the VDD-to-VSS ESD clamp circuits, a whole-chip ESD protection scheme can be constructed to well protect the CMOS IC's in deep-submicron CMOS technologies.

7.2. Turn-on verification

To verify the turn-on behavior of the stacked NCLSCR's in the VDD-to-VSS ESD clamp circuit, an experimental setup is shown in Fig. 23, where an ESD-like voltage pulse generated from a pulse generator (*hp*8116A) is applied to the VDD power line with the VSS grounded. A 0-to-8 V voltage pulse with a pulse width of 400 ns and a rise time of $\sim$6 ns is applied to the VDD power line. If the stacked NCLSCR's in the VDD-to-VSS ESD clamp device are triggered on, the 0-to-8 V voltage pulse will be degraded and clamped to a voltage level around the holding voltage of the stacked NCLSCR's. A typical voltage waveform of the 0-to-8 V voltage pulse degraded by the stacked 3-NCLSCR's is shown in Fig. 24a. When the 0-to-8 V voltage pulse is applied, the stacked 3-NCLSCR's is triggered on and clamps the voltage pulse to a voltage level of 4.75 V, which corresponds to the holding voltage of the stacked 3-NCLSCR's. From the degraded waveform in Fig. 24a, it is also shown that the stacked 3-NCLSCR's have a turn-on time of $\sim$20 ns to fully clamp the applied 0-to-8 V voltage



(a)



(b)

Fig. 21. (a) The input ESD protection circuit, and (b) the output ESD protection circuit, using both the stacked 3-NCLSCR's and the stacked 3-PCLSCR's with the gate-coupled technique.

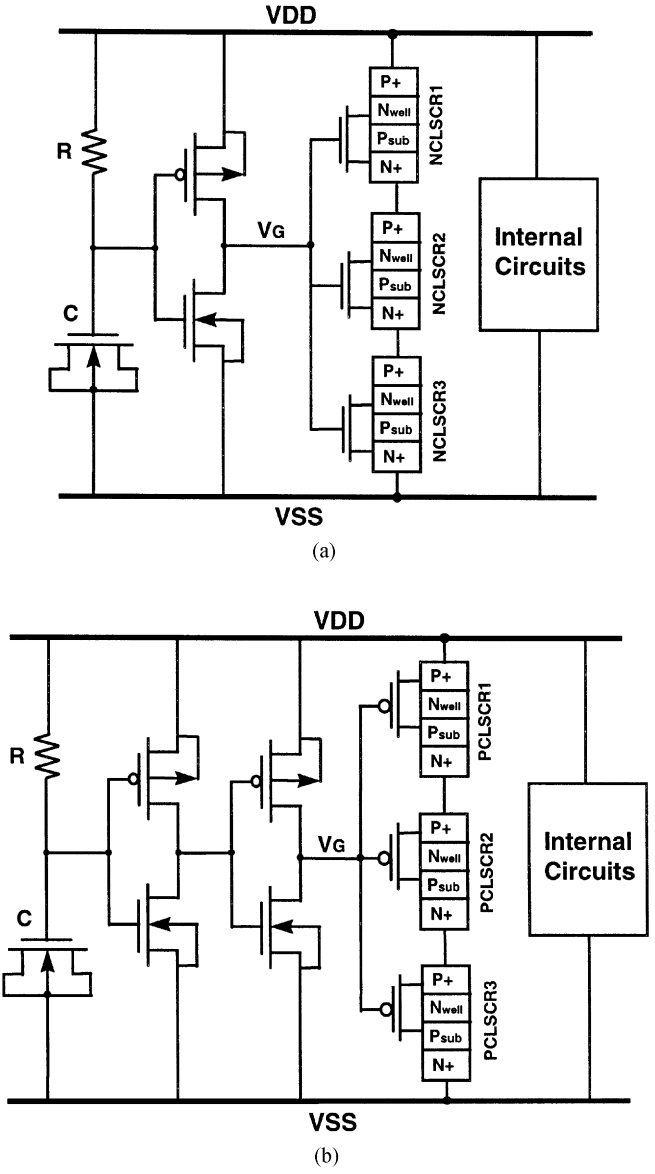


Fig. 22. The VDD-to-VSS ESD clamp circuit using (a) the stacked 3-NCLSCR's, and (b) the stacked 3-PCLSCR's, with the *RC*-based control circuit.

pulse on the VDD power line. If the ESD clamp circuit only has a single NCLSCR between the VDD and VSS power lines, the applied 0–8 V voltage is clamped only to 1.5 V in Fig. 24b. In Fig. 24b, the single NCLSCR also takes a time of $\sim$20 ns to fully turn itself on. From the turn-on times between Figs. 24a and b, it approves that the

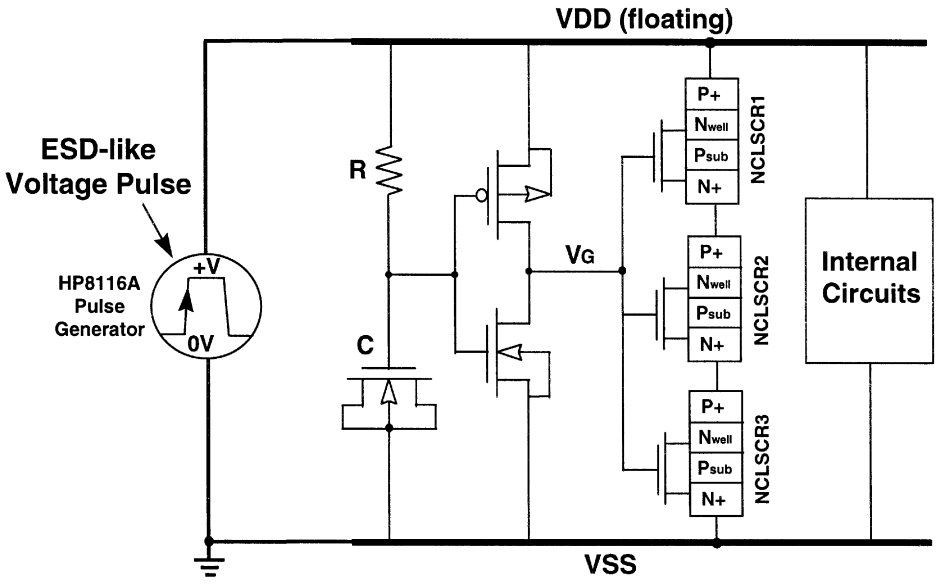
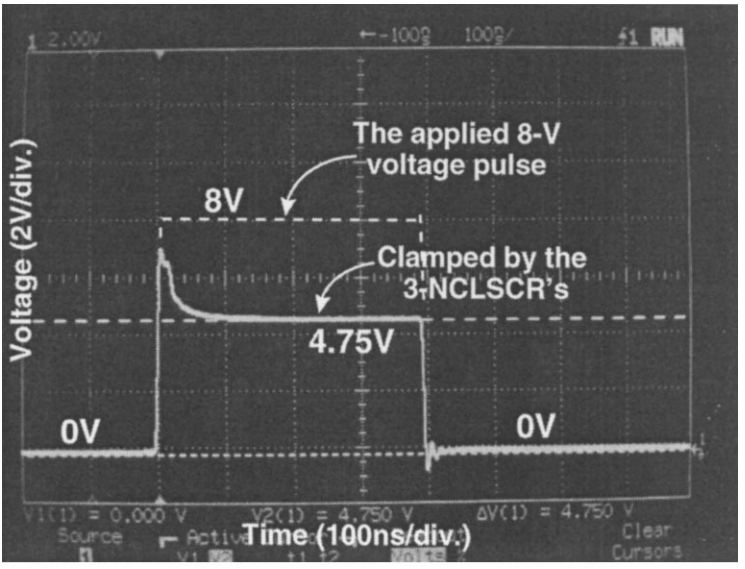


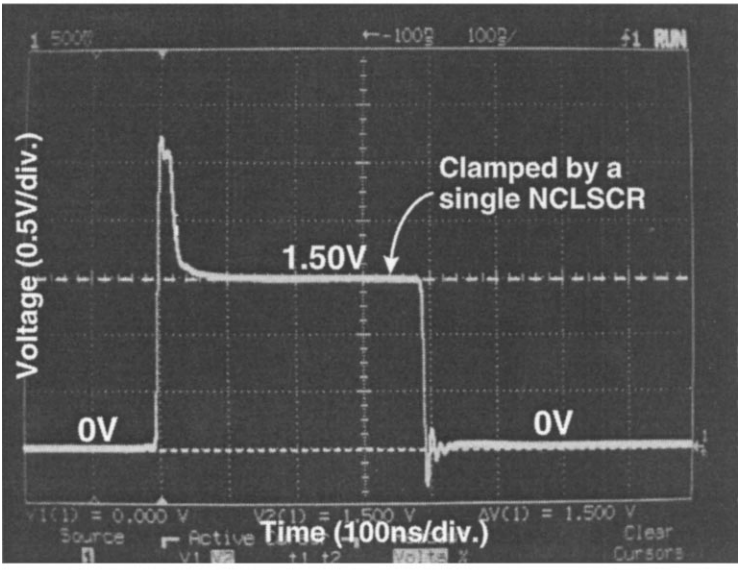
Fig. 23. The experimental setup to verify the turn-on behavior of the VDD-to-VSS ESD clamp circuit with the stacked LVTSCR's during the ESD-stress condition.

turn-on time does not increase when the stacked NCLSCR's have more NCLSCR devices in the stacked configuration. After the stacked NCLSCR's are triggered on, the clamped voltage level is proportional to the holding voltage of the stacked NCLSCR's. This verifies the turn-on efficiency of the stacked NCLSCR's in the ESD-stress condition.

However, in the normal operating condition with 3-V VDD and 0-V VSS power supplies, the stacked NCLSCR's in the ESD clamp circuit should not be triggered on by an overshooting voltage pulse on the VDD power line. To verify this issue, an experimental setup is shown in Fig. 25, where an overshooting voltage pulse is applied to the VDD power line of a CMOS IC with 3-V VDD power supply and the VDD-to-VSS ESD clamp circuit. The measured results at 25°C are shown in Fig. 26a and b for the ESD clamp circuit with stacked 3-NCLSCR's and a single NCLSCR, respectively. In Fig. 26a, a 3-to-4 V overshooting voltage pulse applied to the VDD power line is not degraded, because the stacked 3-NCLSCR's are not triggered on by such an overshooting voltage pulse. But, in Fig. 26b, the 3-to-4 V overshooting voltage pulse applied to the VDD power line is degraded and kept at 1.5 V after the triggering of the 3-to-4 V overshooting voltage pulse, because the VDD-to-VSS ESD clamp circuit with a single NCLSCR is triggered on by this overshooting voltage pulse. The turned-on ESD clamp circuit with a single NCLSCR keeps the voltage level on the VDD power line only at 1.5 V. This causes the so-called latchup problem in CMOS IC's. Thus, the VDD-to-VSS ESD clamp circuit or the input/output ESD



(a)



(b)

Fig. 24. The degraded voltage waveforms of the 0-to-8 V voltage pulse clamped by the VDD-to-VSS ESD clamp circuit with (a) the stacked 3-NCLSCR's, and (b) a single NCLSCR.

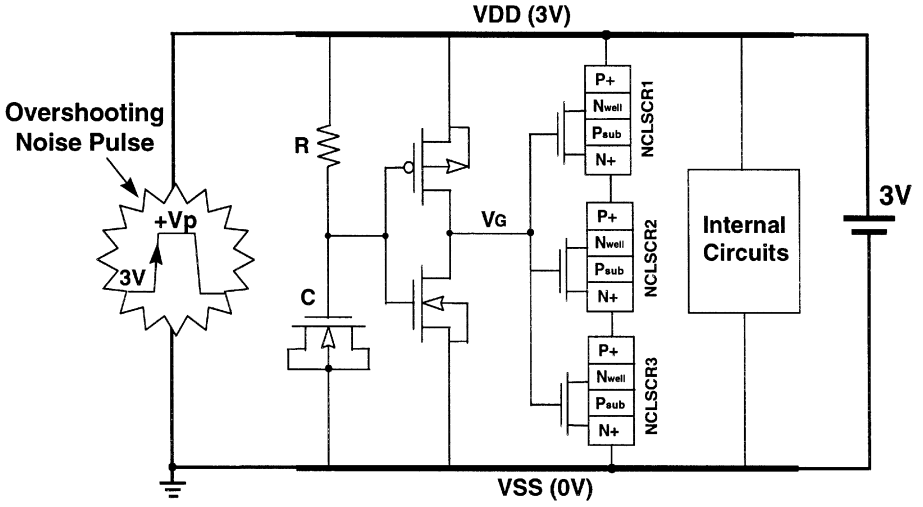
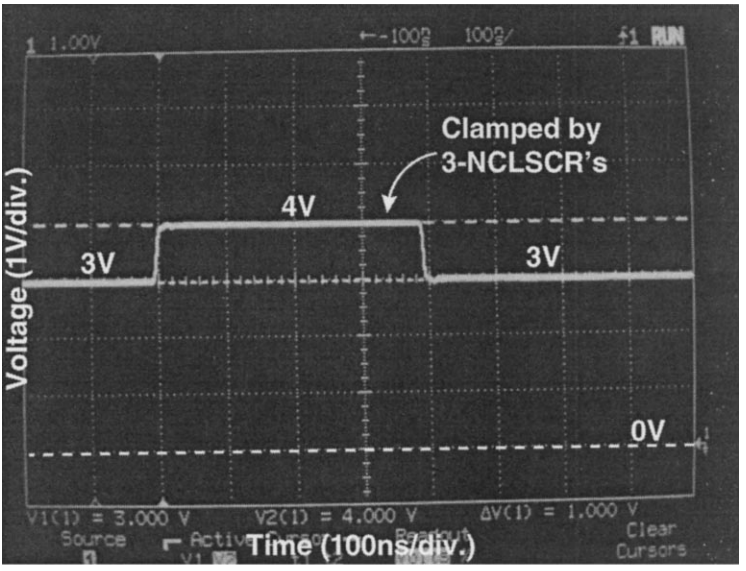


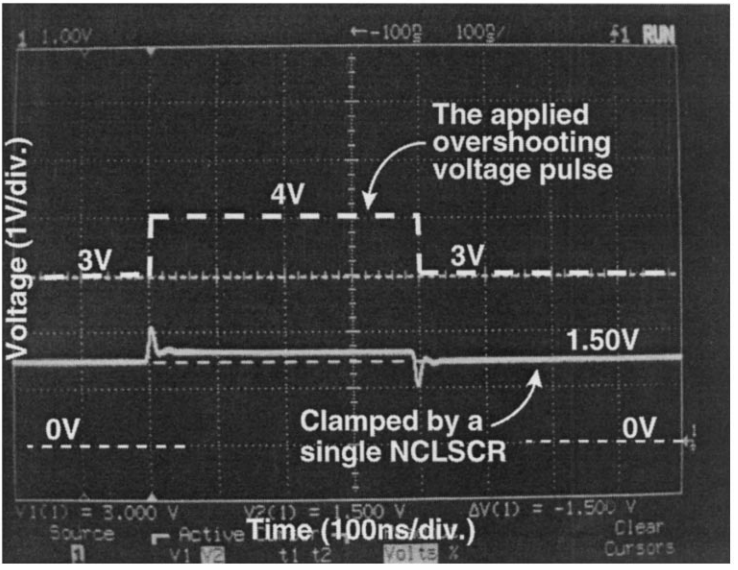
Fig. 25. The experimental setup to verify the turn-on behavior of the VDD-to-VSS ESD clamp circuit with the stacked LVTSCR's in the normal operating condition with 3-V VDD power supply and the overshooting noise pulse.

protection circuits in CMOS IC's with a single LVTSCR have the potential for latchup in noisy environments.

To further verify the safe application of the stacked LVTSCR's, a larger 3-to-8 V overshooting voltage pulse is applied to the VDD power line with a 3-V power supply and the VDD-to-VSS ESD clamp circuit. The measured waveforms at 25°C are shown in Figs. 27a and b for the VDD-to-VSS ESD clamp circuit with stacked 3-NCLSCR's and stacked 2-PCLSCR's, respectively. In Fig. 27a, the 3-to-8 V overshooting voltage pulse is degraded by the stacked 3-NCLSCR's to the voltage level of about 4.94 V. But, after the triggering of the 3-to-8 V overshooting voltage pulse, the VDD voltage level is restored to the original 3 V. This means that the stacked 3-NCLSCR's can effectively clamp the overshooting voltage pulse on the VDD power line but do not cause the VDD-to-VSS latchup problem in the ESD clamp circuit when the IC is in the normal operating condition. In Fig. 27b, the 3-to-8 V overshooting voltage pulse is degraded by the stacked 2-PCLSCR's to the voltage level of about 3.63 V. But, after the triggering of the 3-to-8 V overshooting voltage pulse, the VDD voltage level is also restored to the original 3 V. Because the holding voltage of the stacked 2-PCLSCR's at 25°C is around 3.22 V, the stacked 2-PCLSCR's can automatically turn off after the VDD voltage level has returned to 3 V. As shown in Fig. 18, the holding voltage of the stacked 2-PCLSCR's is decreased to only 2.4 V when the temperature is increased to 150°C. This implies that the stacked 2-PCLSCR's are still susceptible to the latchup problem, if the CMOS IC's are operating in the high-temperature environments.

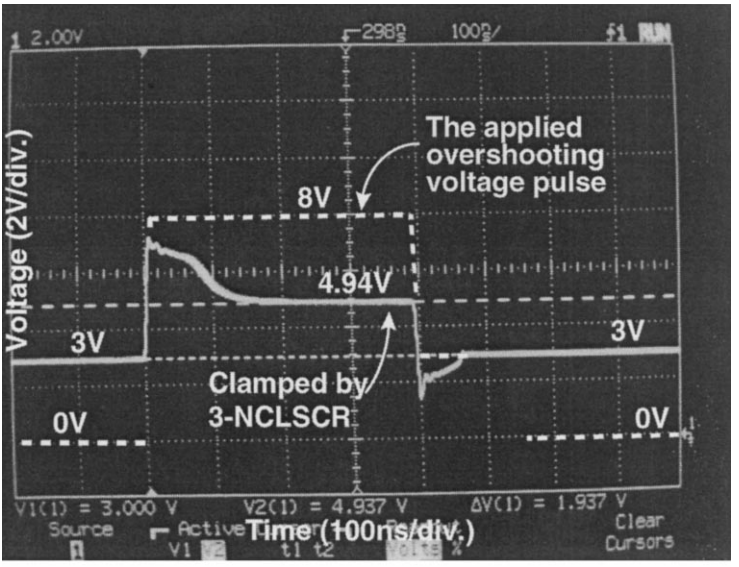


(a)

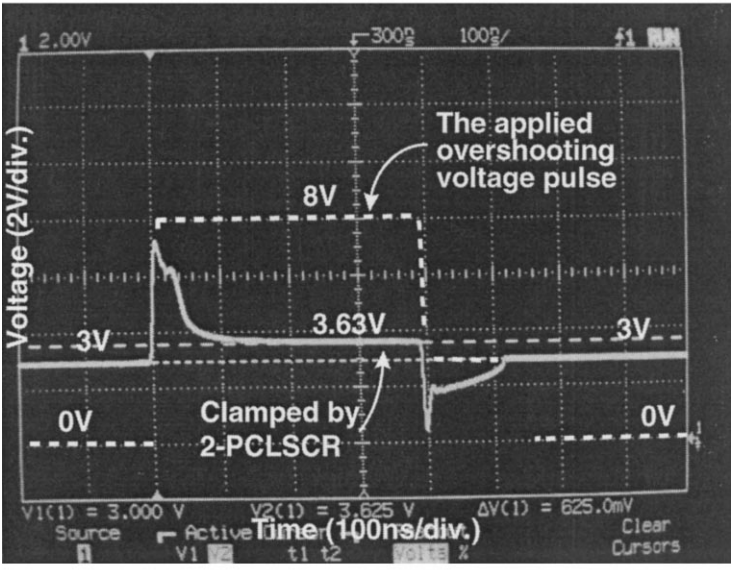


(b)

Fig. 26. The voltage waveforms of the 3-to-4 V overshooting voltage pulse clamped by the VDD-to-VSS ESD clamp circuit with (a) the stacked 3-NCLSCR's, and (b) a single NCLSCR.



(a)



(b)

Fig. 27. The degraded voltage waveforms of the 3-to-8 V overshooting voltage pulse clamped by the VDD-to-VSS ESD clamp circuit with (a) the stacked 3-NCLSCR's, and (b) the stacked 2-PCLSCR's.

7.3. ESD robustness

The VDD-to-VSS ESD clamp circuits designed in Fig. 22 with different number of stacked NCLSCR's or stacked PCLSCR's are tested by the human-body-model (HBM) ESD stress. The failure criterion is defined as the leakage current under the 5-V bias from VDD to VSS is greater than 1 μA. The HBM ESD robustness per device width (V_{ESD}/W) of the stacked NCLSCR's or the stacked PCLSCR's is shown in Fig. 28, where a gate-grounded NMOS (ggNMOS) with a device dimension (W/L) of 480/0.5 (μm/μm) in the same 0.35-μm bulk CMOS process is also tested for reference. All the stacked NCLSCR's, PCLSCR's, and the ggNMOS are made by using neither ESD-implant process nor silicide-blocking process. The ESD robustness per device width (V_{ESD}/W) of the stacked 3-NCLSCR's (ggNM)S is 50 V/μm (3.13 V/μm) in the 0.35-μm bulk CMOS process. The NMOS (PMOS) inserted in each NCLSCR (PCLSCR) device has a channel length of only 0.35 μm. The ggNMOS ($W/L = 480/0.5$) occupies a layout area of 80×76 μm^2 and can sustain an HBM ESD level of only 1.5 kV. But the stacked 3-NCLSCR's with a layout area of 60×60 μm^2 can sustain a 3-kV HBM ESD stress, where every NCLSCR has a layout dimension (W/L) of only 60/20 (μm/μm). Therefore, the ESD robustness per layout area of the stacked 3-NCLSCR's (ggNMOS) can be 0.83 V/μm^2 (0.25 V/μm^2) in the 0.35-μm bulk CMOS process without using the silicide-blocking and ESD-implant process steps. Although the ESD performance of the stacked LVTSCR's is degraded when the number of the LVTSCR's in the stacked configuration is increased, the ESD robustness and area efficiency of the stacked LVTSCR's in 3-V application is still much greater than that of the ggNMOS.

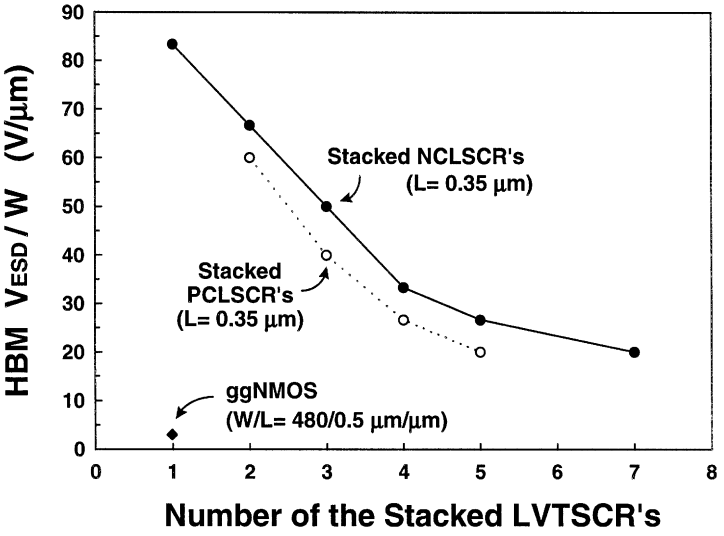


Fig. 28. The HBM ESD robustness per device width (V_{ESD}/W) of the stacked LVTSCR's with different number of NCLSCR or PCLSCR devices in a 0.35-μm silicided CMOS process.

With a tunable holding voltage greater than the VDD voltage level of CMOS IC's, the stacked configuration provides a practical and cost-efficient solution to safely apply the LVTSCR devices for effective on-chip ESD protection without the accidental latchup danger in bulk CMOS technologies.

8. Conclusions

The LVTSCR devices had been reported for on-chip ESD protection in CMOS IC's about ten-years ago, but such devices can be triggered on by the overshooting or undershooting noise pulses to cause a latchup danger when the IC's are operated under normal conditions. In this work, a practical solution of using the stacked LVTSCR's has been successfully designed in bulk CMOS processes to safely apply the LVTSCR for component-level ESD protection without the fatal latchup trouble when the IC's are operating in system applications. The device characteristics, including the temperature dependence and the turn-on speed, of the stacked LVTSCR's in a 0.35-μm bulk CMOS process has been experimentally investigated in more detail. The holding voltage of the stacked LVTSCR's can be linearly adjusted by changing the number of the LVTSCR devices in the stacked configuration for different applications.

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