Investigation of the Gate-Driven Effect and Substrate-Triggered Effect on ESD Robustness of CMOS Devices

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***Abstract*—The gate-driven effect and substrate-triggered effect on electrostatic discharge (ESD) robustness of CMOS devices are measured and compared in this paper. The operation principles of gate-grounded design, gate-driven design, and substrate-triggered design on CMOS devices for ESD protection are explained clearly by energy-band diagrams. The relations between ESD robustness and the devices with different triggered methods are also explained by transmission line pulsing (TLP) measured results and energy-band diagrams. The turn-on mechanisms of nMOS devices with triggered methods are further verified using the emission microscope (EMMI) photographs of the nMOS devices under current stress. The experimental results confirm that the substrate-triggered design can effectively and continually improve ESD robustness of CMOS devices better than the gate-driven design. The human body model (HBM) ESD level of nMOS with a W/L of 400 μm/0.8 μm in a silicided CMOS process can be improved from the original 3.5 kV to over 8 kV by using the substrate-triggered design. The gate-driven design cannot continually improve the ESD level of the device in the same deep-submicron CMOS process.**

***Index Terms*—Energy-band diagram, ESD (electrostatic discharge), gate-driven effect, substrate-triggered effect.**

I. Introduction

TO SUSTAIN reasonable electrostatic discharge (ESD) robustness in deep-submicron CMOS ICs, on-chip ESD protection circuits must be added into the chips [1]. The ESD level of commercial IC products is generally required to be higher than 2 kV in human body model (HBM) ESD stress [2]. The typical design of efficient ESD protection circuits in a CMOS IC to protect the internal circuits against ESD damage is shown in Fig. 1 [3]. To sustain the required ESD level, on-chip ESD protection circuits are often drawn with larger device dimensions. Such ESD protection devices with larger device dimensions are often realized with multiple fingers to reduce total layout area [4]. An example of finger-type nMOS is shown in Fig. 2. To design the area-efficient ESD protection circuits in Fig. 1, the ESD protection devices need to be as robust as possible in a limited layout area.

To improve the turn-on uniformity among those multiple fingers, the gate-driven design [5]–[8] and substrate-triggered design [9]–[12] have been reported to increase ESD robustness of the large-device-dimension nMOS. Recently, ESD robustness of the gate-driven nMOS has been found to be decreased dramatically when the gate voltage is somewhat increased [8], [13]. The gate-driven design causes large ESD current discharging through the strong-inversion channel of the nMOS [14], therefore the nMOS is easily burned out by ESD energy. However, with the substrate-triggered design, the parasitic

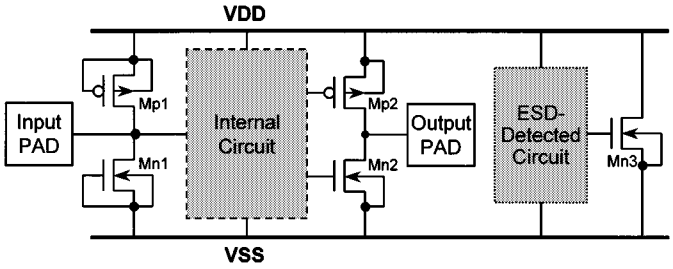

Fig. 1. Typical on-chip ESD protection circuits in a CMOS IC.

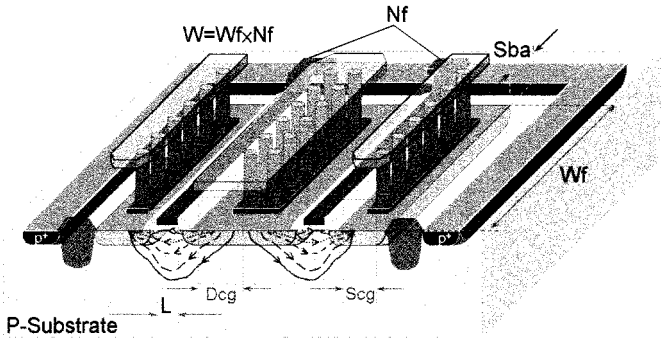

Fig. 2. 3-D structure of finger-type nMOS device with layout parameters.

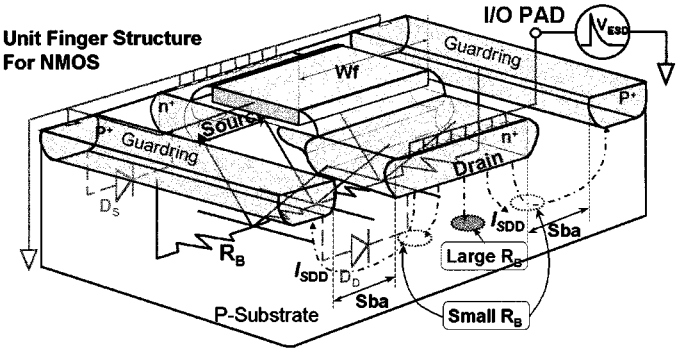

Fig. 3. Illustration of the parasitic devices and layout parameters in a unit-finger structure of a multiple-finger nMOS.

Manuscript received November 30, 2000; revised January 15, 2002. This work was supported in part by the National Science Council (NSC), Taiwan, R.O.C., under Grant NSC-89-2215-E-009-103, and in part by Taiwan Semiconductor Manufacturing Company.

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Publisher Item Identifier S 1530-4388(01)11420-4.

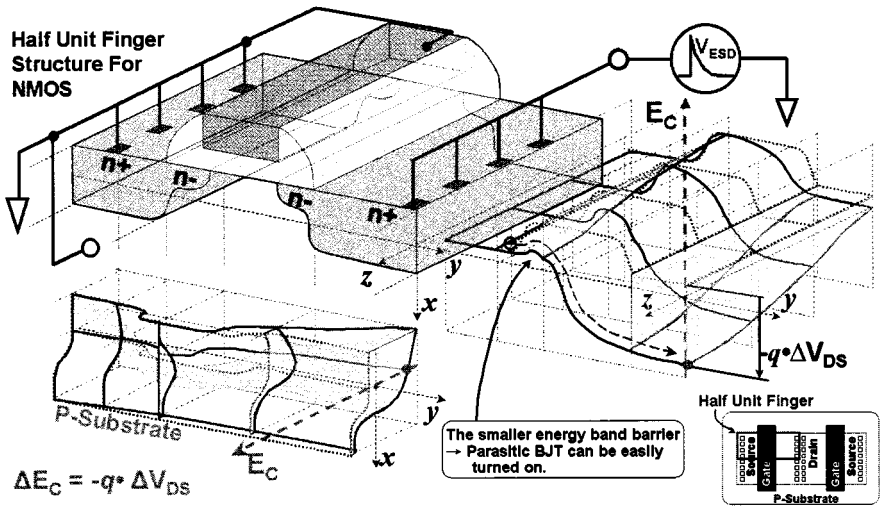

Fig. 4. Analysis of conduction energy-band diagrams for a half unit-finger nMOS during positive ESD stress.

lateral bipolar junction transistor (BJT) of the MOSFET can sustain higher ESD current than the gate-driven MOSFET.

To analyze and explain the failure mechanisms of device under ESD stress, some simulation methods have been developed [15], [16]. In this work, the gate-grounded, gate-driven, and substrate-triggered designs used in the ESD protection circuits are investigated in more detail [17]. To clearly understand the physical mechanisms of ESD current distribution in the device, TLP measured I–V curves, energy-band diagrams, and emission microscope (EMMI) photographs are used to explain the current distribution along MOSFET under the gate-grounded, gate-driven, or substrate-triggered designs. In the literature, the energy-band analysis is first used in this paper to explain the ESD robustness of CMOS devices under ESD stress. The substrate-triggered design has been confirmed to be a good choice to improve ESD robustness of CMOS devices in sub-quarter-micron CMOS technologies.

II. Turn-On Mechanism of MOSFET Under ESD Stress

To illustrate the turn-on behavior of the gate-grounded MOSFET during ESD stress, one unit-finger structure of a multiple-finger nMOS device is shown in Fig. 3. In this structure, two parasitic diodes $D_{\rm S}$ and $D_{\rm D}$ can be found in the p–n junctions between source/drain and guardring of Fig. 3. When the p-type substrate guardring, sources, and gate of this nMOS are connected to ground, the parasitic diode $D_{\rm D}$ between drain and substrate is reverse biased under the positive ESD stress $(V_{\rm ESD})$ in Fig. 3. Some reverse-biased current $(I_{\rm SDD})$ in Fig. 3 can flow into the substrate during the positive ESD stress on the drain of the nMOS. The parasitic lateral BJT with a base resistance $R_{\rm B}$ can be found under the nMOS, as shown in Fig. 3. The reverse-biased current can increase base voltage of the parasitic lateral BJT. Due to the different distances from the base region to the substrate guardring, the base voltage of parasitic lateral BJT in the central region of finger-type nMOS is higher than that in the sided regions in Fig. 3. When the base voltage in the central region is increased up to trigger on the parasitic lateral BJT, the nMOS will enter into its snapback region. Under higher ESD stress, the turned-on region may be extended with more area in each finger of nMOS. But, the lateral BJT in the central region of nMOS is often first triggered into snapback to cause the nonuniform turn-on issue among the multiple fingers of nMOS device.

To understand the turn-on behavior of the parasitic lateral BJT in nMOS, the energy-band diagrams of half unit-finger nMOS device under ESD stress are analyzed in Fig. 4. To simply analyze the variation of energy-band diagrams, only conduction band variations on the x–y and y–z planes along the half unit-finger structure are illustrated in Fig. 4. Because the voltage drop implies negative variation of energy band, the electrons flow from source to drain can be understood from Fig. 4. The related dependence between voltage drop variation and energy variation is expressed as

$$\Delta E_C = -q \cdot \Delta V_{\rm DS}. \tag{1}$$

Because the reverse-biased current pulls down the energy band of the base region in the parasitic lateral BJT, the depletion layer of the reverse-biased junction can modulate the base width. The lower energy-band barrier and shorter effective base width cause the fast turn-on of the parasitic lateral BJT at the central region of the nMOS. Therefore, during positive ESD stress, the multiple fingers of nMOS cannot be uniformly turned on. Only some regions of several fingers in the nMOS were turned on and therefore damaged by ESD.

To verify the turn-on uniformity, different current pulses are applied to the drain of a gate-grounded nMOS, which has a $W/L = 300\,\mu{\rm m}/0.5\,\mu{\rm m}$ in a 0.35-μm silicided CMOS process. The measurement setup is shown in Fig. 5(a), where the current pulse has different pulse heights. The corresponding I–V curve of the gate-grounded nMOS is drawn in Fig. 5(b). The EMMI photographs on the gate-grounded nMOS during the stresses of different current pulses are shown in Fig. 5(c)–(k) to observe its turn-on behavior. From the hot spots in Fig. 5(c)–(f), the reverse-biased breakdown current in the gate-grounded nMOS is initially flowing toward the guardring. When the base potential is increased up to trigger on the parasitic lateral BJT, the hot spots become located at the central regions of the

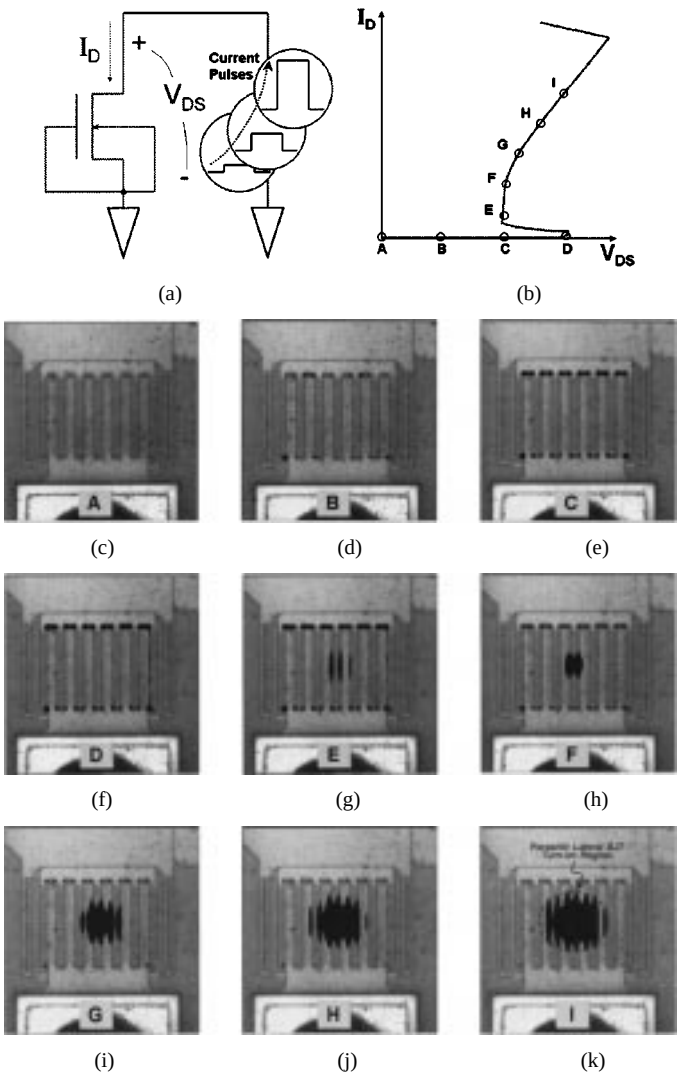

Fig. 5. EMMI photographs on a gate-grounded nMOS ($W/L = 300\ \mu\text{m}/0.5\ \mu\text{m}$) to show its turn-on behavior under the stress of different pulsed currents. (a) The measurement setup. (b) The corresponding I–V curve of a gate-grounded nMOS. (c)–(f) The hot spots in the gate-grounded nMOS before it enters into the snapback region. (g)–(k) The hot spots in the gate-grounded nMOS after it enters into the snapback region.

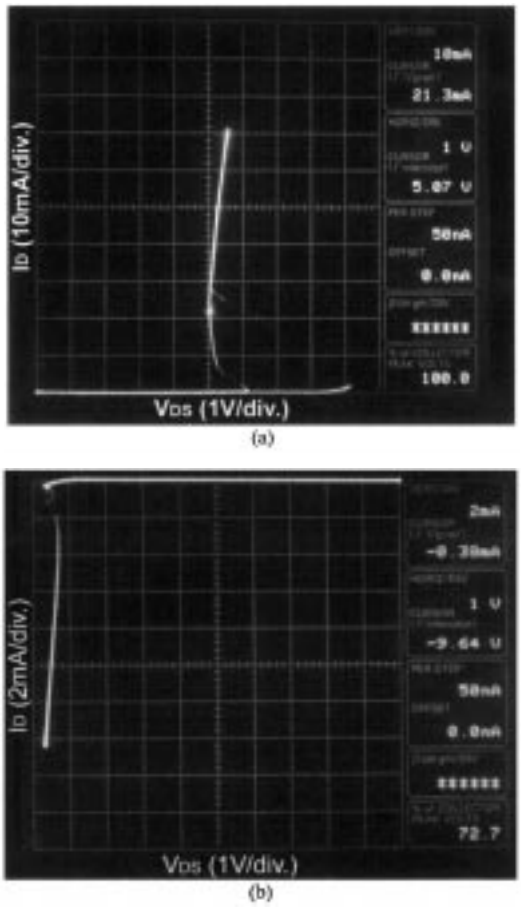

Fig. 6. Measured snapback I–V curves of (a) nMOS and (b) pMOS, with a channel length of 0.35 μm.

finger-type nMOS, as those shown in Fig. 5(g)–(k). Because the short-channel nMOS has an obvious snapback I–V curve, as that shown in Fig. 6(a), the turned-on central fingers in Fig. 5(k) cause the ESD current to mainly discharge through those fingers. If the turned-on region cannot be extended to the full regions of all fingers before a second breakdown occurs in nMOS, the turned-on central region in Fig. 5(k) will be burned out by the overheating ESD current. This often causes a low ESD level, even if the multiple-finger nMOS has a large device dimension. On the contrary, the pMOS has no obvious snapback I–V curve, as that shown in Fig. 6(b). The pMOS eventually has a good uniform turn-on efficiency.

Depending on the doping profile of impurities in the channel region and some layout parameters of the MOSFET, the external ESD voltage can lower the energy band of the surface channel or turn on the parasitic lateral BJT. Generally, there are three main current paths in the MOSFET during ESD stress. The first path is the strong-inversion current along the surface channel of the MOSFET when some positive voltage is biased at the gate [14], [18]. This current path is shown as Path1 in Fig. 7(a). The second path is formed by the drain-induced barrier lowering in the LDD region near the surface channel, as Path2 shown in Fig. 7(b), where the gate is biased at 0 V. The third path is formed by the parasitic lateral BJT in the MOSFET [14], but it is far away from the channel surface of the MOSFET, which is shown as Path3 in Fig. 7(c) with a 0-V gate bias. During positive ESD stress, a high voltage is applied on the drain of the MOSFET and pulls down the energy band of the drain. The corresponding two-dimensional (2-D) energy-band diagrams on the x–y plane of nMOS under different conditions are illustrated in Fig. 7(d) with a positive gate bias, in Fig. 7(e) with lowered energy band near LDD, and in Fig. 7(f) with lowered energy band far away from the surface, respectively [14], [19]. Three electron flow paths (Path1, Path2, and Path3) have been clearly indicated in those band diagrams. To further understand such turn-on paths, one-dimensional (1-D) energy-band diagrams along the A–A' lines of Fig. 7(a)–(c) in the x-axis direction are drawn in Fig. 7(g)–(i), respectively. A high electric field across the gate oxide can be found in Fig. 7(g) and (h), but it is not found in Fig. 7(i) during ESD stress. With different current paths, the nMOS during ESD stress may be damaged by different failure mechanisms. However, the gate or substrate biases of MOSFET can affect the current paths along the MOSFET during ESD stress. Therefore, the ESD robustness of MOSFET

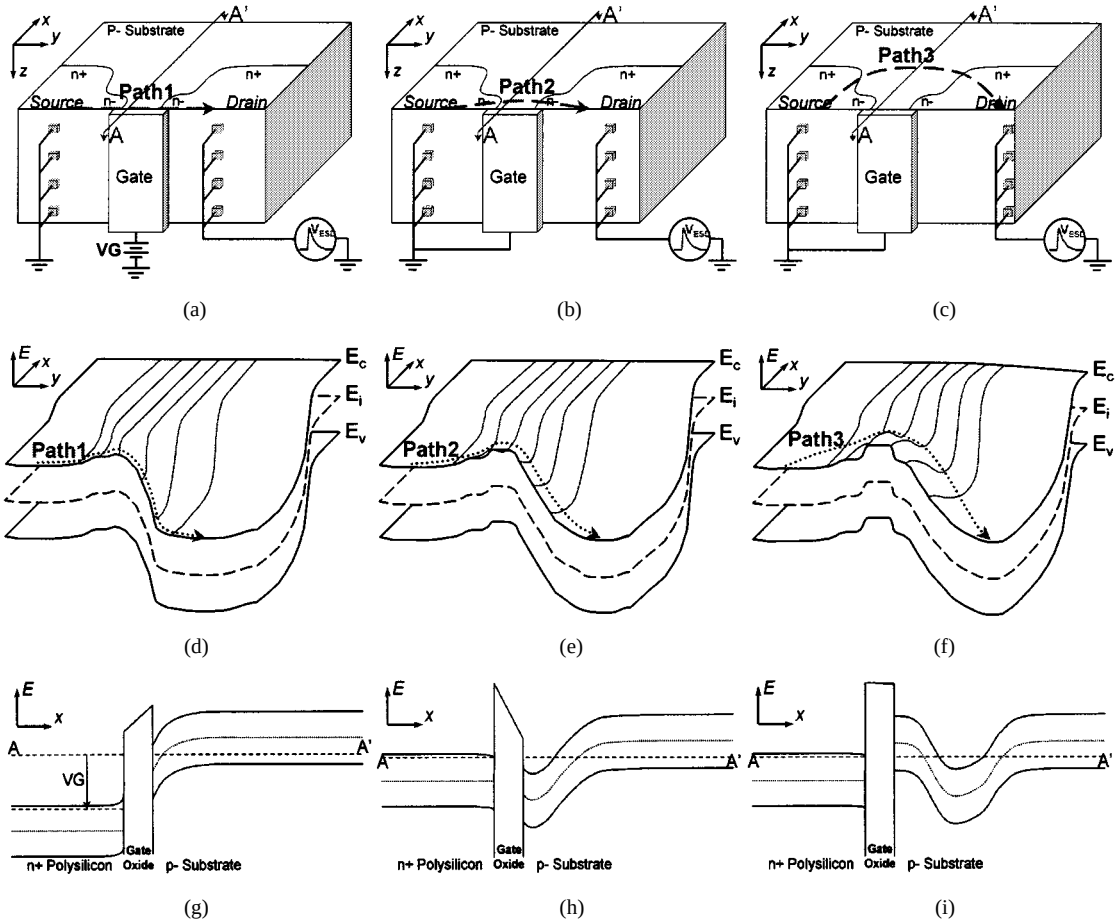

Fig. 7. Illustrations of energy-band diagram for a nonsilicided nMOS with different stress conditions. (a)–(c) Devices under different biases. (d)–(f) 2-D band diagrams of nMOS in the corresponding conditions of (a)–(c), respectively. (g)–(i) The x-axis band diagrams along the line A–A' of nMOS in (a)–(c), respectively. A gate voltage V_G is applied on the gate of nMOS in (a).

can be further improved by the gate-driven or the substrate-triggered designs.

III. Gate-Grounded MOSFET

To understand the benefit of gate-driven or substrate-triggered designs, the ESD robustness of gate-grounded nMOS must be first investigated. Some layout parameters can affect ESD robustness of the ESD protection device [13]. The main layout parameters that affect ESD robustness of CMOS devices are the channel width (W), the channel length (L), the clearance from contact to poly-gate edge at drain and source regions ($D_{\rm cg}$ and $S_{\rm cg}$), the spacing from the drain diffusion to the guardring diffusion $(S_{\rm ba})$, and the finger width $(W_{\rm f})$ of each unit finger, which have been indicated in Fig. 2 with the three-dimensional (3-D) device structure. To clearly compare with the triggered techniques, only the channel-width variation of gate-grounded MOSFET is considered in this investigation. The ZapMaster ESD tester, produced by Keytek Instrument Corporation, is used to measure the HBM ESD level of the fabricated test chips. The failure criterion is generally defined at 1-μA leakage current under $1.1 \times V_{\rm DD}$ bias, when the device is kept off. The experimental results are measured and discussed in the following. To investigate the turn-on behavior of device during high ESD current stress, the TLP technique has been widely used to measure the second breakdown characteristics of devices [20], [21]. The TLP measured results are also shown and analyzed in the following.

To discharge more ESD current, the channel widths of the ESD protection devices are often designed with larger dimensions. However, if nonuniform turn-on effect is considered, the MOSFET with a larger channel width cannot sustain high ESD level as expected. The nMOS and pMOS devices with different channel widths W have been fabricated in a 0.35-μm silicided CMOS process. Each unit-finger width $W_{\rm f}$ of the nMOS and pMOS devices in this investigation is kept as 50 μm. The nMOS and pMOS devices with or without the resist protection oxide (RPO) layer [22] to block the silicided diffusion on the drain region are also drawn in the test chips to investigate their ESD levels. For both nMOS and pMOS devices in this investigation, the channel length L, the clearance from the drain contact to poly-gate edge $D_{\rm cg}$, the clearance from the source contact to poly-gate edge $S_{\rm cg}$, and the spacing from the drain diffusion to the guardring diffusion $S_{\rm ba}$ are kept at 0.8, 3, 1, and 4 μm, respectively.

To analyze the second breakdown characteristics of nMOS, the transmission line pulsing generator (TLPG) [20], [21] in Fig. 8(a) is used to measure the second breakdown current and the turn-on resistance of the nMOS. The corresponding circuit for TLPG measurement on a gate-grounded nMOS is shown in

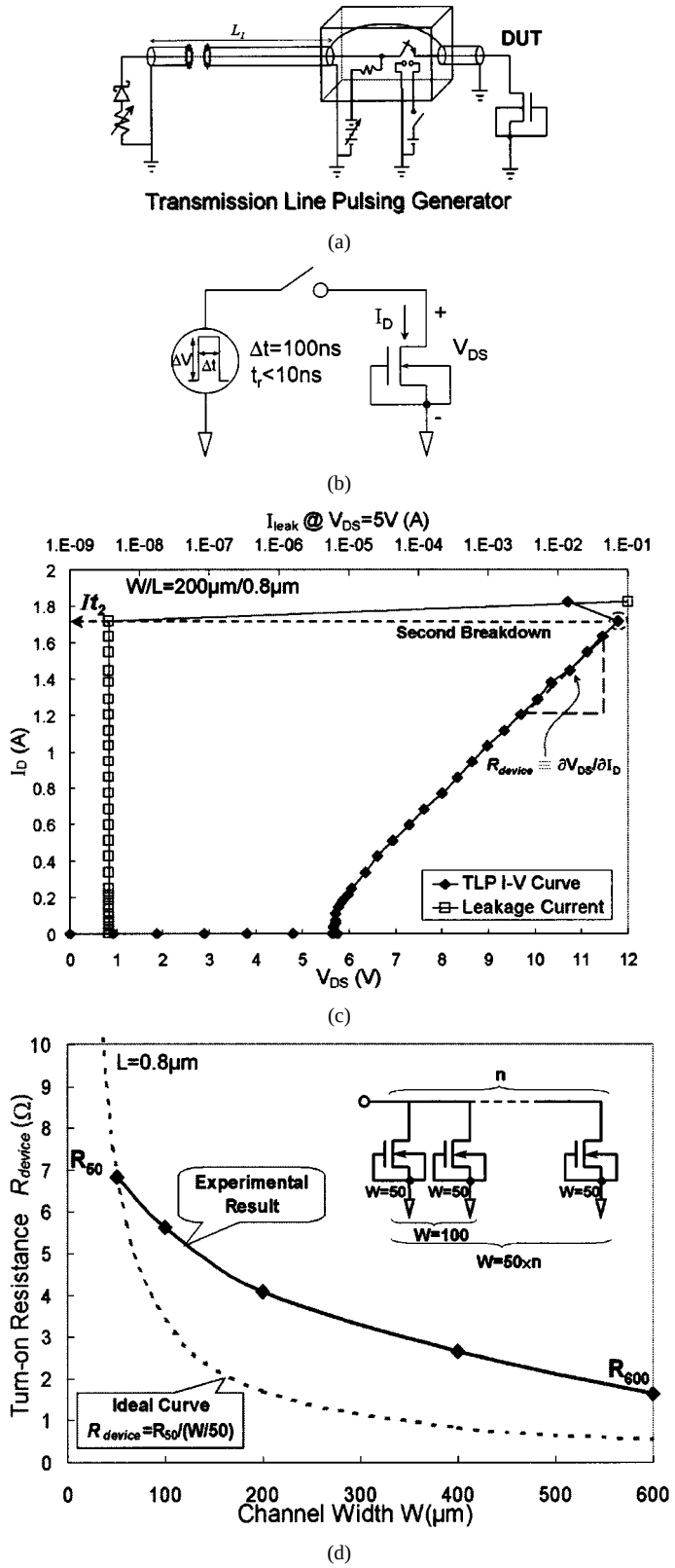

Fig. 8. (a) Illustration of transmission line pulsing generator (TLPG). (b) The corresponding circuit for TLPG measurement on a gate-grounded nMOS. (c) The measured I–V characteristics and leakage currents of nMOS by TLP with a pulse width of 100 ns. (d) The turn-on resistances of finger-type nMOS devices with different channel widths, but with the same unit-finger width and channel length.

Fig. 8(b). The measured I–V characteristics and leakage currents of nMOS with $W/L = 200\ \mu\text{m}/0.8\ \mu\text{m}$ by TLP with a pulse width of 100 ns are shown in Fig. 8(c). The second breakdown current is indicated as It_2 in Fig. 8(c). The turn-on resistance is defined as the voltage variation over current variation before second breakdown in the TLP measured I–V curve. The turn-on resistance can be expressed as

$$R_{\text{device}} \equiv \frac{\partial V_{\text{DS}}}{\partial I_{\text{D}}}. \tag{2}$$

From the TLP measured results, the relation between second breakdown current (It_2) and HBM ESD level (V_{ESD}) can be approximated as [23], [24]

$$\text{HBM}V_{\text{ESD}} \approx (1500 + R_{\text{device}}) \cdot It_2. \tag{3}$$

The turn-on resistances of finger-type nMOS devices with different channel widths, but with the same unit-finger width and channel length, are shown in Fig. 8(d). For an nMOS with 50-μm channel width, the turn-on resistance R_{50} in Fig. 8(d) is 6.83 Ω. If the nMOS with longer channel width can be uniformly turned on, the dependence between the turn-on resistance and the channel width can be drawn as the ideal curve (dashed line) in Fig. 8(d). In the ideal case, the turn-on resistance of nMOS with 600-μm channel width must be only 0.57 Ω. But, the experimental result on the turn-on resistance $R_{600}(= 1.64\ \Omega)$ of nMOS with 600-μm channel width in Fig. 8(d) is far from the ideal turn-on resistance. It implies that the finger-type gate-grounded nMOS device with a longer channel width cannot be uniformly turned on during ESD stress.

The relations between the device channel widths W and the HBM ESD level of nMOS and pMOS devices in a 0.35-μm CMOS process have been experimentally investigated in Fig. 9(a) and (b), respectively. In Fig. 9(a), the nMOS is tested under the positive-to-V_{SS} ESD stress, whereas the pMOS is tested under the negative-to-V_{DD} ESD stress in Fig. 9(b). In Fig. 9(a), the HBM ESD level of the nMOS device is increased while the device channel width is increased. If the device channel width is increased, more fingers have to be drawn and connected in parallel to form the large-dimension nMOS device. The ESD robustness of such large-dimension device may be increased while the device channel width is increased. But, in Fig. 9(a), the ESD level (3.4 kV) of the silicide-blocking nMOS with a channel width of 600 μm is less than that (3.5 kV) of the nMOS with a channel width of 400 μm. This is due to the nonuniform turn-on issue among the multiple fingers of a large-dimension device. In the finger-type nMOS, if the base current cannot uniformly trigger on the distributed parasitic lateral BJTs of the nMOS, the ESD current will be concentrated in some local regions to cause the nonuniform turn-on phenomena in the nMOS under ESD stress, as those shown in Fig. 5.

In Fig. 9(b), the HBM ESD levels of the pMOS with or without silicided diffusion are both increased as the device channel width is increased. The ESD level of the silicided pMOS with a channel width of 400 μm is around -2.45 kV, but that of the silicide-blocking pMOS with the same device dimension and layout style is -4.45 kV. This verifies the effectiveness of the silicide-blocking process used to improve ESD

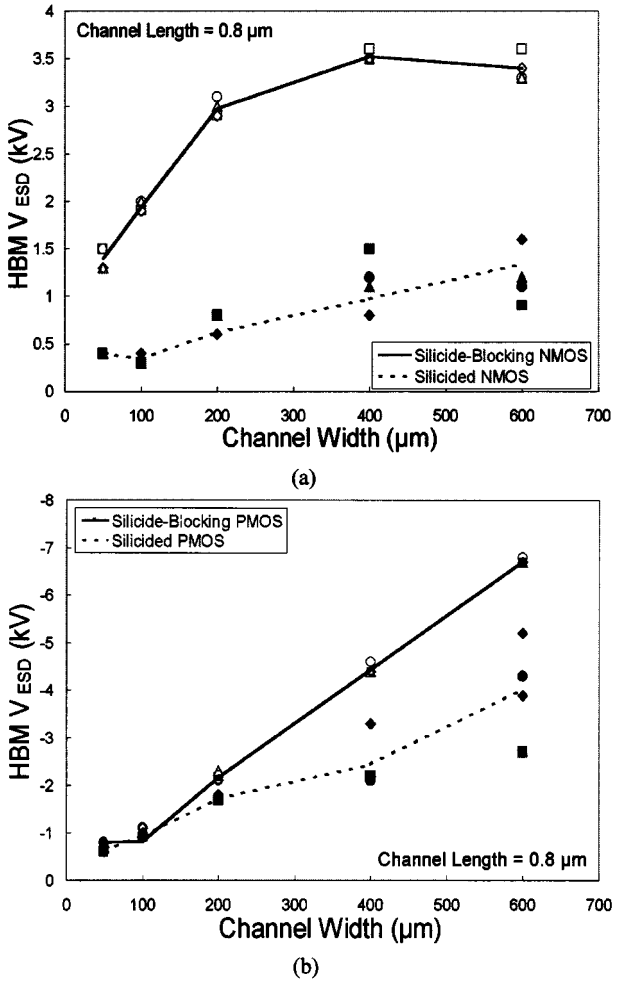

Fig. 9. Dependence of HBM ESD level on the channel width of (a) nMOS and (b) pMOS, with or without silicided diffusion.

level in deep-submicron CMOS technologies. The continued increase of ESD level, when the channel width of pMOS has been increased, is due to the decreased snapback characteristics of the pMOS. The snapback I–V characteristic of a pMOS was shown in Fig. 6(b). Comparing the I–V curves between Fig. 6(a) and (b), the pMOS with less snapback characteristics causes a more turn-on uniformity among its multiple fingers. Therefore, it has a continued increase on its ESD level, when the channel width of pMOS is increased.

The nMOS with silicide-blocking process (without silicided diffusion) can sustain a higher ESD level than that with the silicided diffusion [25]. NMOS devices with or without silicide silicided diffusion have different turn-on resistances in the TLP-measured I–V curves of Fig. 10. The turn-on resistance of the silicided nMOS with $W/L = 200\ \mu\text{m}/0.8\ \mu\text{m}$ is only 2.45 Ω, but that of the silicide-blocking nMOS with the same device dimension and layout style is 4.06 Ω. However, the It_2 of the silicide-blocking nMOS is 103% higher than that of the silicided nMOS.

The silicide diffusion on the drain of MOSFET can decrease the ballast resistance of the device structure [25] and change the current distribution in the device. The mainly ESD current in the silicided nMOS is concentrated in the channel surface

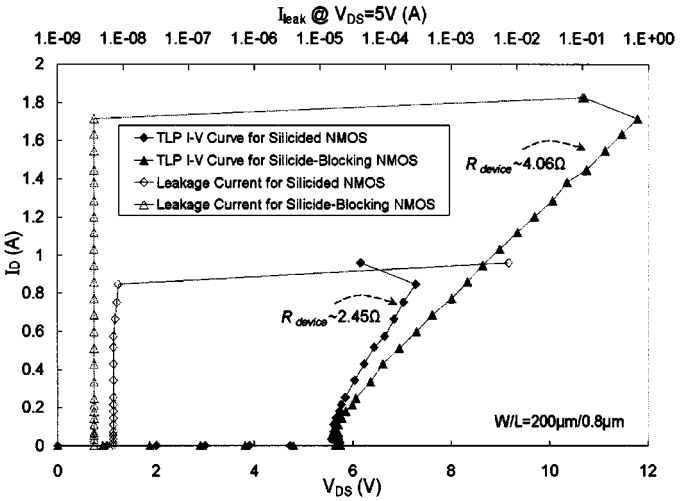

Fig. 10. TLP measured I–V curves of nMOS devices with or without silicided diffusion, but with the same device dimension of $W/L = 200\ \mu\text{m}/0.8\ \mu\text{m}$.

of the nMOS, but it can be away from the channel surface in the silicide-blocking nMOS. Because the nMOS devices with or without silicided diffusion have different failure mechanisms, the silicide-blocking nMOS can sustain much higher HBM ESD stress in the experimental results of Fig. 9. The average ESD level of the silicided nMOS with a channel width of 200 μm is only 0.57 kV, but that of the silicide-blocking nMOS with the same device dimension and layout style is 3 kV.

To explain the degradation of ESD robustness of the silicided nMOS device, the energy-band diagrams of nMOS with or without the silicided diffusion are compared in Fig. 11(a) and (b). A positive ESD stress is applied to the drain of the nMOS, whereas the gate, source, and bulk of the nMOS are connected to ground. The energy-band diagrams are analyzed along both the lines A–A' and B–B' in Fig. 11(a) with silicided diffusion, and in Fig. 11(b) without silicided diffusion. The $E_{\rm C}$ and $E_{\rm V}$ in Fig. 11 are the conduction and valence energy levels, respectively. The regions G and S in Fig. 11 are defined as the effective current discharging regions near the channel surface and in the deep substrate of the nMOS under positive ESD stress. From Fig. 11(a), the drain voltage can pull down the band diagram at the drain silicided diffusion because of the silicided diffusion with a low resistance and close to the LDD structure. The major voltage drop of drain bias $V_{\rm DS}$ is located along the surface channel of the MOSFET. Therefore, the energy band on the surface channel will be lowered. This effect of drain-induced barrier lowering can enhance the channel current forming in the nMOS device. Major ESD current will flow into the turned-on region G in Fig. 11(a), which is very close to the interface between the gate oxide and the surface channel of the nMOS. With a shallower current path in the device, the ESD current can easily damage the surface channel and the gate oxide of nMOS. But, a silicide-blocking diffusion can reduce the turn-on probability of Path2 in Fig. 7. The energy-band diagram in Fig. 11(b) can explain this phenomenon. The drain p–n junction near the surface channel is connected in series with a larger sheet resistance in the silicide-blocking nMOS, but the p–n junction at the bottom of drain diffusion has a smaller sheet resistance. The sheet resistance of silicide-blocking drain diffusion can reduce the voltage

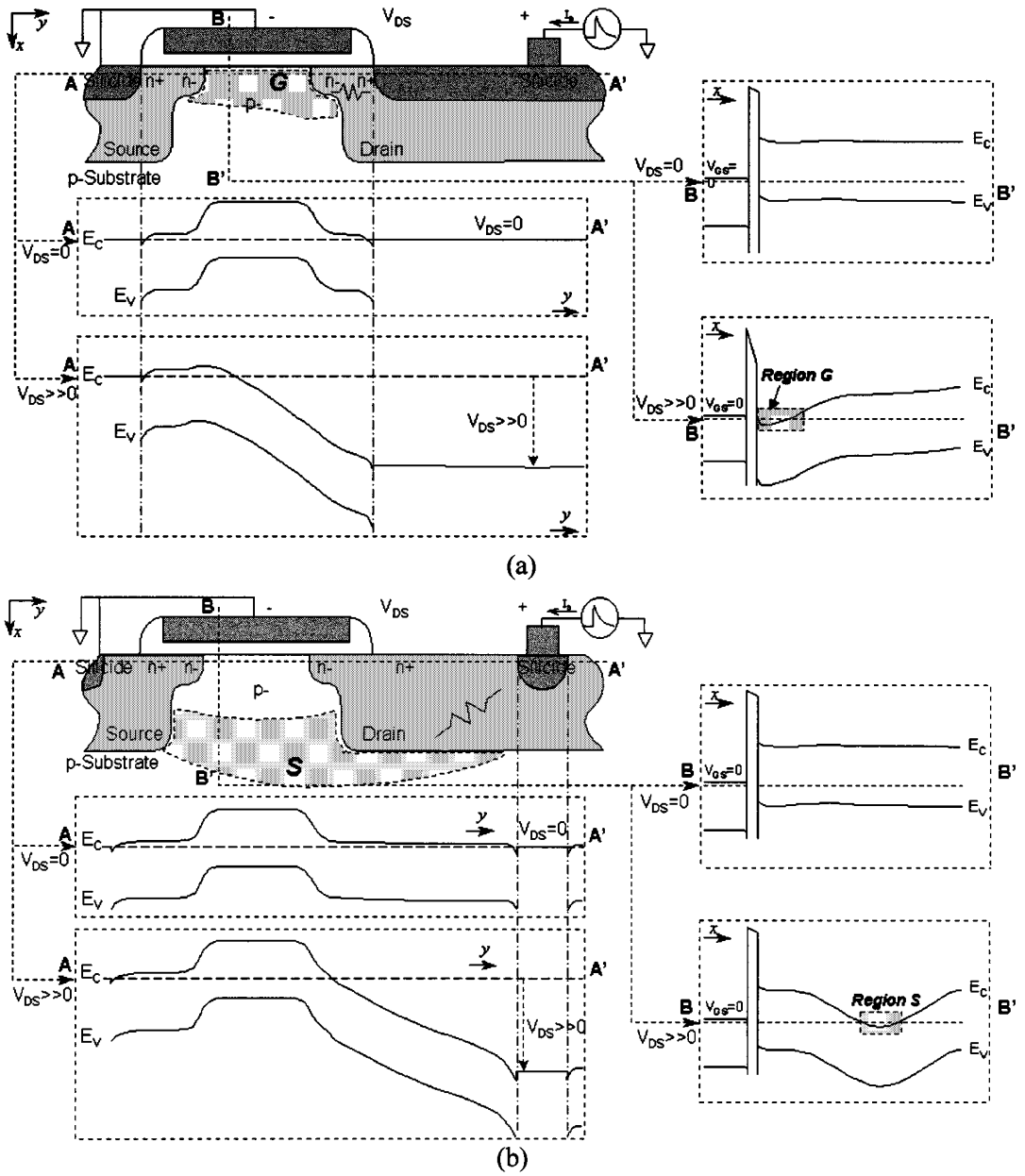

Fig. 11. Illustration of the variation on energy band of gate-grounded nMOS. (a) With silicided diffusion. (b) Without silicided diffusion.

drop on the channel surface. So, the ESD current is discharged through the parasitic lateral BJT, which is far away from the channel surface. The silicide-blocking drain diffusion can avoid ESD overstress on the surface channel and the gate oxide, therefore the silicide-blocking nMOS has a much higher ESD robustness.

IV. Gate-Driven Effect

To improve ESD robustness of the ESD protection devices, the gate-driven design had been reported to uniformly trigger on the multiple fingers of the large-dimension nMOS. But, the coupled voltage on the gate of the nMOS also turns on the strong-inversion channel of the nMOS, therefore the ESD current discharges through the channel region of the ESD protection nMOS. Due to the shallower junction depths and the LDD structure at the drain/source regions, the turned-on nMOS is weak to ESD stress [26].

To investigate this gate-driven effect, the sub-circuit inserted in Fig. 12 is used to measure ESD levels of the nMOS and pMOS under different gate biases. The layout parameters of nMOS and pMOS are the same as the data shown in Section III, but the gates of the MOSFETs are biased at different voltage levels. The different gate biases are applied to the gate of the MOSFET, and ESD voltage discharges into the drain of the MOSFET. In the 0.35-μm CMOS process, the HBM ESD levels on both the nMOS and pMOS devices with different channel widths W are shown in Fig. 12(a) and (b). The ESD level of the nMOS with $W = 600\,\mu$m is initially increased while the gate bias increases from 0 to 4 V. But the ESD level is suddenly decreased while the gate bias is greater than 6 V (8.5 V) for nMOS with the channel width of 200 μm (600 μm), as that shown in Fig. 12(a).

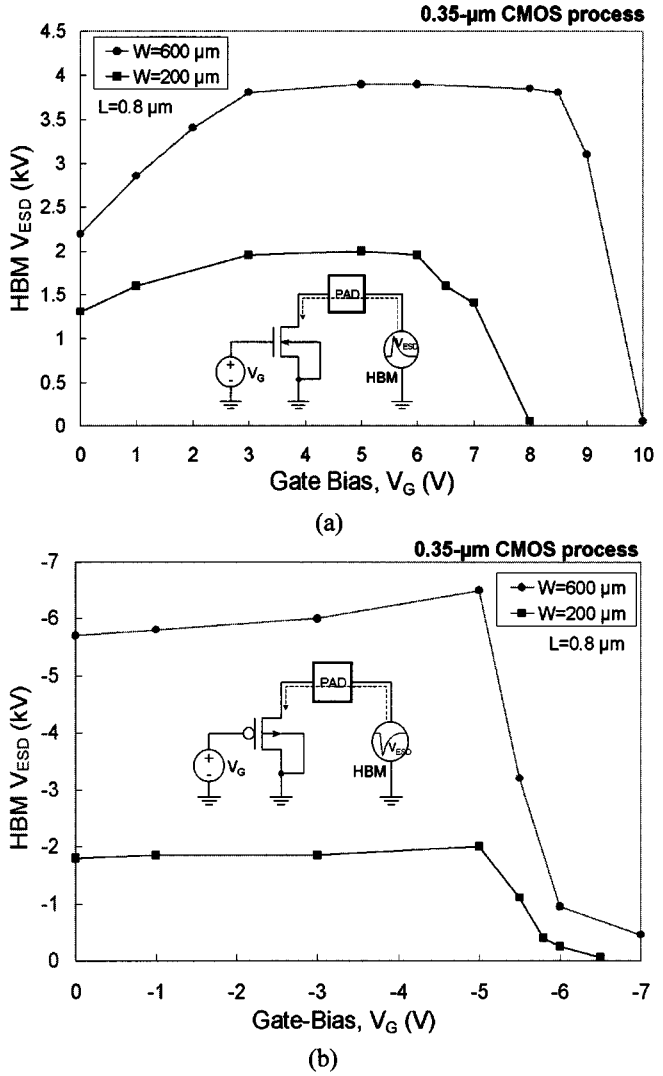

Fig. 12. Gate bias effect on the HBM ESD robustness of (a) nMOS and (b) pMOS, without silicided diffusion in a 0.35-μm silicided CMOS process.

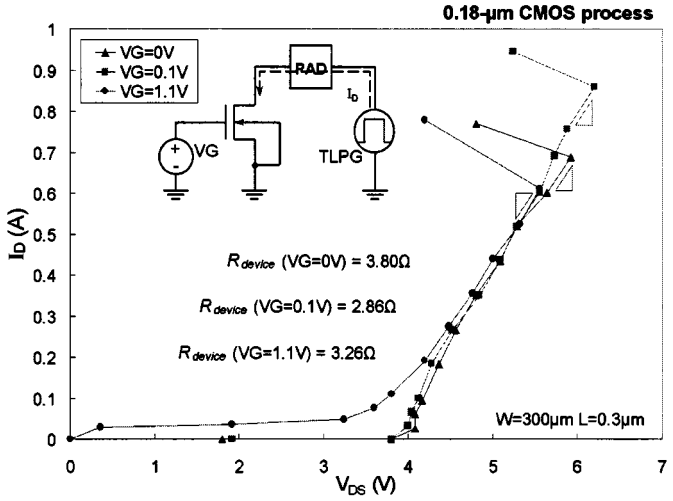

Fig. 13. TLP measured I–V curves and turn-on resistances of the gate-driven nMOS devices with silicide-blocking mask in a 0.18-μm salicided CMOS process.

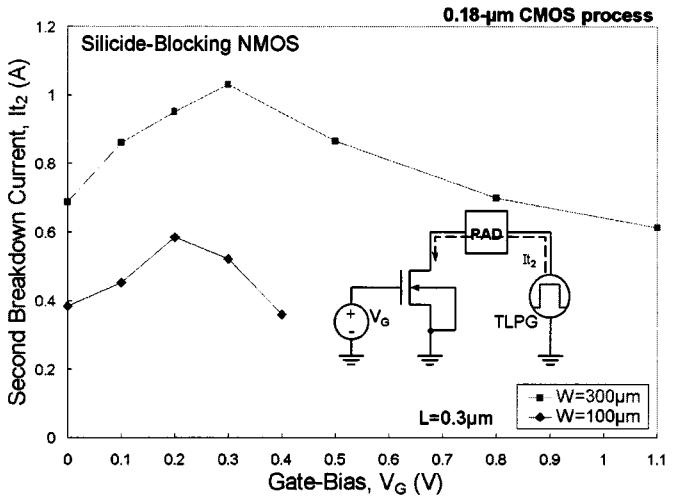

Fig. 14. Gate-driven effect on the second breakdown current of silicide-blocking nMOS in a 0.18-μm salicided CMOS process.

There is a similar gate-driven effect on the pMOS device. In Fig. 12(b), the ESD level (in absolute value) of the pMOS with $W = 600$ μm is initially increased while the gate bias changes from 0 to -5 V. But the ESD level is suddenly decreased while the gate bias is lower than -5 V. When the gate bias is increased up to some critical value, the ESD level of the nMOS or pMOS is suddenly decreased.

In a 0.18-μm salicided CMOS process, the TLP measured I–V characteristics of gate-driven nMOS ($W/L = 300$ μm/0.3 μm) with 0, 0.1, and 1.1-V gate biases are shown in Fig. 13. From the experimental results in Fig. 13, the turn-on resistance is decreased from 3.8 to 2.86 Ω when the gate bias is changed from 0 to 0.1 V. But the turn-on resistance is increased from 2.86 to 3.26 Ω when the gate bias is increased from 0.1 to 1.1 V. In the 0.18-μm salicided CMOS process, the dependences of second breakdown currents on the gate biases of nMOS with different channel widths are shown in Fig. 14. The second breakdown current of nMOS with $W = 300$ μm is initially increased from 0.69 to 1.03 A while the gate bias increases from 0 to 0.3 V. But the It_2 is suddenly decreased in Fig. 14 while the gate bias is only greater than 0.2 V (0.3 V) for nMOS with 100-μm (600-μm) channel width. Because only a very small voltage on the gate of the nMOS can degrade the ESD robustness of the nMOS, the gate-driven technique is hardly designed for ESD protection in the 0.18-μm salicided CMOS process.

To clearly explain the gate-bias effect, the energy-band diagrams of nMOS with different gate biases ($V_{GS} = 0$, $V_{GS} > 0$, $V_{GS} \gg 0$, and $V_{GS} \ggg 0$) are illustrated in Fig. 15. The same positive ESD stress is applied on the drain of nMOS for each case. The cross-sectional view of the nMOS device is shown in Fig. 15(a). Energy bands along the lines A–A', B–B', and C–C' of the nMOS in Fig. 15(a) are analyzed with the different gate biases, which are shown in Fig. 15(b) with $V_G = 0$, in Fig. 15(c) with $V_G > 0$, in Fig. 15(d) with $V_G \gg 0$, and in Fig. 15(e) with $V_G \ggg 0$, respectively. In the $V_{GS} = 0$ case, there is no coupled voltage on the gate of nMOS. The ESD current is discharged through the region S of the nMOS in Fig. 15(b). When the V_{GS} is increased by an external gate bias, the energy band of the channel surface in nMOS can be lowered by the gate bias

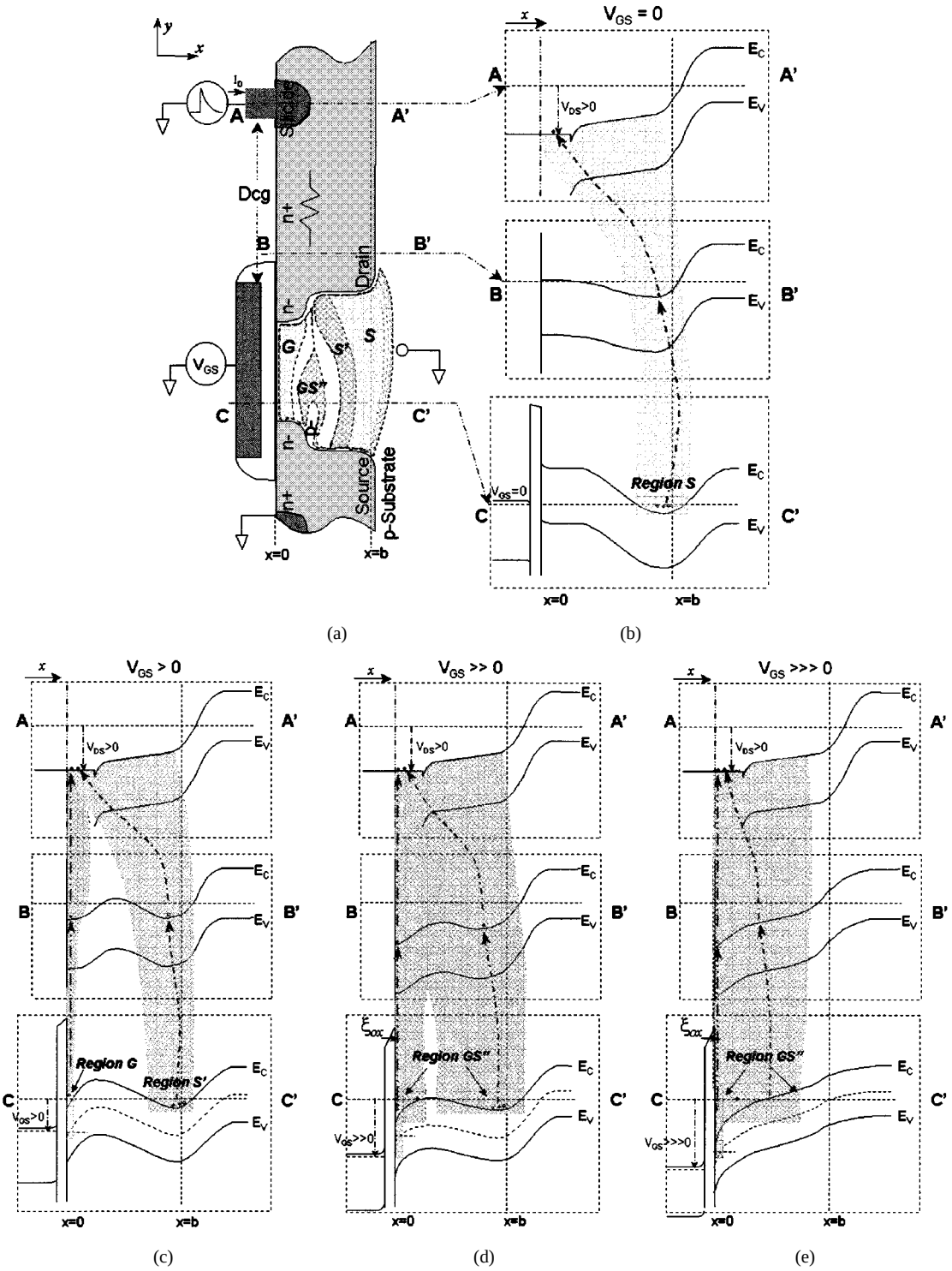

Fig. 15. Illustrations of (a) the gate-driven nMOS device structure, and the variation on energy band of the gate-driven nMOS with different gate biases of (b) $V_{\rm GS} = 0$, (c) $V_{\rm GS} > 0$, (d) $V_{\rm GS} \gg 0$, and (e) $V_{\rm GS} \ggg 0$.

$V_{\rm GS}$. If the gate bias is increased enough, channel current can be formed by accumulation charges in the region G of Fig. 15(c). Therefore, the ESD current is discharged through the region G and the region S′ in Fig. 15(c). So, the gate-driven nMOS has two current paths to discharge the ESD current. If the gate bias is continually increased, the discharge regions G and S′ will be extended and combined together as the merged region GS″ in Fig. 15(d). Then, the gate-driven ESD protection devices can sustain higher ESD robustness. But the turn-on mechanism depends on the impurities doping profiles in the region GS″ of the nMOS in Fig. 15(d). When a larger gate bias is applied on the gate of the nMOS, more ESD current is concentrated into the turn-on surface region in Fig. 15(e), where the larger electric field is built across the gate oxide. From the TLP measured I–V curves in Fig. 13, the increase of lower gate-driven voltage on the nMOS can decrease the turn-on resistance of the nMOS

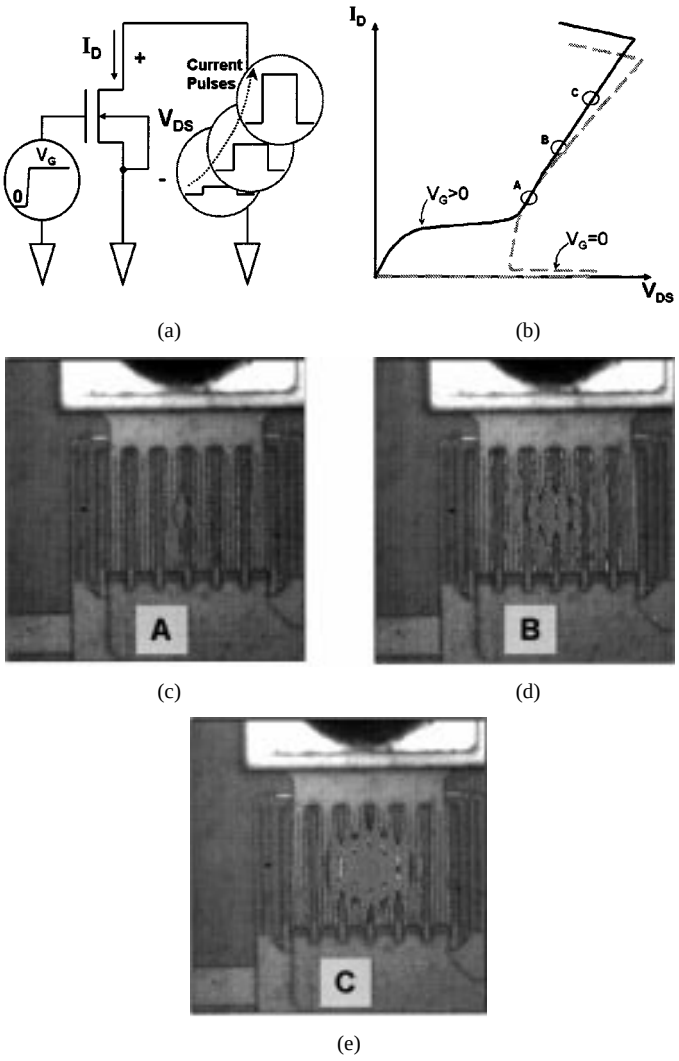

Fig. 16. EMMI photographs on a gate-driven nMOS ($W/L = 300\ \mu\text{m}/0.5\ \mu\text{m}$) to observe its turn-on behavior under the stress of different pulsed currents. (a) Measurement setup. (b) Corresponding I–V curve of a gate-driven nMOS. (c)–(e) Hot spots in the gate-driven nMOS under different current stresses.

during the TLP measurement. But, the higher gate bias causes an increase on the turn-on resistance of nMOS. These imply that the higher gate bias will concentrate the ESD current at a smaller turn-on region in the channel surface of nMOS and build a very high electric field across the gate oxide.

To observe the turn-on behavior of the gate-driven device, the gate of the nMOS is biased with a power supply and an increased current pulse is applied to its drain, as that shown in Fig. 16(a). The corresponding I–V curve of a gate-driven nMOS is drawn in Fig. 16(b). The EMMI photographs of the gate-driven nMOS with different stressed current pulses are shown in Fig. 16(c)–(e). From the hot spots in Fig. 16(c)–(e), the channels of all fingers can be uniformly turned on under any current pulse stress. But only some parasitic lateral BJTs in the central regions can be turned on during high current pulse stress, as that shown in Fig. 16(e). From the investigation of the EMMI photographs, the gate-driven technique can uniformly turn on the channel current but it cannot enhance the turn-on uniformity of parasitic lateral BJTs in the MOSFET.

To further discuss the gate-driven effect, the electric field (ξ_{ox}) across the gate oxide of MOSFET is increased by the accumulation charges and gate bias V_{GS}, as that shown in Fig. 15(d) and (e). The high electric field can easily destroy the gate oxide and damage the channel surface of the MOSFET. On the other hand, the doping profile of impurities under the gate oxide is an important factor to affect the quantities of channel current and the turn-on area of lateral BJT. If the doping profiles of impurities are adjusted, the gate-driven design can be further optimized for ESD protection. For another issue in the gate-driven design, coupled voltage on the gate of ESD protection device must be limited to avoid damaging the gate oxide and surface channel of the MOSFET. From the measured results in Figs. 12 and 14, the gate-coupled circuit used to improve ESD robustness of the ESD protection devices must be correctly optimized to avoid the sudden degradation on the ESD level of the gate-driven ESD protection devices.

V. Substrate-Triggered Effect

To avoid the sudden degradation of the ESD level of the gate-driven devices, the substrate-triggered design had been proposed to improve ESD robustness of the ESD protection devices. To investigate the substrate-triggered effect on ESD robustness of nMOS, different substrate currents are applied to the substrate of nMOS, and ESD current discharges into the drain of the nMOS. The HBM ESD levels of the substrate-triggered nMOS in a 0.35-μm silicided CMOS process are shown in Fig. 17(a) and (b) with different channel widths and lengths. The inserted sub-circuit shows the experimental setup to measure the substrate-triggered effect. In Fig. 17(a), the ESD level of the nMOS with a device dimension of $W = 400\ \mu$m and $L = 0.8\ \mu$m can be significantly increased from 3.5 kV to greater than 8 kV while the substrate current increases from 0 to 2.8 mA. In Fig. 17(b), the nMOS device $(W = 200\ \mu m)$ with a shorter channel length and higher substrate current can sustain a much higher ESD level. The ESD level of the nMOS with a channel length of 0.5 μm under 0-V gate bias and 0-A substrate current is only 2.8 kV, but the ESD level is increased up to 4.4 kV while the nMOS has a substrate current of 4 mA. As shown in Fig. 17, the ESD level is continually improved while the substrate current increases up to 4 mA.

In a 0.18-μm salicided CMOS process, the TLP measured I–V characteristics of substrate-triggered nMOS $(W/L = 300\ \mu\text{m}/0.3\ \mu\text{m})$ with 0-, 2-, and 8-mA substrate currents are shown in Fig. 18. From the experimental results in Fig. 18, the turn-on resistance is continually decreased from 3.92 to 2.73 Ω while the substrate current is changed from 0 to 8 mA. The substrate current can change the turn-on resistance of nMOS during ESD stress. It implies that substrate current can change the turn-on area or turn-on path of parasitic lateral BJT in the nMOS to sustain higher ESD stress. The dependence of It_2 on substrate current on the nMOS devices with different channel widths in a 0.18-μm salicided CMOS process are shown in Fig. 19. The second breakdown currents of nMOS with both $W = 300\ \mu$m and $W = 100\ \mu$m can be continually increased during high current pulse stress. The second breakdown current It_2 of the nMOS with a channel

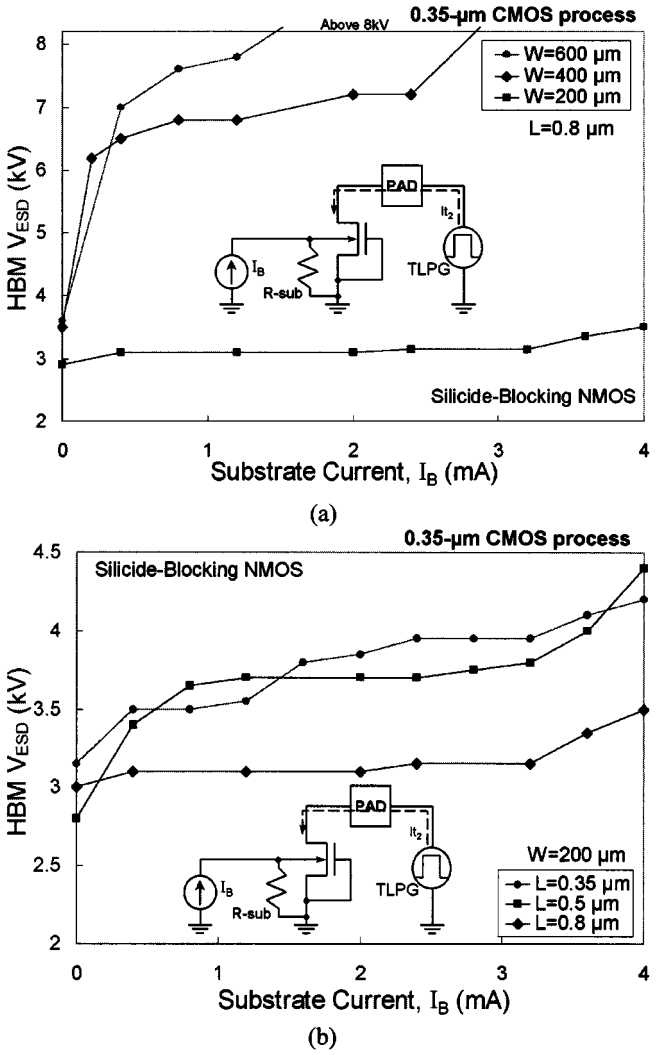

Fig. 17. Effect of substrate current on the ESD robustness of nMOS devices with (a) different channel widths and (b) different channel lengths, in a 0.35-μm silicided CMOS process.

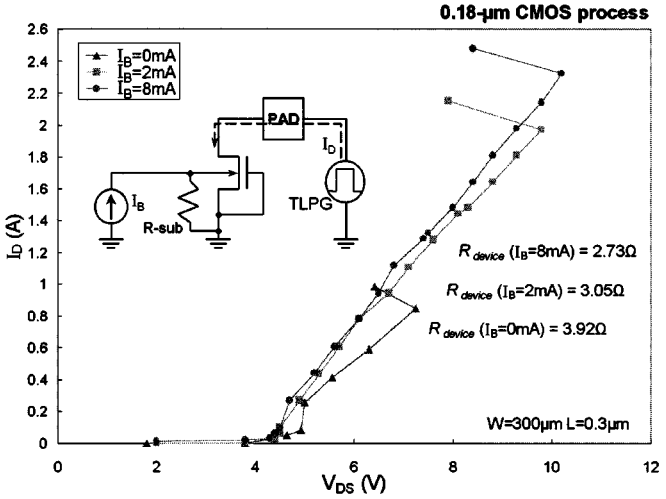

Fig. 18. TLP measured I–V curves and turn-on resistances of the substrate-triggered nMOS devices with silicide-blocking mask in a 0.18-μm salicided CMOS process.

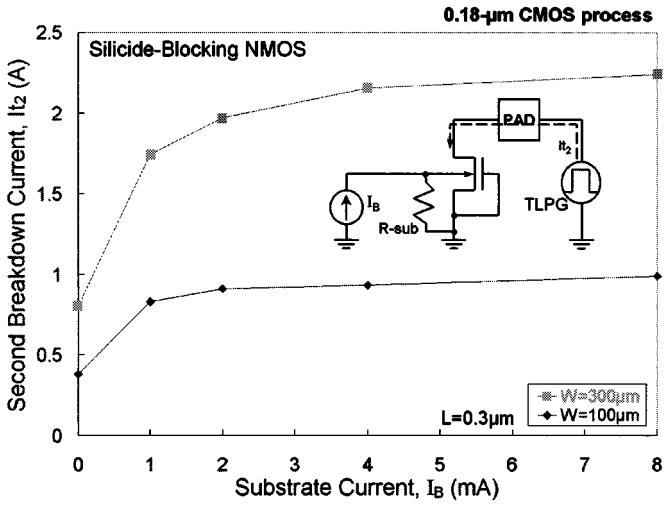

Fig. 19. Effect of substrate current on the ESD robustness of silicide-blocking nMOS devices with different channel widths in a 0.18-μm salicided CMOS process.

width of 300 μm under a 0-mA substrate current is only 0.8 A, but it is increased up to 2.2 A while the nMOS has a substrate current of 4 mA.

To explain the effect of substrate-triggered design, the energy-band diagrams with different substrate-triggered biases ($V_{\rm BS} = 0$, $V_{\rm BS} > 0$, and $V_{\rm BS} \gg 0$) under the same positive ESD stress are shown in Fig. 20. The energy-band diagrams along the lines A–A', B–B', and C–C' in Fig. 20(a) are analyzed in Fig. 20(b) with $V_{\rm BS} = 0$, in Fig. 20(c) with $V_{\rm BS} > 0$, and in Fig. 20(d) with $V_{\rm BS} \gg 0$. Comparing to the gate-driven design, there is no gate bias to lower the energy bands on the surface channel of the substrate-triggered nMOS as shown in Fig. 20(c) and (d). In Fig. 20(b), there is no substrate bias on the nMOS, so the current distribution region S of the parasitic lateral BJT in nMOS is smaller than those regions S′ and S″ of the substrate-triggered devices in Fig. 20(c) and (d). The substrate bias can lower the energy bands in the substrate region and extend the current distribution from the region S in Fig. 20(b) to the region S′ in Fig. 20(c) or the region S″ in Fig. 20(d). The device with substrate-triggered design has more and wider current distribution region in its device structure. Therefore, the device with higher substrate-triggered bias has more space for heat dissipation to sustain higher ESD stress. Therefore, substrate-triggered devices can sustain higher ESD robustness. From the above explanation, the turned-on region of parasitic lateral BJT can be extended into more area and be far away from the channel surface by the substrate bias in MOSFET. Therefore, the ESD protection devices with substrate-triggered design can have much higher ESD robustness in general CMOS technologies.

To verify the turn-on behavior of the substrate-triggered device, the substrate of the nMOS is biased with a power supply and an increased current pulse is applied to its drain, as that shown in Fig. 21(a). The corresponding I–V curve of a substrate-triggered nMOS is drawn in Fig. 21(b). The EMMI photographs of the substrate-triggered nMOS under different current pulses are shown in Fig. 21(c)–(e). From the hot spots in Fig. 21(c)–(e), the parasitic lateral BJTs of all fingers in nMOS can be uniformly turned on under any current pulse stress. All fingers of nMOS can be greatly turned on during high current

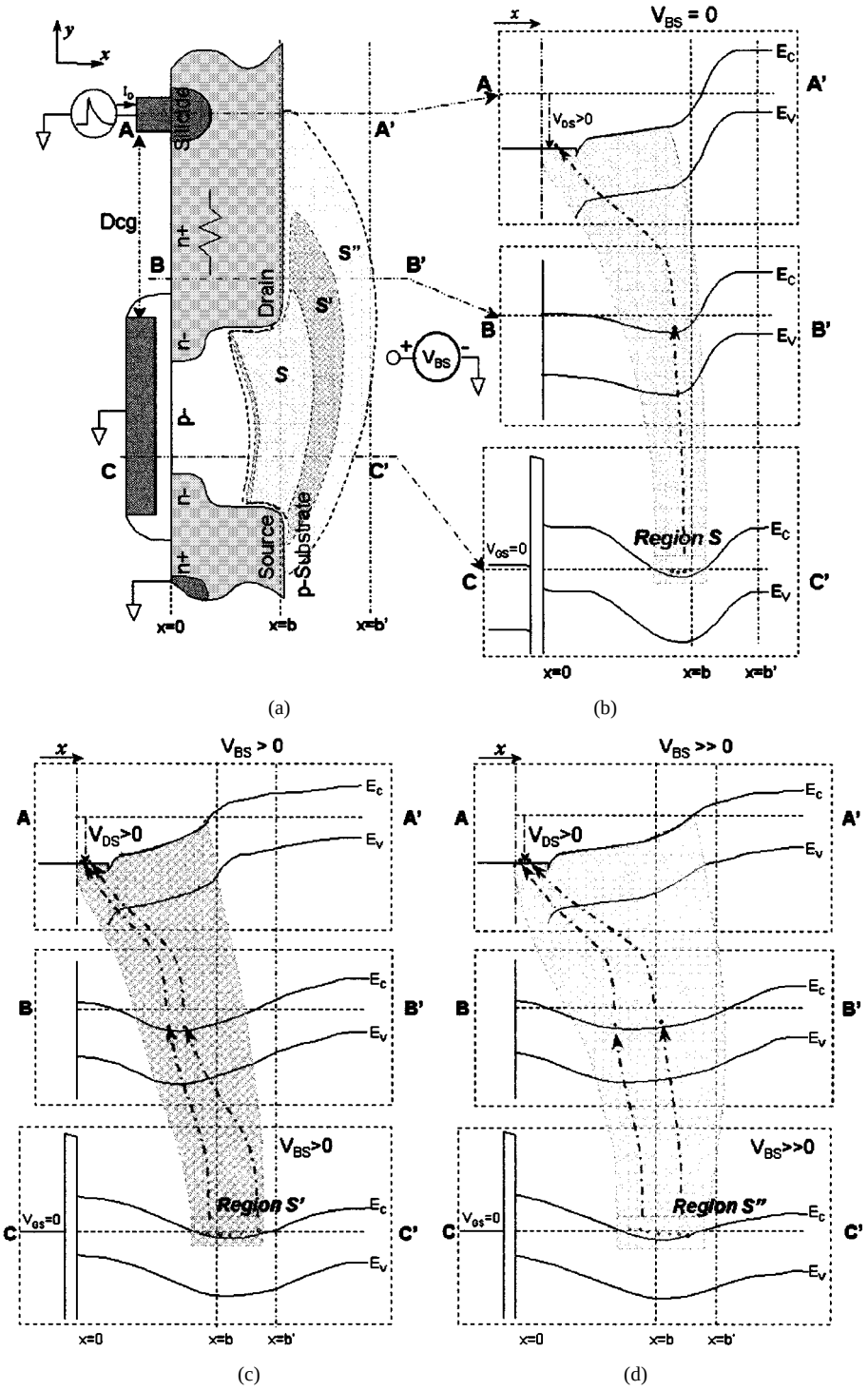

Fig. 20. Illustrations of (a) the substrate-triggered nMOS device structure, and the variation on energy band of the substrate-triggered nMOS with different substrate biases of (b) $V_{\rm BS} = 0$, (c) $V_{\rm BS} > 0$, and (d) $V_{\rm BS} \gg 0$.

pulse stress in Fig. 21(e). So, the substrate-triggered technique can uniformly turn on the parasitic lateral BJTs in the MOSFET during ESD stress.

The substrate-triggered design can effectively improve ESD robustness of the ESD protection devices without the sudden degradation as that in the gate-driven design. Therefore, this substrate-triggered design is more suitable to improve ESD robustness of the ESD protection devices and circuits in the sub-quarter-micron CMOS technologies.

VI. Conclusion

It has been proven that the gate-grounded large-dimension ESD protection devices cannot be uniformly turned on during ESD stress to sustain high ESD level as required. The gate-driven and substrate-triggered techniques can improve the ESD robustness of the large-dimension ESD protection devices. But the higher gate bias can induce larger channel current and higher electric field across the gate oxide to

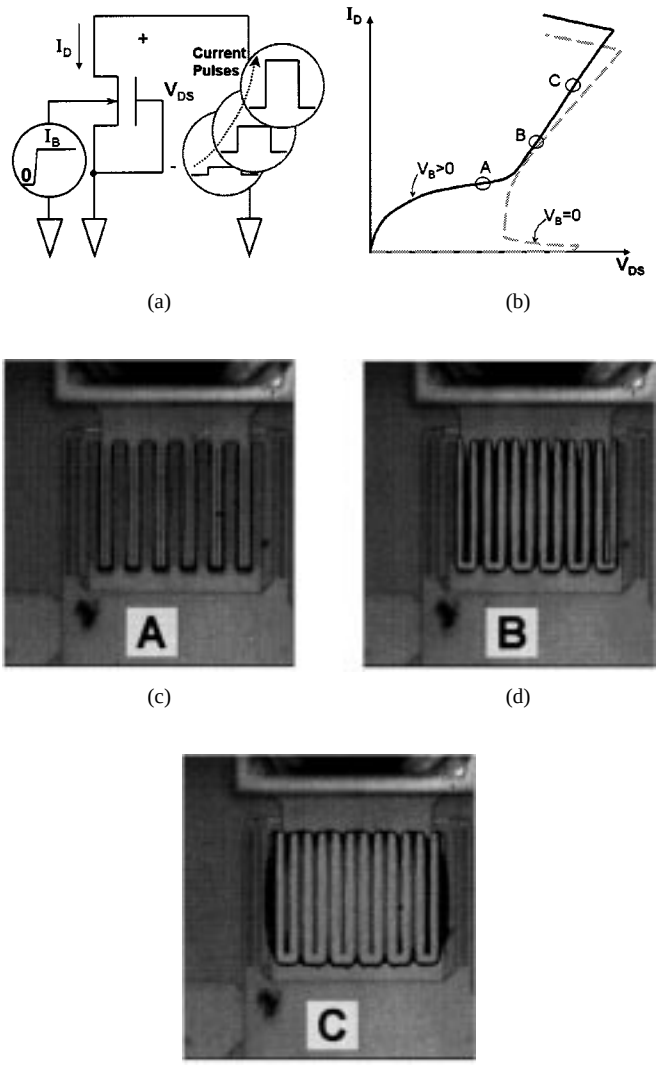

Fig. 21. EMMI photographs on a substrate-triggered nMOS ($W/L = 300\ \mu\text{m}/0.5\ \mu\text{m}$) to observe its turn-on behavior under the stress of different pulsed currents. (a) Measurement setup. (b) Corresponding I–V curve of a substrate-triggered nMOS. (c)–(e) Hot spots in the substrate-triggered nMOS under different current stresses.

damage the MOSFET, from the example of the energy-band diagrams. This effect causes the degradation of ESD robustness in gate-driven devices. Compared to the gate-driven design, the substrate-triggered design can avoid the forming of channel current and enhance the space-charge region to sustain higher ESD current far away from the channel surface. From the energy-band analysis, the substrate-triggered design can continually increase the turn-on area for heat dissipation. Therefore, the substrate-triggered design can effectively improve ESD robustness of the ESD protection devices. From the experimental results, the gate-driven design has been confirmed to cause a sudden degradation of ESD robustness of the ESD protection devices. But the substrate-triggered design can continually increase ESD robustness of the ESD protection devices. Therefore, the substrate-triggered design can be one of the most effective solutions to improve ESD robustness of CMOS devices in sub-quarter-micron CMOS technologies.

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