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Design and Analysis of On-Chip ESD Protection Circuit with Very Low Input Capacitance for High-Precision Analog Applications

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Abstract. An ESD protection design is proposed to solve the ESD protection challenge to the analog pins for high-frequency or current-mode applications. By including an efficient power-rails clamp circuit into the analog I/O pin, the device dimension (W/L) of ESD clamp device connected to the I/O pad in the analog ESD protection circuit can be reduced to only 50/0.5 (μm/μm) in a 0.35-μm silicided CMOS process, but it can sustain the human-body-model (machine-model) ESD level of up to 6 kV (400 V). With such a smaller device dimension, the input capacitance of this analog ESD protection circuit can be significantly reduced to only $\sim$1.0 pF (including the bond pad capacitance) for high-frequency applications. A design model to find the optimized layout dimensions and spacings on the input ESD clamp devices has been also developed to keep the total input capacitance almost constant (within 1% variation), even if the analog input signal has a dynamic range of 1 V.

Key Words: electrostatic discharge (ESD), ESD protection circuit, input capacitance, analog pin

1. Introduction

Electrostatic discharge (ESD) has been the main reliability concern on semiconductor products, especially in the scaled-down CMOS technologies [1,2]. Due to the low breakdown voltage of the thinner gate oxide in deep-submicron CMOS technologies, an efficient ESD protection circuit should be designed and placed on every input pad to clamp the overstress voltage across the gate oxide of the internal circuits. A conventional ESD protection design with the two-stage structure for digital input pin is shown in Fig. 1, where a gate-grounded short-channel NMOS is used as the secondary protection device to clamp the overstress voltage across the gate oxide of the input circuits. To provide a high ESD level, a robust device (such as SCR [3], field-oxide device [4], or long-channel NMOS) is used as the main discharge element in the primary protection stage to bypass ESD current on the input pad. Between the primary stage and the secondary stage of the input ESD protection circuit, a resistor is added to limit the ESD current flowing through the short-channel NMOS in the secondary stage. The resistance value of this resistor is dependent on the turn-on voltage of the ESD clamp device in the primary stage and the It2 (secondary breakdown current) of the short-channel NMOS in the secondary stage. The primary ESD clamp device must be triggered on to bypass ESD current before the gate-grounded NMOS (ggNMOS) in the secondary stage was damaged by the overstress ESD current. If the primary ESD clamp device has a high turn-on voltage, the resistance should be large enough with an order of kΩ [3]. Such two-stage ESD protection design can provide high ESD level for the digital input pins. But the large series resistance and the large junction capacitance in the ESD clamp devices cause a long RC delay to the input signal, it is not suitable for analog applications.

For current-mode input signal or high-frequency applications, the series resistance between the input pad and internal circuits is forbidden. Therefore, the two-stage ESD protection design in Fig. 1 is no longer suitable for analog input pins. To protect the analog input pin, the typical ESD protection circuit with a single-stage ESD protection design is shown in Fig. 2, where a ggNMOS is used as the ESD clamp device. Due to the lack of a series resistance to limit ESD current toward the ggNMOS, as

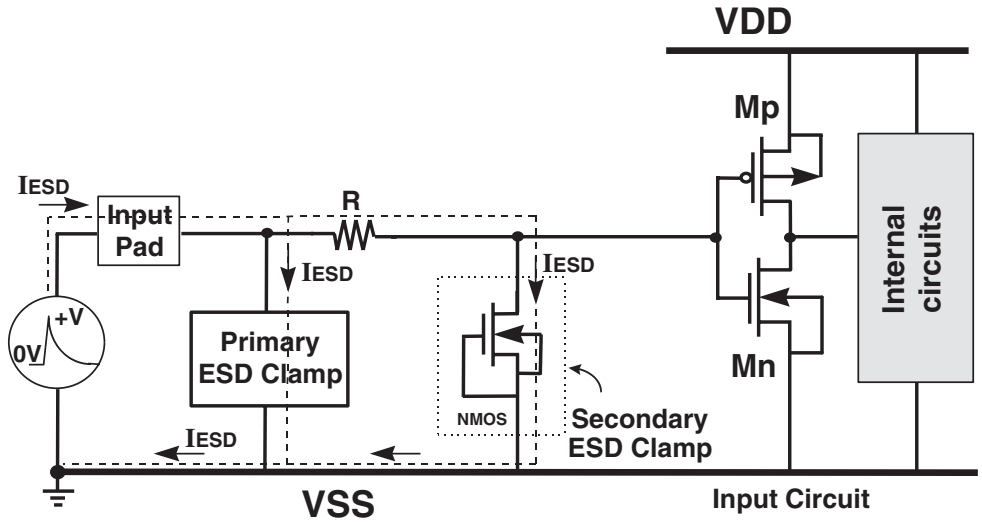


Fig. 1. A schematic diagram of the conventional two-stage ESD protection circuit for digital input pin in CMOS IC's.

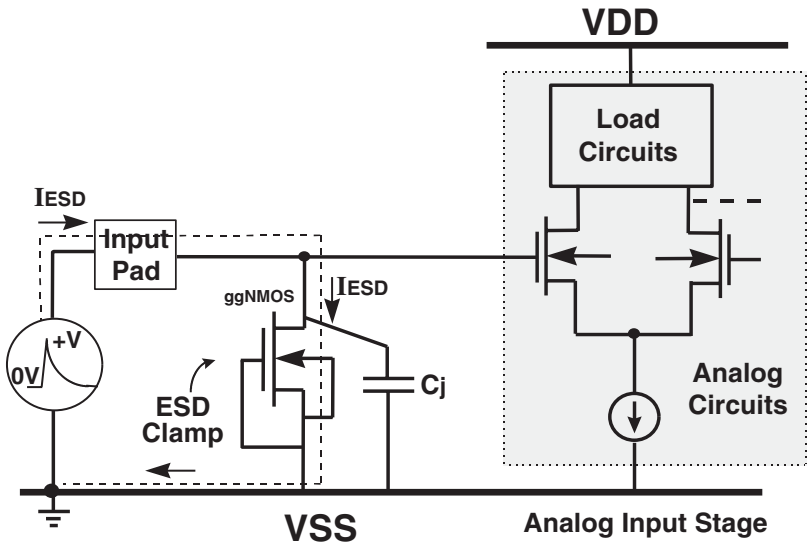


Fig. 2. A schematic diagram of the single-stage ESD protection circuit for analog input pin in CMOS IC's.

well as the ESD robustness of the NMOS device is seriously degraded by the advanced deep-submicron CMOS technologies [5–6], such a ggNMOS is often designed with a larger device dimension and a wider drain-contact-to-poly-gate layout spacing to sustain an acceptable ESD level [6,7]. The additional silicide-blocking mask had been included into the deep-submicron CMOS process to increase ESD robustness of the ESD clamp device. The schematic cross-sectional view of a ggNMOS with the silicide-blocking drain region is illustrated in Fig. 3. But the ggNMOS with a larger device dimension and a wider drain region contributes a larger parasitic drain capacitance to the input pad. Such a parasitic junction capacitance is nonlinear and dependent on the input voltage level.

For some high-resolution circuit operations, the input capacitance of an analog input pin is required to be kept as a constant as possible within the input voltage range. A major distortion source in high-speed analog circuits, especially in the single-ended input

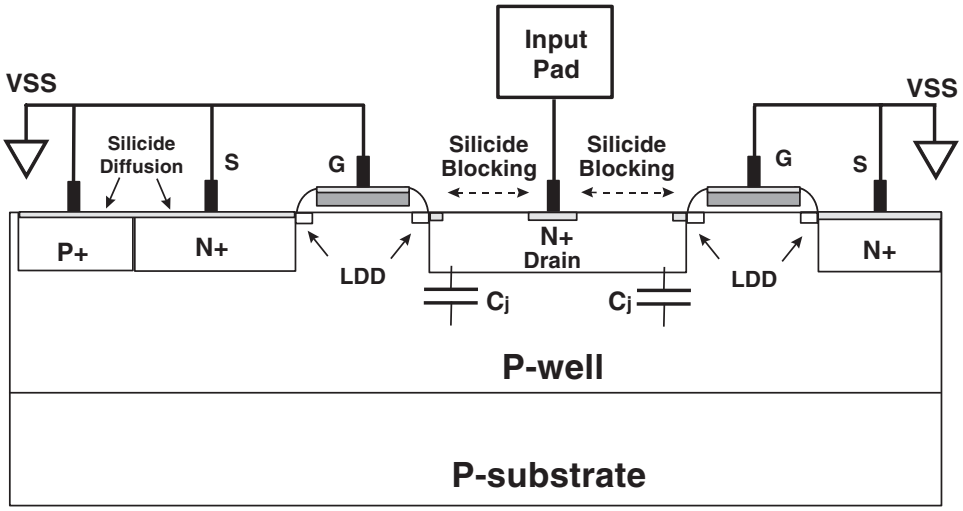


Fig. 3. The schematic cross-sectional view of the ggNMOS with the silicide-blocking drain region.

implementations, is the voltage-dependent nonlinear input capacitance associated with the ESD clamp devices at the analog input pad. The typical degradation on the circuit performance due to the nonlinear input capacitance of the input ESD clamp devices had been reported in [8], where the input capacitance varying from 4 pF to 2 pF due to the input voltage swing from 0 V to 2 V caused an increase on the harmonic distortion in an analog-to-digital converter (ADC) and therefore degraded the precision of the ADC from 14-bit to become only 10-bit. Thus, it has been an emergent challenge to design an effective ESD protection circuit for high-precision analog applications in the scaled-down CMOS technologies.

In this paper, a novel ESD protection design with the advantages of small input capacitance, no series resistance, and high ESD level, has been practically implemented in a 0.35-μm CMOS technology to protect the analog pins for high-precision analog applications [9].

2. ESD Test on Analog Input/Output Pins

To investigate the ESD robustness of input/output pins in IC's, the pin combinations for ESD zapping had been specified in the test standards [10,11]. For an input pin, there are four pin combinations (ESD-stress modes), as shown in Fig. 4, where the ESD voltage is applied to an input (or output) pin with the VDD or VSS pins relatively grounded. Except for such ESD-zapping pin combinations, an additional pin-to-pin ESD stress had been especially specified in the standards for the analog circuits with operational amplifiers or differential input stages to verify the ESD level of the analog pins. The analog pin-to-pin ESD stress for the differential input pins of an operational amplifier is illustrated in Fig. 5, where the positive or negative ESD voltage is applied to the inverting input pin with the corresponding non-inverting input pin relatively grounded. During such an analog pin-to-pin ESD stress, all the other pins including both the VDD and VSS pins are floating.

The ESD current during such an analog pin-to-pin ESD stress is illustrated in Fig. 6 with the differential input stage of an operational amplifier. Because of the lack of series resistor between the analog input pad and the internal circuits, the overstress ESD current easily reaches to the thinner gate oxide of the differential input stage with a common-source circuit structure. If the VSSA power connection between the inverting input pin and the non-inverting input pin has a long metal line in the IC layout, the gate oxide of the differential input stage is easily ruptured by the ESD voltage to cause a discharging current path as the dashed line shown in Fig. 6. The ESD clamp device (such as the large-dimension ggNMOS in Fig. 2) between the inverting input pad and the VSSA power line can not provide effective ESD protection against this additional analog pin-to-pin ESD stress. Therefore, some modified ESD protection designs should be included into the analog ESD protection circuit to overcome this analog pin-to-pin ESD-stress issue.

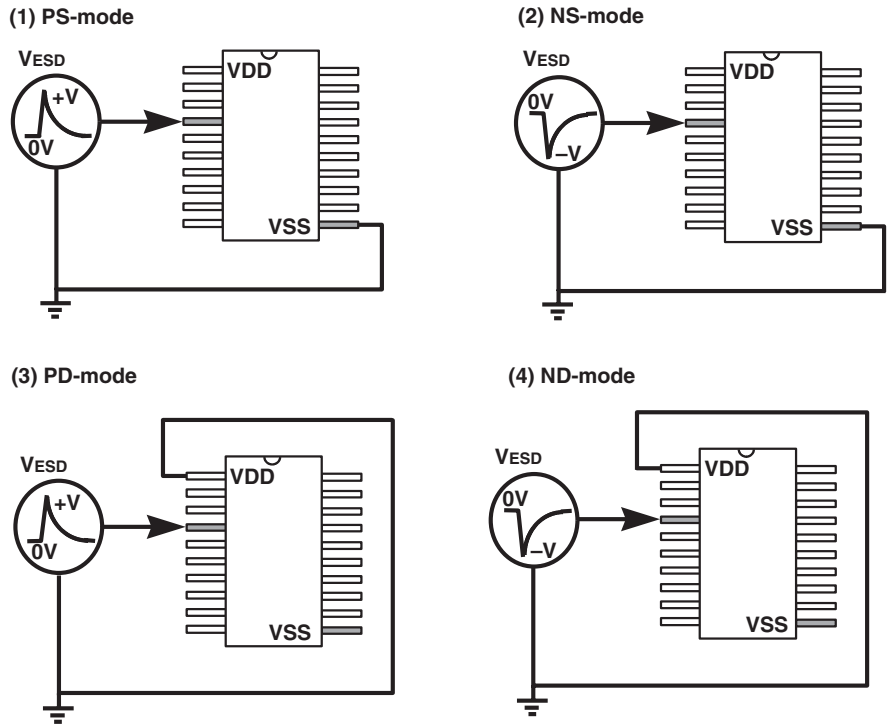


Fig. 4. Pin combinations of ESD testing on the input or output pins of an IC in the Human-Body-Model (HBM) ESD stress.

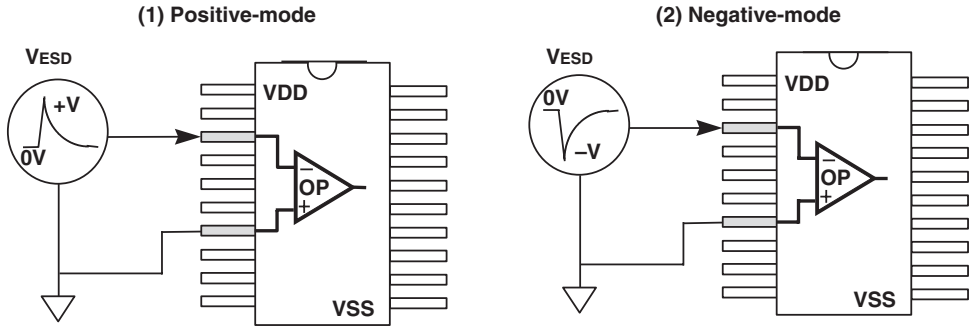


Fig. 5. The pin combination of the additional analog pin-to-pin ESD stress to verify the ESD level of analog circuits with the operational amplifier or differential input stage.

3. ESD Protection Design for Analog Pins

3.1. Circuit Configuration and Operation

The proposed ESD protection circuit for analog pins is shown in Fig. 7, whereas its practical layout in a 0.35-μm silicided CMOS cell library is drawn in Fig. 8. In Fig. 7, the Dp1 (Dn1) is the parasitic junction diode in the drain region of Mp1 (Mn1) device. In order to reduce the input capacitance of the analog pin, the Mn1 and Mp1 are both designed with a much smaller device dimension (W/L) of only 50/0.5 (μm/μm). The HBM ESD level of a stand-alone NMOS with a device dimension of 50/0.5 (μm/μm) is less than 500 V in the 0.35-μm silicided CMOS process, while the NMOS is zapped in the PS-mode ESD stress. But, such

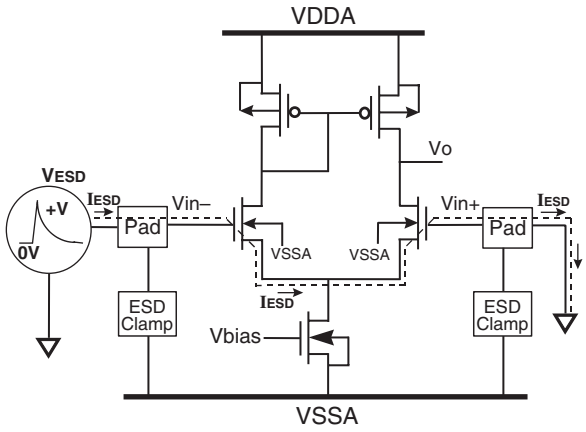


Fig. 6. The ESD current path during the analog pin-to-pin ESD stress.

a small NMOS can sustain an HBM ESD level of 8000 V in the same 0.35-μm silicided CMOS process, while the NMOS is zapped in the NS-mode ESD stress. In the PS-mode (NS-mode) ESD stress, the NMOS is operated in its drain-breakdown condition (drain diode forward-bias condition) to bypass ESD current. The power dissipation located on the ESD clamp device is equal to the product of ESD current and the operating voltage of the device during the ESD events. Therefore, an NMOS has quite different ESD levels between the PS-mode and NS-mode ESD stresses. Similarly, a stand-alone PMOS with a small device dimension also has a high ESD level in the PD-mode ESD stress but has a much low ESD level in the ND-mode ESD stress.

To avoid the small-dimension Mn1 and Mp1 into the drain-breakdown condition in the PS-mode and ND-mode ESD stresses to cause a much low ESD level, an

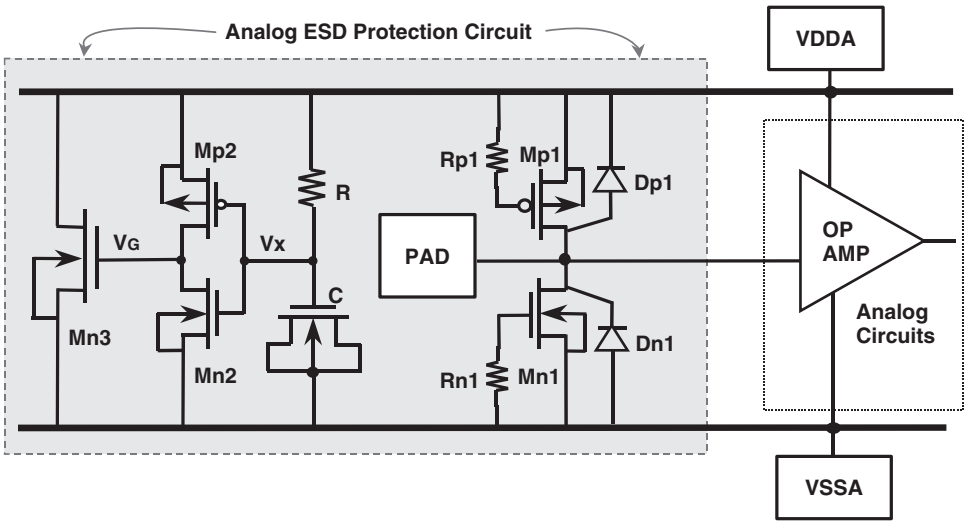


Fig. 7. The proposed ESD protection circuit for analog pins.

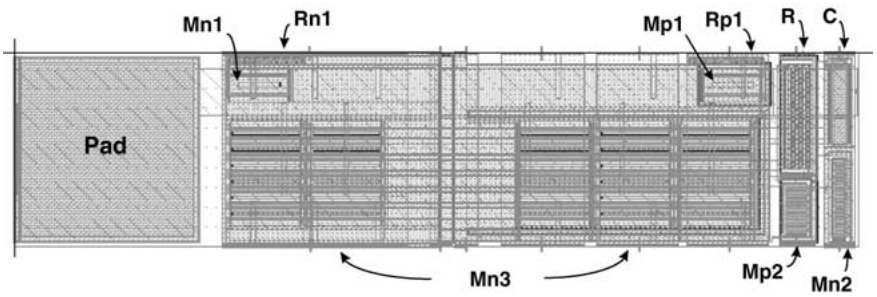


Fig. 8. Layout example of the proposed ESD protection circuit for analog pins in a 0.35-μm silicided CMOS process.

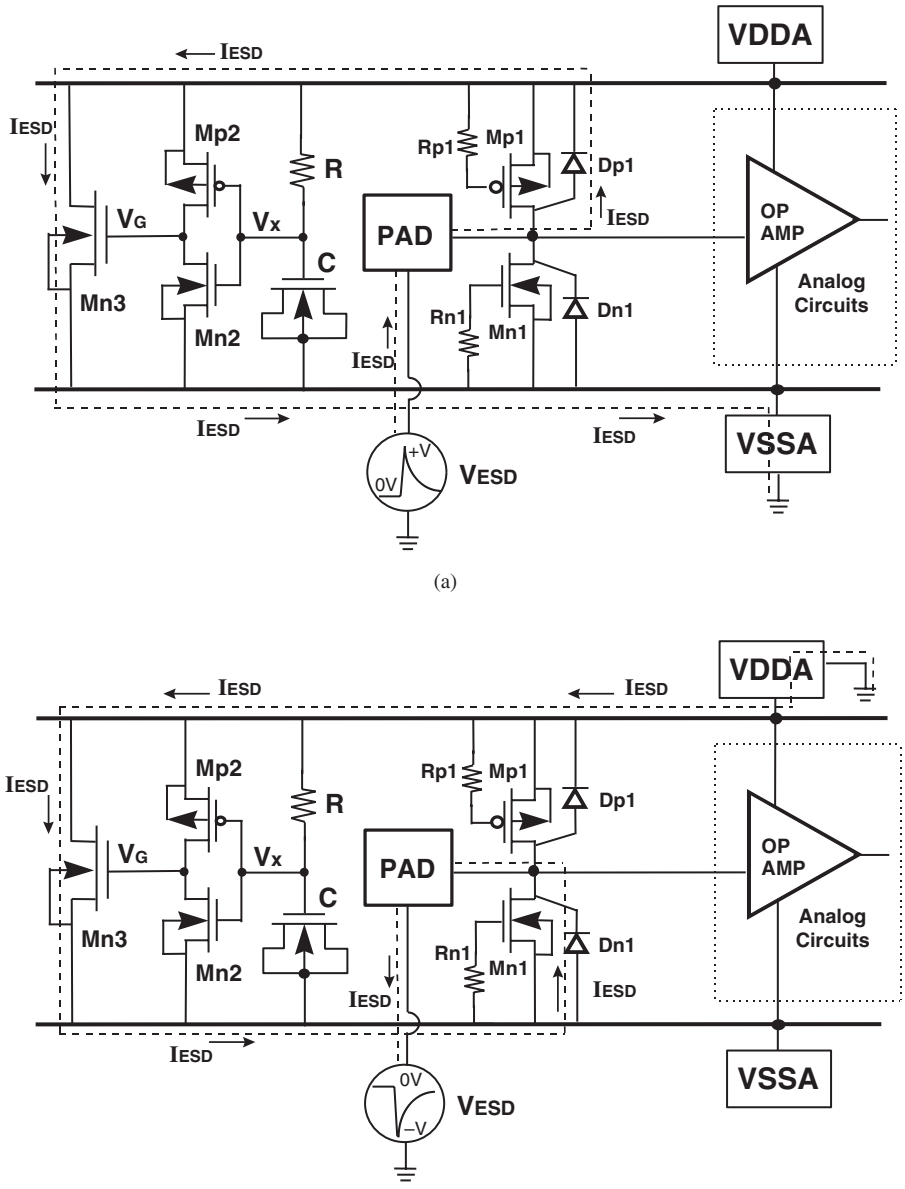


Fig. 9. The ESD current path in the proposed analog ESD protection circuit when the analog pin is zapped in (a) the PS-mode, (b) the ND-mode, ESD stress.

efficient ESD clamp circuit between the power rails is co-constructed into the analog ESD protection circuit to increase the overall ESD level. In Fig. 7, the *RC*-based ESD detection circuit [12–13] is used to trigger on the Mn3 device, when the pad is zapped in the PS-mode or ND-mode ESD stresses. The ESD current paths in this analog ESD protection circuit are illustrated by the dashed lines in Fig. 9(a) and 9(b), respectively, when the analog pin is zapped in the PS-mode and ND-mode ESD stresses. Because the Mn1 in the PS-mode (Mp1 in the ND-mode) ESD stress is not operated in the drain-breakdown condition, the ESD current is bypassed through the forward-biased drain diode Dp1 in Mp1 (Dn1 in Mn1) and the turned-on Mn3. The

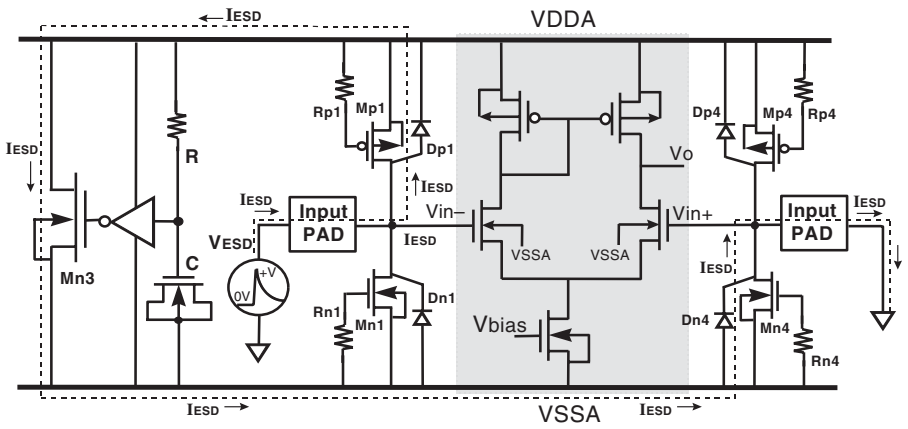


Fig. 10. The ESD current path in the proposed analog ESD protection circuit when the input pins are zapped in analog pin-to-pin ESD stress.

Mn3 is especially designed with a larger device dimension (W/L = 1800 μm/0.5 μm in Fig. 8) to sustain a high ESD level. Although the large-dimension Mn3 has a large junction capacitance, this capacitance does not contribute to the analog pad. Therefore, the analog pin can sustain a much higher ESD level in the four-mode ESD stresses but only with a very small input capacitance.

When the input pins are zapped in the analog pin-to-pin ESD stress (Fig. 6), the ESD current path along this proposed analog ESD protection circuit is illustrated in Fig. 10. During the pin-to-pin ESD stress, both of the VDDA and VSSA power lines in the IC are floating. The ESD current is first conducted from the zapped pad to the VDDA power line through the junction diode Dp1 in the Mp1 of input ESD protection circuit. Therefore, the VDDA line is charged by the ESD energy. The VSSA line initially has a voltage level near to ground because the VSSA line is connected to a grounded pad through the diode Dn4 in Mn4 of another input ESD protection circuit. The pin-to-pin ESD-stress voltage across the two pins of differential input stage therefore becomes across the VDDA and VSSA power lines. The Mn3 connected between the VDDA and VSSA power lines is turned on by the *RC*-based ESD-detection circuit to bypass the ESD current from VDDA to VSSA. Finally, the ESD current flows out the chip from the VSSA power line to the grounded pad through the forward-biased diode Dn4 in Mn4. With suitable design on the ESD-detection circuit to quickly turn on the Mn3 [13], the pin-to-pin ESD stress can be quickly discharged away from the gate oxide of the differential input stage. The pin-to-pin ESD current discharging path shown in Fig. 10 is therefore quite different to that shown in Fig. 6. By using this design, the gate oxide of analog differential input stage can be fully protected without adding any series resistance between the input pad and analog internal circuits. Therefore, the analog input signal can have the widest bandwidth from the pad to the internal circuits, which are protected by the proposed analog ESD protection circuit.

3.2. Input Capacitance

The input capacitance of this proposed analog ESD protection circuit can be calculated as:

$$C_{in} = C_{PAD} + C_n + C_p \tag{1}$$

where the C_{PAD} is the parasitic capacitance of the bond pad. The $C_p(C_n)$ is the drain junction capacitance and the drain-to-gate overlapped capacitance in the Mp1 (Mn1). The drain junction capacitance of a single NMOS or PMOS is strongly bias-dependent. The input capacitance of the previous ESD protection design with a single NMOS in Fig. 2 varies extensively when the input signal has different voltage level. But, the input capacitance of the proposed analog ESD protection circuit (Fig. 7) with a complementary PMOS and NMOS structure can be kept almost constant even if the input signal has a voltage swing from 0 V to VDD (3 V). The total input junction capacitance of the analog ESD protection circuit with different device dimensions are accurately calculated in the frequency domain by using

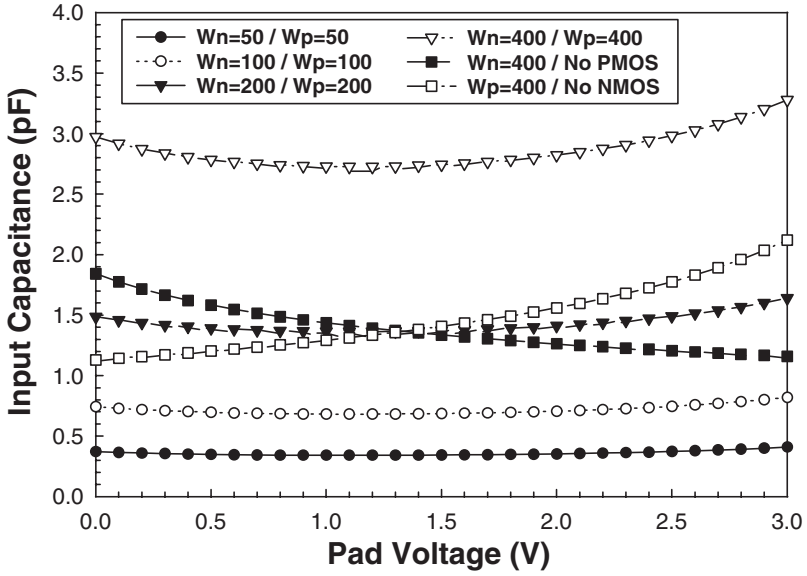


Fig. 11. The input junction capacitance of the analog ESD protection circuit with different device dimensions in Mn1 and Mp1 during different input voltage levels on the pad.

the pin-capacitance-measurement simulation [14] in the Star-Hspice CAD tool.

The simulated results are shown in Fig. 11, where the channel widths of Mn1 and Mp1 vary from 50 μm to 400 μm with a fixed channel length of 0.5 μm under different voltage levels on the input pad. The drain-contact-to-poly-gate spacing in both Mn1 and Mp1 is drawn as 3.4 μm, whereas the source side spacing is drawn as 1.55 μm. With both device dimensions of 50/0.5 in Mn1 and Mp1, the input capacitance of the proposed analog ESD protection circuit is only varying from 0.37 pF to 0.4 pF when the input voltage swing is from 0 V to 3 V. But, the input capacitance of the traditional ESD protection circuit in Fig. 2 with a ggNMOS of W/L = 400/0.5 (μm/μm) varies from 1.83 pF to 1.12 pF, when the input voltage swing is from 0 V to 3 V for an IC with 3-V VDD power supply.

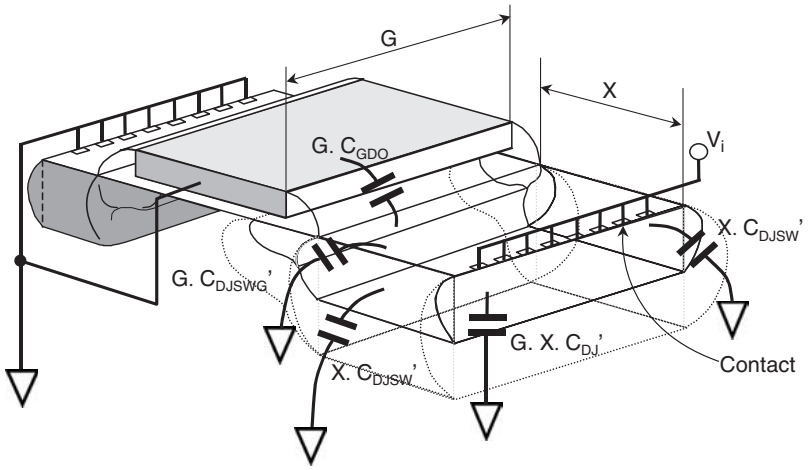
The layout size of the metal bond pad for wire bonding in the 0.35-μm CMOS process is specified as 96×96 μm^2, which contributes a parasitic C_{PAD} of 0.67 pF. So, the total input capacitance of this analog ESD protection circuit including the bond pad is only about 1.04–1.07 pF, even if the input signal has a voltage swing from 0 V to 3 V. With such a small and almost constant input capacitance, this proposed analog ESD protection circuit is more suitable for high-precision and high-frequency applications in both analog input and output pins.

4. Layout Design to Keep a Constant Input Capacitance

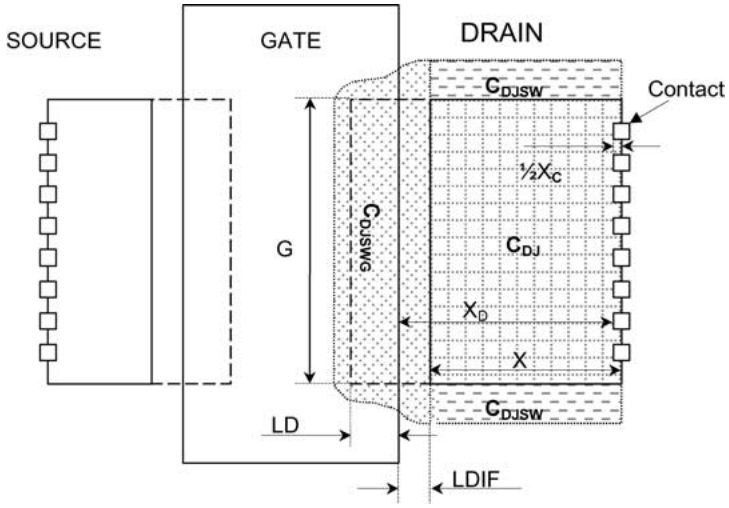
In this Section, the input capacitance of the proposed analog ESD protection circuit is calculated with device parameters and layout dimensions. A design model to optimize the layout dimensions and spacing of ESD clamp devices has been developed to keep the input capacitance almost constant [15]. The variation on the input capacitance of the proposed analog input ESD clamp devices can be designed below 1%.

4.1. Calculation on the Input Capacitance

The main nonlinear source on the input capacitance is the bias-dependent junction capacitance at the drain regions of the Mn1 and Mp1 of the input ESD protection circuit in Fig. 7. When the input signal on the input pad has an increasing voltage waveform, the drain junction capacitance of Mn1 decreases but the drain junction capacitance of Mp1 increases. On the contrary, the drain junction capacitance of Mn1 increases but the drain junction capacitance of Mp1 decreases, when the input signal on the input pad has a decreasing voltage waveform. From the complementary structure of the proposed analog ESD protection circuit, the input capacitance can be kept almost constant if suitable layout



(a)



(b)

Fig. 12. (a) The three-dimension structure of a finger-type MOS device. (b) The corresponding top-view layout of a finger-type MOS device with specified layout spacings.

dimensions and spacings are selected to draw the Mn1 and Mp1 devices.

The device structure of the ESD clamp devices are generally drawn in the finger-type structure to save total layout area of the I/O cells, as that shown in Fig. 8. The three-dimension structure of an finger-type NMOS (or PMOS) device is drawn in Fig. 12(a), whereas the top view of device layout with the specified layout spacings is drawn in Fig. 12(b). The finger length of a single poly finger is defined as G, which is also as the channel width of the finger-type MOS device. The spacing from the center of drain contact to the edge of the lightly-doped drain (LDD) region is marked as X, which will be used in the following equations to calculate the junction capacitance for the drain bottom plane. The clearance between the poly gate and the drain contact is marked as X_D, and the width of drain contact is marked as X_C. Therefore, the spacing X defined in Fig. 12 can be written as

$$X = X_D + \frac{1}{2}X_C - LDIF \tag{2}$$

where the *LDIF* is the length of lightly-doped drain diffusion adjacent to the gate. This *LDIF* is an extracted

device parameter which is given in *HSPICE* parameters of a CMOS process.

The drain region of MOS device with a single poly finger has three different junction capacitance (C_{DJ}, C_{DJSW}, and C_{DJSWG}) and one drain-to-gate overlapped capacitance (C_{GD}), which are also shown in Fig. 12. The equation of each capacitance is summarized in the following [16]:

$$C_{GD} = CGDO \cdot G \tag{3}$$

$$C_{DJ} = G \cdot X \cdot C'_{DJ} \tag{4}$$

$$C_{DJSW} = X \cdot C'_{DJSW} \tag{5}$$

$$C_{DJSWG} = G \cdot C'_{DJSWG} \tag{6}$$

where

$$C'_{DJ} = CJ\left(1+\frac{V_R}{PB}\right)^{-MJ} \text{F/m}^2 \tag{7}$$

$$C'_{DJSW} = CJSW\left(1+\frac{V_{SW}}{PBSW}\right)^{-MJSW} \text{F/m} \tag{8}$$

$$C'_{DJSWG} = CJSWG\left(1+\frac{V_{SWG}}{PBSWG}\right)^{-MJSWG} \text{F/m} \tag{9}$$

The C'_{DJ} is the junction capacitance per unit area of the drain bottom plane. The C'_{DJSW} and C'_{DJSWG} are the junction capacitance per unit length of the drain region at the sidewall by field-oxide side and the sidewall by the poly-gate side, respectively. The devices parameters used to calculate the capacitance of NMOS and PMOS devices in a 0.35-μm silicided CMOS process are listed in Table 1 [17].

Table 1. Device parameters on the drain capacitance of NMOS and PMOS devices in a 0.35-μm silicided CMOS process.

	NMOS	PMOS
CGDO	2.79e-10 F/m	2.31e-10 F/m
CJ	1.01893e-3 F/m^2	1.46829e-3 F/m^2
CJSW	3.057956e-10 F/m	4.173308e-10 F/m
CJSWG	1.524314e-10 F/m	1.013197e-10 F/m
MJ	0.3075043	0.5464087
MJSW	0.1929617	0.3948903
MJSWG	0.1929617	0.3948903
PB	0.6944474 V	0.9191281 V
PBSW	0.6944494 V	0.9191281 V
PBSWG	0.6944494 V	0.9191281 V
LDIF	1.2e-7 m	1.2e-7 m

Substituting the above equations into equation (1) with the device parameters for Mn1 and Mp1, the total input capacitance C_{in} of the proposed analog ESD protection circuit can be expressed as

$$\begin{aligned} C_{in} = C_{PAD} + k_n \cdot \Bigg\{ & G_n \cdot CGDO_n + G_n \cdot X_n \cdot CJ_n \\ & \times \left(1+\frac{V_i}{PB_n}\right)^{-MJ_n} + G_n \cdot CJSWG_n \\ & \times \left(1+\frac{V_i}{PBSWG_n}\right)^{-MJSWG_n} + 2 \cdot X_n \cdot CJSW_n \\ & \times \left(1+\frac{V_i}{PBSW_n}\right)^{-MJSW_n} \Bigg\} \\ & + k_p \cdot \Bigg\{ G_p \cdot CGDO_p + G_p \cdot X_p \cdot CJ_p \\ & \times \left(1+\frac{V_{DD}-V_i}{PB_p}\right)^{-MJ_p} + G_p \cdot CJSWG_p \\ & \times \left(1+\frac{V_{DD}-V_i}{PBSWG_p}\right)^{-MJSWG_p} + 2 \cdot X_p \cdot CJSW_p \\ & \times \left(1+\frac{V_{DD}-V_i}{PBSW_p}\right)^{-MJSW_p} \Bigg\} \end{aligned} \tag{10}$$

where

$k_n(k_p)$ is the finger number of the poly gate in the finger-type Mn1 (Mp1) layout;
$G_n(G_p)$ is the finger length of the poly gate in the finger-type Mn1 (Mp1) layout;
$X_n(X_p)$ is the layout spacing between the drain contact and the poly gate, defined in equation (2), in the finger-type Mn1 (Mp1) layout; and
V_i is the input voltage level on the pad.

When the layout spacings in Mn1 and Mp1 are modified, the total input capacitance of the proposed analog ESD protection circuit can be adjusted. Based on equation (10), the desired layout parameters to minimize the variation on the input capacitance within some input voltage range can be obtained.

4.2. *Layout Design to Minimize Variation on Input Capacitance*

If the partial differential equation of $\partial C_{in}/\partial V_i$ is equal to zero, the input capacitance becomes independent to the input voltage level, and then the input capacitance can be kept as constant. Unfortunately, the layout parameters (K_n, K_p, G_n, G_p, X_n, and X_p) on the Mn1 and Mp1 devices with *HSPICE* parameters in the 0.35-μm silicided CMOS process can not keep this $\partial C_{in}/\partial V_i$ term always zero, while the input signal has a voltage swing from 0 V to VDD (3 V).

In the analog applications, the analog input signal generally has a common reference voltage, indicated as V_{com} in this work. For the symmetrical analog input signals with a maximum amplitude of ΔV, the minimum ($V_{\min}$) and maximum ($V_{\max}$) voltage level of the analog input signals can be written as

$$V_{\min} = V_{com} - \Delta V \tag{11}$$

and

$$V_{\max} = V_{com} + \Delta V \tag{12}$$

According to the mean value theorem [18], if the input capacitance at the voltage levels of $V_{\min}$ and $V_{\max}$ are kept the same, the condition of $\partial C_{in}/\partial V_i = 0$ is located within this analog voltage range. Therefore, the input capacitance has a minimized variation within the analog input voltage range between $V_{\min}$ and $V_{\max}$. Substituting the $V_{\min}$ and $V_{\max}$ into equation (10), the condition of $C_{in}(V_{\max}) = C_{in}(V_{\min})$ to minimize the variation on the total input capacitance can be obtained as

$$\begin{aligned} &k_n \cdot \{\alpha \cdot G_n \cdot X_n + \beta \cdot G_n + 2 \cdot \gamma \cdot X_n\} \\ &\quad = k_p \cdot \{\eta \cdot G_p \cdot X_p + \theta \cdot G_p + 2 \cdot \kappa \cdot X_p\} \end{aligned} \tag{13}$$

where

$$\alpha = CJ_n \left[\left(1 + \frac{V_{\min}}{PB_n}\right)^{-MJ_n} - \left(1 + \frac{V_{\max}}{PB_n}\right)^{-MJ_n} \right] \tag{14}$$

$$\beta = CJSWG_n \left[\left(1 + \frac{V_{\min}}{PBSWG_n}\right)^{-MJSWG_n} - \left(1 + \frac{V_{\max}}{PBSWG_n}\right)^{-MJSWG_n} \right] \tag{15}$$

$$\gamma = CJSW_n \left[\left(1 + \frac{V_{\min}}{PBSW_n}\right)^{-MJSW_n} - \left(1 + \frac{V_{\max}}{PBSW_n}\right)^{-MJSW_n} \right] \tag{16}$$

$$\eta = CJ_p \left[\left(1 + \frac{V_{DD} - V_{\max}}{PB_p}\right)^{-MJ_p} - \left(1 + \frac{V_{DD} - V_{\min}}{PB_p}\right)^{-MJ_p} \right] \tag{17}$$

$$\theta = CJSWG_p \left[\left(1 + \frac{V_{DD} - V_{\max}}{PBSWG_p}\right)^{-MJSWG_p} - \left(1 + \frac{V_{DD} - V_{\min}}{PBSWG_p}\right)^{-MJSWG_p} \right] \tag{18}$$

$$\kappa = CJSW_p \left[\left(1 + \frac{V_{DD} - V_{\max}}{PBSW_p}\right)^{-MJSW_p} - \left(1 + \frac{V_{DD} - V_{\min}}{PBSW_p}\right)^{-MJSW_p} \right] \tag{19}$$

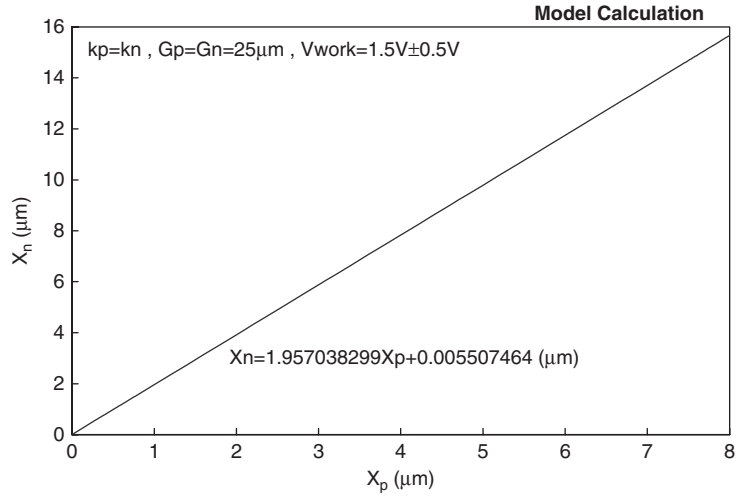
By applying the device parameters of the 0.35-μm silicided CMOS process into equations (13)–(19), the condition to keep the input capacitance with a minimum variation at the voltage levels of $V_{DD} = 3$ V, $V_{com} = 1.5$ V, and $\Delta V = 0.5$ V can be found as

$$\begin{aligned} &k_n \cdot \{1.029515 \times 10^{-4} \cdot G_n \cdot X_n + 1.098674 \\ &\quad \times 10^{-11} \cdot G_n + 2.204072 \times 10^{-11} \cdot X_n\} \\ &= k_p \cdot \{2.011205 \times 10^{-4} \cdot G_p \cdot X_p + 1.156346 \\ &\quad \times 10^{-11} \cdot G_p + 4.762930 \times 10^{-11} \cdot X_p\} \end{aligned} \tag{20}$$

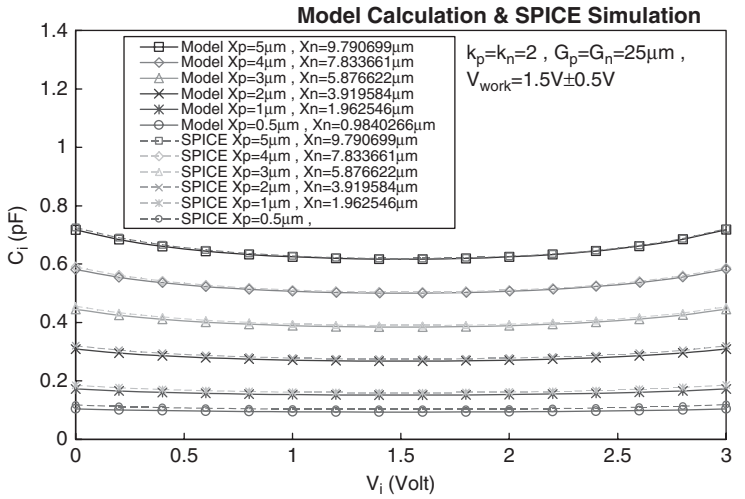
Therefore, if the layout parameters (K_n, K_p, G_n, G_p, X_n, and X_p) on the finger-type Mn1 and Mp1 devices are correctly chosen to meet this condition of equation (20), the input capacitance of the proposed analog ESD protection circuit can have a minimum variation within the desired analog voltage range. This implies that the variation on the input capacitance of the proposed analog ESD protection circuit can be minimized by only choosing the suitable device dimensions and layout spacings in the finger-type Mn1 and Mp1 devices. This is quite useful to design the proposed analog ESD protection circuit with an almost-constant input capacitance for specified analog applications in a given CMOS process.

4.3. *Design Examples*

If $k_p = k_n = 2$ and $G_p = G_n = 25$ μm are chosen with the voltage levels of $V_{DD} = 3$ V, $V_{com} = 1.5$ V, and $\Delta V = 0.5$ V, the relation between the layout spacings



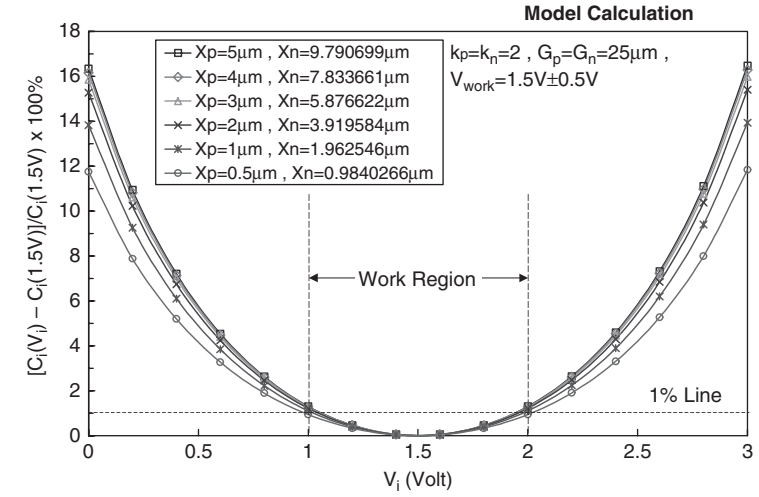
(a)



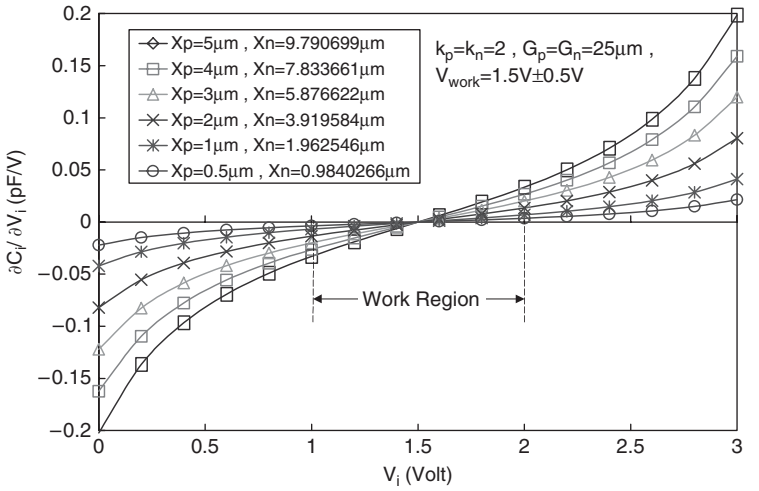
(b)

Fig. 13. (a) The relation between the layout parameters X_n and X_p to meet the condition in equation (20) with the analog common reference voltage biased at 1.5 V. (b) The relation between the total input capacitance and the input voltage level under different layout parameters X_n and X_p. (c) The relation between the variation percentage on the input capacitance and the input voltage level under different layout parameters X_n and X_p. (d) The relation between the calculated $\partial C_{in}/\partial V_i$ value and the input voltage level under different layout parameters X_n and X_p.

of X_n and X_p to meet the condition of equation (20) is calculated in Fig. 13(a), where the X_n is found to be linearly dependent on the X_p. Based on this condition with the specified layout parameters, the relation between the total input capacitance and the input voltage level is calculated from equation (10) and shown in Fig. 13(b). The simulation results from *HSPICE* on the total input capacitance of the proposed analog ESD protection circuit are also included in Fig. 13(b) to verify the accuracy of the derived model equations. The model calculated results well agree to the *HSPICE* simulated results in Fig. 13(b) under many sets of different layout parameters, where each set of different layout parameters meets the condition of equation (20). This has verified the accuracy of the derived model equations in this work. As shown in Fig. 13(b), if the layout parameters X_n and X_p are chosen with smaller values, the proposed analog ESD protection circuit also has



(c)



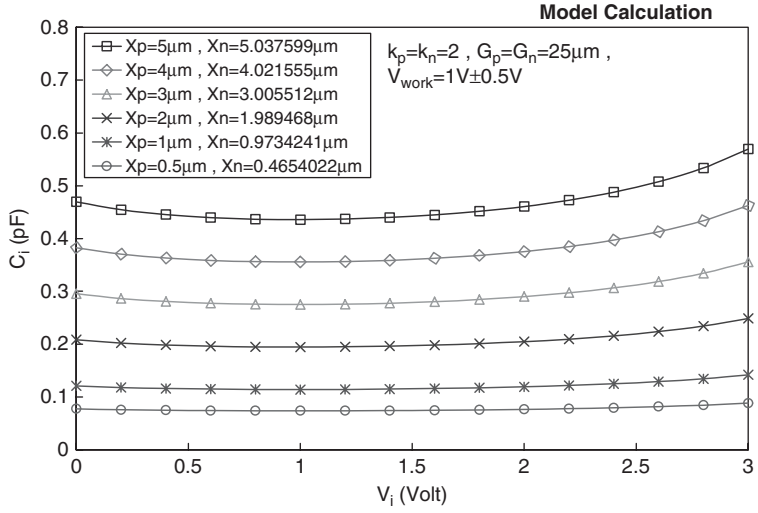
(d)

Fig. 13. (*Continued*)

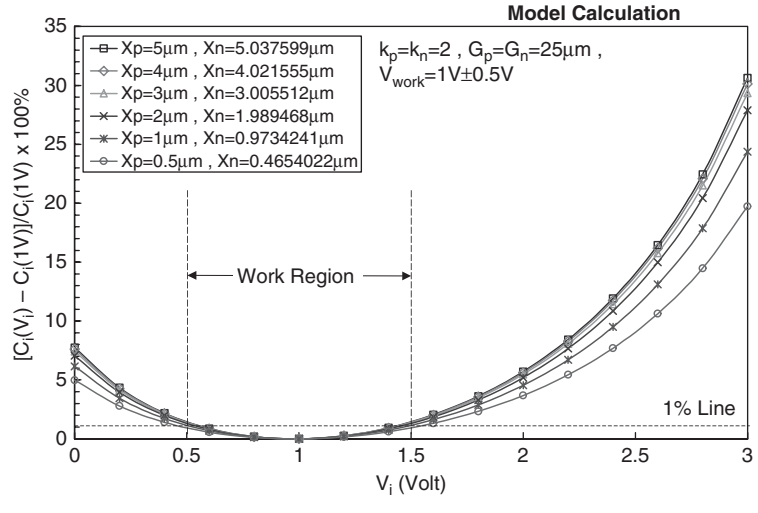
a smaller input capacitance. Besides, the analog ESD protection circuit has the smallest input capacitance, when the input voltage level is biased at the analog common reference voltage V_{com}. The percentage of variation on the input capacitance in Fig. 13(b) with respect to the smallest input capacitance at $V_{com} = 1.5$ V under many sets of different layout parameters are calculated and drawn as a function of input voltage in Fig. 13(c). If the layout parameters X_n and X_p are chosen with smaller values, the analog ESD protection circuit also has a smaller variation percentage on the input capacitance. Based on such layout parameters found by equation (20), the relation between the partial differential value of $\partial C_{in}/\partial V_i$ and the input voltage is shown in Fig. 13(d). The $\partial C_{in}/\partial V_i$ has a value of zero when the input voltage level just biased at the V_{com} of 1.5 V. Within the desired analog voltage range of 1–2 V, the variation percentage of the input capacitance is found within 1% in the work region shown in Fig. 13(c). With such a small 1% variation on the

input capacitance, this proposed analog ESD protection circuit is very suitable for high-precision analog applications.

In Fig. 13(a)–13(d), the input capacitance is calculated with the analog common reference voltage (V_{com}) chosen at 1.5 V, which is equal to the half of 3-V VDD. If the analog input signals have different common reference voltages, the input capacitance with minimum variation within the desired input voltage range can be found by the above equations. For example, if the voltage levels of $V_{DD} = 3$ V, $V_{com} = 1.0$ V, and $\Delta V = 0.5$ V are chosen with $k_p = k_n = 2$ and $G_p = G_n = 25$ μm, the relation between X_n and X_p to sustain the condition of equation (13) becomes $X_n = 1.01604 \cdot X_p - 0.04261968$. Based on this condition, the relation between the input capacitance and the input voltage level is calculated and shown in Fig. 14(a), and the variation percentage on the input capacitance is shown in Fig. 14(b) under different layout parameters. Because the analog common reference voltage (V_{com}) is chosen



(a)



(b)

Fig. 14. The relations between (a) the total input capacitance, and (b) the variation percentage on the input capacitance, of the proposed analog ESD protection circuit and the input voltage level under different layout parameters X_n and X_p, which meet the condition in equation (13) with an analog common reference voltage biased at 1.0 V.

at 1.0 V in Fig. 14, the input capacitance has the smallest capacitance when the input voltage level is biased at 1 V. Within the desired analog voltage range (work region) of 0.5–1.5 V, the variation percentage of the input capacitance is also within 1% in this work region.

On the contrary, if the analog common reference voltage (V_{com}) is chosen at 2.0 V for analog applications with a higher input voltage level, the relation between X_n and X_p to sustain the condition of equation (13) becomes $X_n = 3.75596 \cdot X_p + 0.09672$ with the design condition of $V_{DD} = 3$ V, $\Delta V = 0.5$ V, $k_p = k_n = 2$, and $G_p = G_n = 25$ μm. Based on this condition, the relation between the input capacitance and the input voltage level is calculated and shown in Fig. 15(a), and the

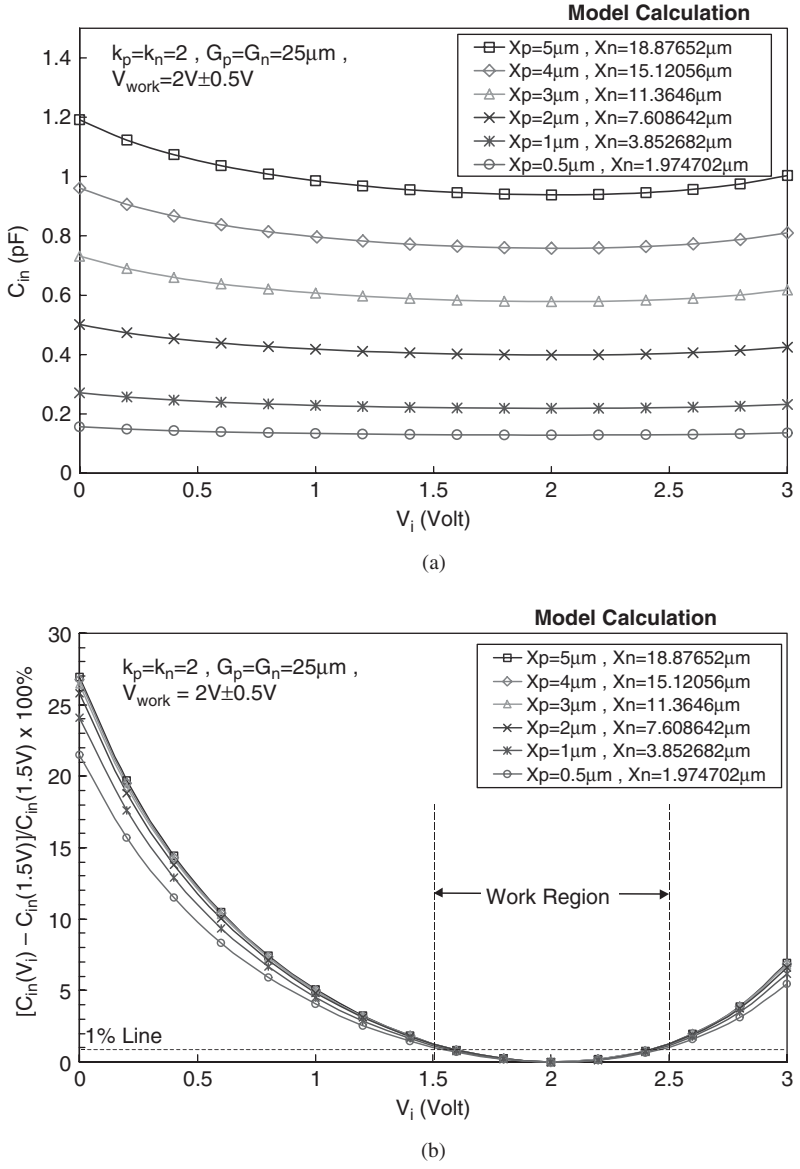


Fig. 15. The relations between (a) the total input capacitance, and (b) the variation percentage on the input capacitance, of the proposed analog ESD protection circuit and the input voltage level under different layout parameters X_n and X_p, which meet the condition in equation (13) with an analog common reference voltage biased at 2.0 V.

variation percentage on the input capacitance is shown in Fig. 15(b) under different layout parameters. Because the analog common reference voltage (V_{com}) is chosen at 2.0 V in Fig. 15, the input capacitance has the smallest capacitance when the input voltage level is biased at 2 V. Within the desired analog voltage range (work region) of 1.5–2.5 V, the variation percentage of the input capacitance is also within 1% in this work region. This has shown the flexibility of the derived model to find the suitable layout parameters to minimize the voltage-dependent variation on the input capacitance of the proposed analog ESD protection circuit.

5. Experimental Results

The proposed analog ESD protection circuit has been practically fabricated in a 0.35-μm silicided CMOS process with an operational amplifier as its input circuit. In the test chip, both the inverting and non-inverting input pins are protected by the proposed analog ESD protection circuit. The silicide-blocking mask is also used on the device Mn1, Mp1, and Mn3 to improve their ESD robustness, but without using the extra ESD-implantation process modification.

5.1. ESD Test Results

The fabricated analog ESD protection circuits are zapped by the *ZapMaster* ESD tester produced by *Keytek* Instrument corp. in both the HBM (human-body model) and MM (machine model) ESD stresses. The ESD test results of the maximum sustain voltage are summarized in Table 2, which includes the analog pin-to-pin ESD stress. The failure criterion is defined as the leakage current at the pad exceeds 1 μA under 5-V voltage bias after any ESD zapping. As shown in Table 2, the proposed analog ESD protection circuit can successfully provide the analog pins with an HBM (MM) ESD level of above 6000 V (400 V) in all ESD-stress conditions but without adding any series resistor between the pad and the internal circuits. This verifies the effectiveness of the proposed analog ESD protection circuit, especially in the analog pin-to-pin ESD stress.

Table 2. ESD level of the proposed analog ESD protection circuit in the human-body-model (HBM) and machine-model (MM) ESD test.

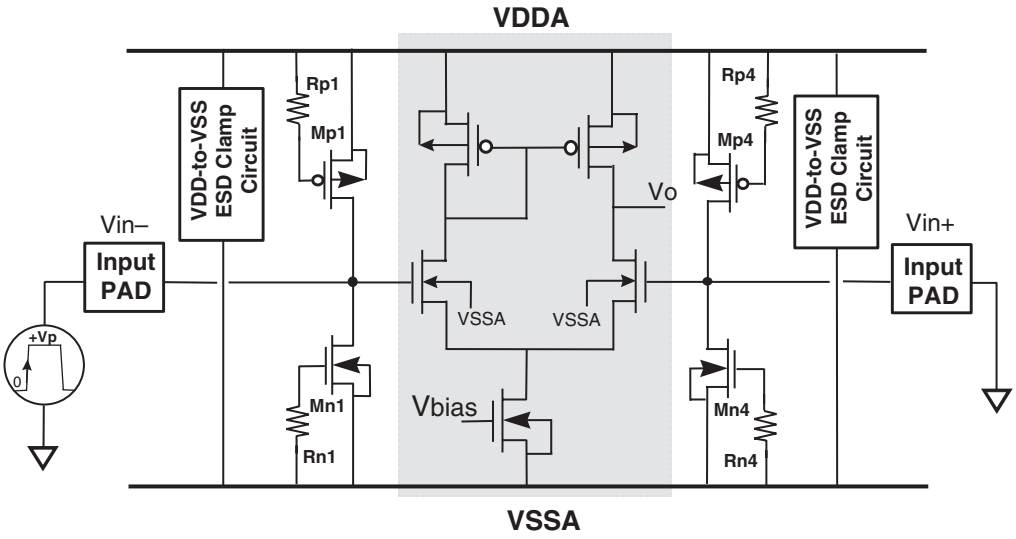
	Pin Combination in ESD Test				
	PS-Mode	NS-Mode	PD-Mode	ND-Mode	Pin-to-Pin
HBM (V)	6000	−8000	7000	−7000	6000
MM (V)	400	−400	400	−400	400

The conventional ESD protection design in Fig. 2 with a ggNMOS of W/L = 480/0.5 (μm/μm) for analog input pin is also fabricated in the same testchip as a reference. The HBM PS-mode ESD level of the design in Fig. 2 is ∼3 kV, but its analog pin-to-pin HBM ESD level is below 500 V. The pin-to-pin ESD damage location is founded on the poly gate of the first input stage in the operational amplifier circuit. So, the conventional ESD protection design cannot protect the thinner gate oxide of the differential input stage in deep-submicron CMOS technologies during the pin-to-pin ESD stress.

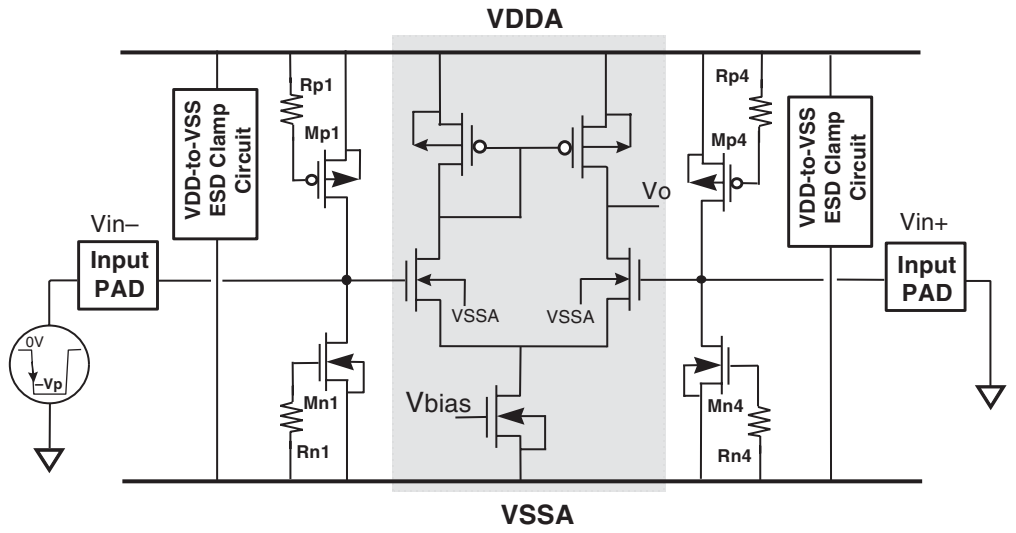
5.2. Turn-on Verification

To verify the turn-on efficiency of the proposed analog ESD protection circuit during the pin-to-pin ESD stress, a square-type voltage pulse generated from a pulse generator (hp 8118A) is applied to the inverting pin of an operational amplifier, whereas the non-inverting pin of the operational amplifier is relatively grounded and both the VDDA and VSSA pins are floating. The experimental setup to verify the turn-on efficiency in the positive and negative pin-to-pin ESD-stress conditions are shown in Fig. 16(a) and 16(b), respectively.

The measured voltage waveforms in the positive pin-to-pin ESD-stress condition are shown in Fig. 17(a) and 17(b). The voltage waveform in Fig. 17(a) is the original voltage pulse generated from the hp 8118A pulse generator with a pulse height of 8 V and a pulse width of 200 ns. The 8-V voltage pulse has a rise time around ∼10 ns, which is similar to the rise time (5–15 ns) of an HBM ESD pulse. The drain breakdown voltage of the NMOS Mn1 in the 0.35-μm silicide CMOS process without extra ESD-implantation process modification is about 8.5 V. Therefore, the voltage pulse with a pulse height of 8 V does not cause the drain breakdown in Mn1 in the analog ESD protection circuit. By applying such a voltage pulse to the analog pin, the turn-on efficiency of the proposed analog ESD protection circuit can be practically verified. While



(a)



(b)

Fig. 16. The experimental setup to verify the turn-on efficiency of the proposed analog ESD protection circuit during (a) the positive, and (b) the negative, pin-to-pin ESD-stress conditions.

this positive voltage pulse is applied to the analog pin as shown in Fig. 16(a), it is clamped by the proposed analog ESD protection circuit and the degraded voltage waveform is shown in Fig. 17(b). The voltage waveforms in the negative pin-to-pin ESD-stress condition are also measured and shown in Fig. 18(a) and 18(b). The voltage waveform in Fig. 18(a) is the original negative voltage pulse generated from the pulse generator with a pulse height of -8 V and a pulse width of 200 ns. While this negative voltage pulse is applied to the analog pin as shown in Fig. 16(b), it is clamped by the analog ESD protection circuit to a voltage level of only -5 V, where the degraded voltage waveform is shown in Fig. 18(b). From Fig. 17(b) and Fig. 18(b),

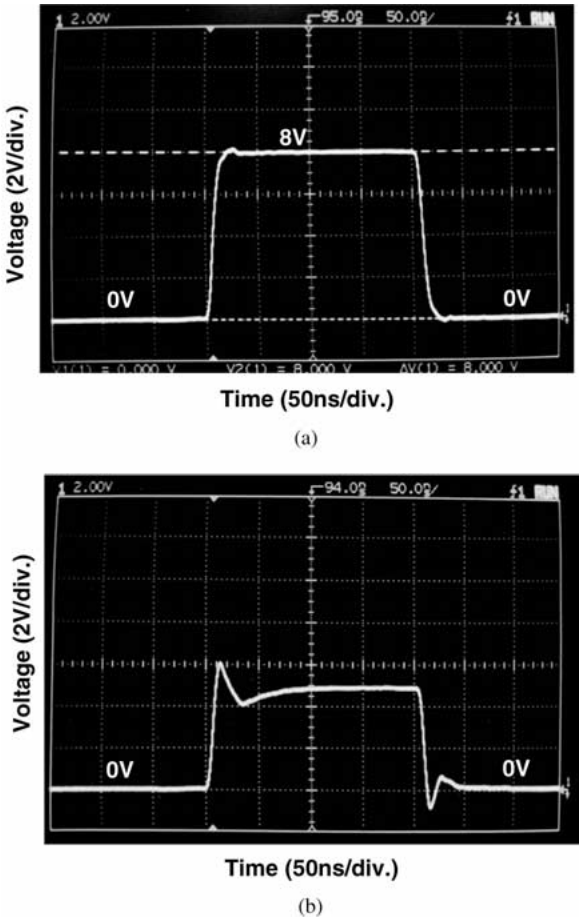


Fig. 17. (a) The measured voltage waveform of the original 8-V voltage pulse generated from a pulse generator, (b) the degraded voltage waveform when the 8-V voltage pulse is applied to the analog inverting input pin in the pin-to-pin stress condition as shown in Fig. 16(a).

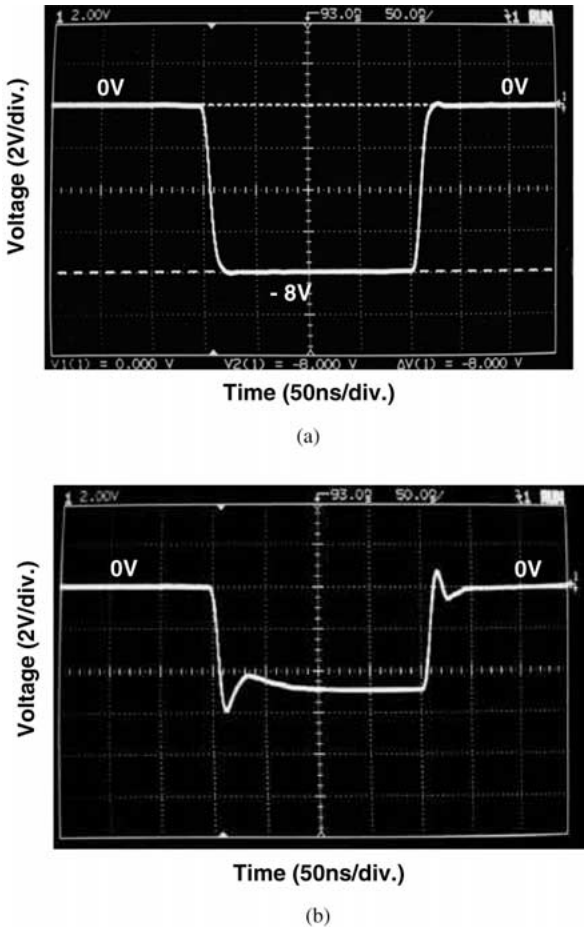


Fig. 18. (a) The measured voltage waveform of the original negative (−8 V) voltage pulse generated from a pulse generator, (b) the degraded voltage waveform when the voltage pulse is applied to the analog inverting input pin in the pin-to-pin stress condition as shown in Fig. 16(b).

the voltage pulses are actually clamped by the proposed analog ESD protection circuit during the pin-to-pin ESD-stress conditions. Therefore, the thinner gate oxide of the differential input stage can be safely protected during the pin-to-pin ESD stress.

The turn-on efficiency of the proposed analog ESD protection circuit during the PS-mode and ND-mode ESD stresses are also verified. The experiment setup are shown in Fig. 19(a) and 19(b) for the PS-mode and ND-mode ESD stresses, respectively. While the positive voltage pulse with a voltage level of 8 V, as that shown in Fig. 17(a), is applied to the analog input pin in the PS-mode ESD-stress condition, the positive voltage pulse is clamped by the analog ESD protection circuit and the degraded voltage waveform on the pad is measured in Fig. 20(a). While the negative voltage pulse, as that shown in Fig. 18(a), is applied to the analog input pin in the ND-mode ESD-stress condition, the negative (−8 V) voltage pulse is clamped by the analog ESD protection circuit and the degraded voltage waveform on the pad is measured in Fig. 20(b). This has practically verified the turn-on efficiency of the proposed analog ESD protection circuit.

From above experimental verification, the positive or negative voltage pulses are really clamped by the proposed analog ESD protection circuit through

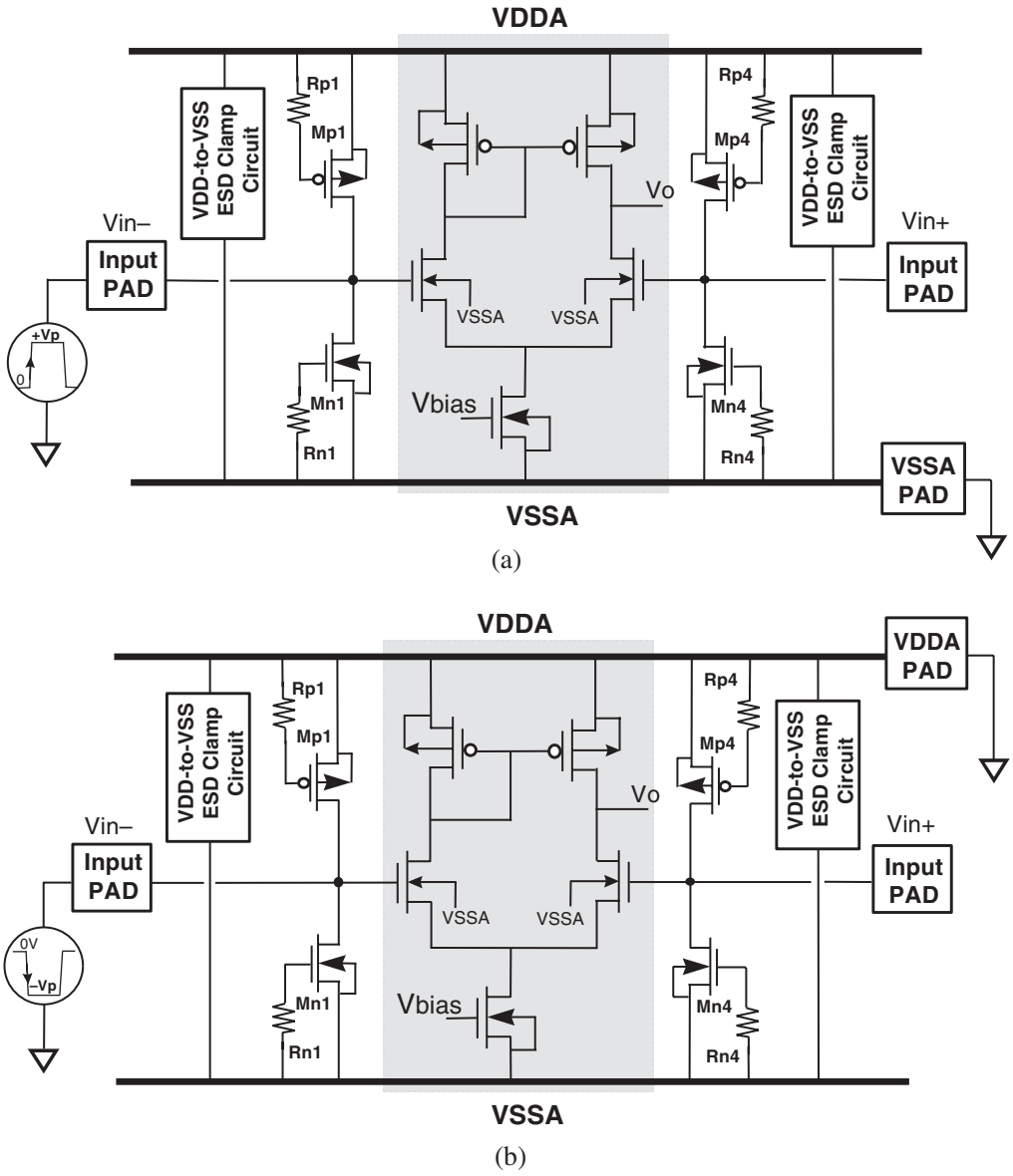
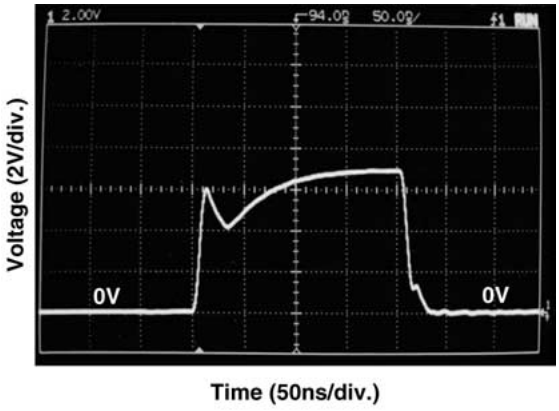
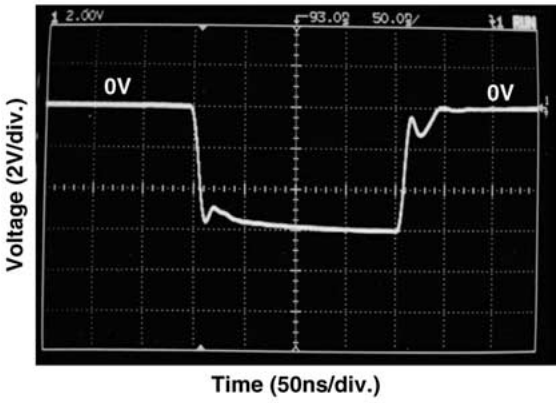


Fig. 19. The experimental setup to verify the turn-on efficiency of the proposed analog ESD protection circuit during (a) the PS-mode ESD stress, and (b) the ND-mode ESD stress.

the VDDA-to-VSSA ESD clamp device Mn3. The Mn1 and Mp1 in the input ESD protection circuit are operated in the junction diode forward-based condition, rather than the drain breakdown condition, therefore the proposed analog ESD protection circuit can sustain a much high ESD level even if the Mn1 and Mp1 have quite smaller device dimensions. So, the thinner gate oxide of the differential input stage can be safely protected by this proposed analog ESD protection circuit without adding the series resistance between the pad and the internal circuits. With quite smaller device dimensions in Mn1 and Mp1, the total input junction capacitance connected to the pad can be practically reduced for high-frequency applications.



(a)



(b)

Fig. 20. (a) The degraded voltage waveform when the positive 8 V voltage pulse is applied to the inverting analog input pin in the PS-mode ESD-stress condition. (b) The degraded voltage waveform when the negative −8 V voltage pulse is applied to the inverting analog input pin in the ND-mode ESD-stress condition.

6. Conclusion

An analog ESD protection circuit with a very low and almost constant input capacitance, high ESD level, but no series resistance, has been successfully designed and verified in a 0.35-μm silicided CMOS process. The ESD test results and turn-on verification have shown that the proposed analog ESD protection circuit can effectively protect the analog circuits, especially the differential input stage under the pin-to-pin ESD-stress condition. A design model to optimize the layout dimensions and spacings in the input ESD clamp devices has been also developed to keep the input capacitance almost constant. With suitable layout parameters on the input ESD clamp devices, the variation of total input capacitance of the proposed analog ESD protection circuit can be kept below 1% while the analog signal has a voltage swing of 1 V. With a very small and almost constant input capacitance, this proposed analog ESD protection circuit is very suitable to protect the analog input or output pins against ESD stress for current-mode, high-frequency, or high-resolution circuit applications.

Acknowledgments

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