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Layout design to minimize voltage-dependent variation on input capacitance of an analog ESD protection circuit ☆

Ming-Dou Ker*, Tung-Yang Chen

Integrated Circuits & Systems Laboratory, Institute of Electronics, National Chiao-Tung University, 1001 Ta-Hsueh Road, Hsinchu, Taiwan 300, ROC

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Abstract

A design model to find the optimized device dimensions and layout spacings on the input ESD clamp devices is developed in this work to keep the total input capacitance almost constant, even if the analog signal has a varying input voltage. An analog ESD protection circuit has been designed to solve ESD protection challenge on the analog pins for high-frequency applications. The device dimension (W/L) of ESD protection device connected to the I/O pad can be reduced to only 50 μm/0.5 μm in a 0.35-μm silicided CMOS process, but it can sustain HBM (MM) ESD level up to 6 kV (400 V). With such a smaller device dimension, the input capacitance of this analog ESD protection circuit can be significantly reduced to only ~0.4 pF for high-frequency applications. This input capacitance can be further reduced if the ESD protection devices are designed with smaller device dimensions. Moreover, by using the optimized layout design to draw the layout of ESD protection NMOS and PMOS devices, the voltage-dependent variation on input capacitance of this analog ESD protection circuit can be kept below 1% under an input voltage swing of 1 V. With such almost constant input capacitance, the nonlinear distortion causing by on-chip ESD protection circuit can be minimized for high-precision applications. © 2002 Elsevier Science B.V. All rights reserved.

Keywords: ESD; Analog circuit; Input capacitance

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*Corresponding author.
E-mail address: mdker@ieee.org (M.-D. Ker).

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1. Introduction

Electrostatic discharge (ESD) has become the main reliability concern on semiconductor products, especially in the scaled-down CMOS technologies [1,2]. Due to low breakdown voltage of the thinner gate oxide in deep-submicron CMOS technologies, efficient on-chip ESD protection circuit should be designed and placed on each pad to clamp the overstress voltage across internal circuits. The conventional input ESD protection circuit with two-stage protection scheme for digital input pins often has a series resistor connected between the primary ESD protection stage and the secondary ESD protection stage. But the large series resistance and the large junction capacitance in ESD clamp devices cause a long *RC* delay to the input signals, it is not suitable for analog pins, especially for the high-frequency applications [3–5]. For current-mode or RF input signals, the series resistance between the input pad and internal circuits is forbidden. Therefore, the traditional two-stage ESD protection design is no longer suitable for such analog input pins.

For some high-precision analog circuits, the input capacitance of an analog input pin including ESD protection circuit and a bond pad is required as constant as possible. A major distortion in analog circuits, especially in the single-ended input implementations, comes from the voltage-dependent nonlinear input capacitance of ESD clamp devices connected to the analog input pin. The typical degradation on analog circuit performance due to the nonlinear input capacitance of ESD clamp devices had been reported in [6], where the input capacitance was varying from 4 to 2 pF due to the input voltage increasing from 0 to 2 V. Such nonlinear input capacitance caused an increase on the harmonic distortion in an analog-to-digital converter (ADC), and degraded precision of the ADC from 14-bit to become only 10-bit. Thus for high-precision analog applications, the input capacitance generated from ESD clamp devices on the input pad needs to be kept as constant as possible.

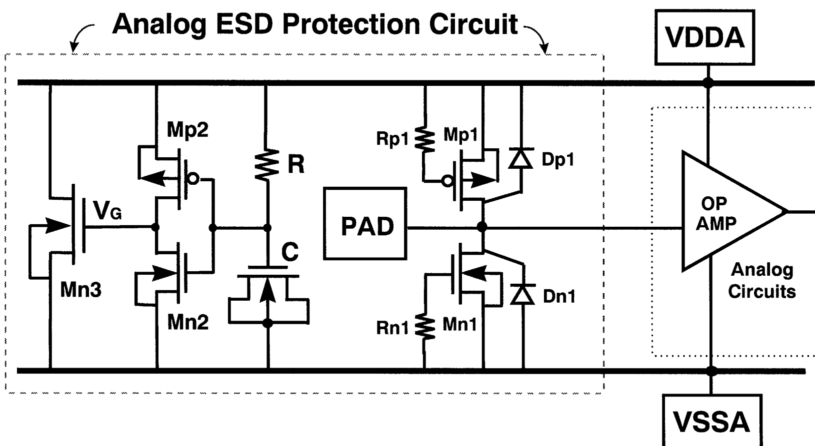


Fig. 1. The ESD protection circuit for high-frequency analog pin [7].

Recently, a turn-on efficient ESD protection circuit has been proposed to protect the high-frequency analog I/O pin, which is re-drawn in Fig. 1 [7]. This analog ESD protection circuit can sustain HBM (MM) ESD stress of up to 6 kV (400 V) in a 0.35-μm silicided CMOS process, but has a very small input capacitance of only ~0.4 pF for high-frequency applications. The circuit operations and experimental results of this analog ESD protection circuit will be briefly summarized in Section 2. In this paper, a design model to further optimize the device dimensions and layout spacings of this analog ESD protection circuit is developed to keep the input capacitance almost constant for more high-precision applications [8]. From the calculation results, the voltage-dependent variation on input capacitance of this analog ESD protection circuit can be designed below 1% while the analog input signal has a voltage swing of 1 V.

2. Analog ESD protection circuit

The analog ESD protection circuit is shown in Fig. 1, where Dp1 (Dn1) is the parasitic junction diode in drain region of Mp1 (Mn1) device. In order to reduce input capacitance on the analog pin, Mn1 and Mp1 are both designed with smaller device dimensions (W/L) of only 50 μm/0.5 μm [7]. The human-body-model (HBM) [9,10] ESD level of a stand-alone NMOS with a device dimension of 50 μm/0.5 μm is less than 500 V in the 0.35-μm silicided CMOS process, while the NMOS is zapped in the PS-mode (positive to VSS) ESD stress. But, such a small NMOS can sustain an HBM ESD level of greater than 6000 V in the same 0.35-μm silicided CMOS process, while the NMOS is zapped in the NS-mode (negative to VSS) ESD stress. In the PS-mode (NS-mode) ESD stress, the NMOS is operated in its drain junction reverse-breakdown (forward-bias) condition to discharge ESD current. Therefore, an NMOS has quite different ESD levels between the PS-mode and NS-mode ESD stresses. Of course, a stand-alone PMOS with a small device dimension also has a high ESD level in the PD-mode (positive to VDD) ESD stress, but has a much low ESD level in the ND-mode (negative to VDD) ESD stress.

To avoid the small-dimension Mn1 and Mp1 into the drain-breakdown condition under PS-mode or ND-mode ESD stresses to result in a much low ESD level, a turn-on efficient power-rail ESD clamp circuit is co-constructed into this analog ESD protection circuit to increase the overall ESD level. In Fig. 1, the RC-based ESD detection circuit [11,12] is used to trigger on Mn3 device, when the pad is zapped under PS-mode or ND-mode ESD stresses. The ESD current paths along this analog ESD protection circuit are illustrated by the dashed lines in Figs. 2(a) and (b), respectively, when the analog pin is zapped in the PS-mode and pin-to-pin ESD stresses. In Fig. 2(b), the pin-to-pin ESD stress across the two input pins of a differential input stage can be transferred across the VDDA and VSSA power lines. Mn3 connected between VDDA and VSSA power lines are turned on by the RC-based ESD detection circuit to conduct ESD current from VDDA to VSSA. Finally, ESD current flows out the chip from VSSA power line to the grounded pad through the forward-biased diode Dn4 in Mn4. With suitable design on the RC-based ESD

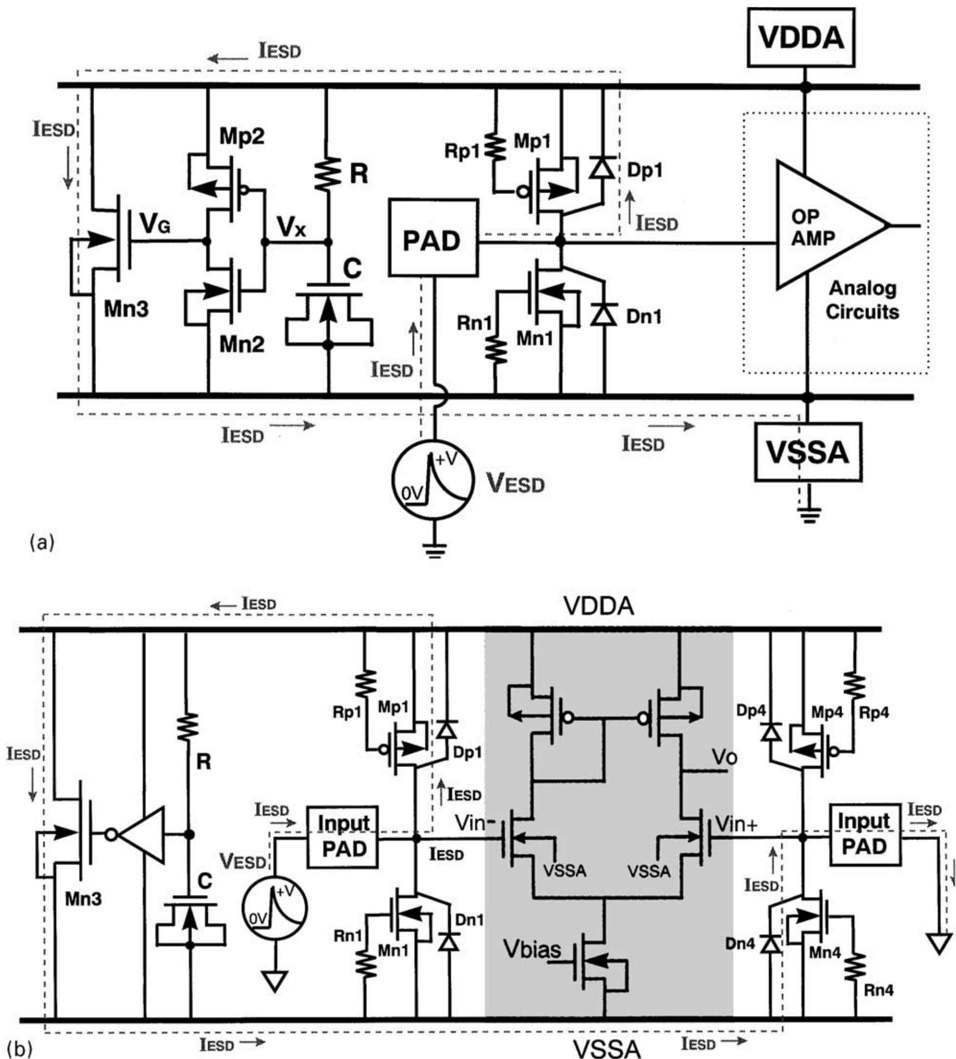


Fig. 2. The ESD current path along the analog ESD protection circuit when the analog pin is zapped in (a) the PS-mode, and (b) the pin-to-pin, ESD stresses.

detection circuit to quickly turn on Mn3, the pin-to-pin ESD stress can be effectively discharged away from the gate oxide of the differential input stage. Because Mn1 and Mp1 in this analog ESD protection circuit are not operated in the drain-breakdown condition, ESD current is discharged through the forward-biased drain diode Dp1 in Mp1 (Dn1 in Mn1) and the turned-on Mn3. So, Mn3 is especially designed with a larger device dimension (typically, $W/L = 1800\,\mu\text{m}/0.5\,\mu\text{m}$) to sustain a high ESD level. Although the large-dimension Mn3 has a large junction capacitance, this

capacitance does not contribute to the analog pad. Therefore, the analog pin can sustain a much higher ESD level but only with a very small input capacitance.

The spacing from drain contact to poly gate in both Mn1 and Mp1 is drawn as 3.4 μm, whereas the spacing at source side is drawn as 1.55 μm. With device dimension of 50 μm/0.5 μm in both Mn1 and Mp1, the input capacitance of this analog ESD protection circuit is varying from 0.37 to 0.4 pF when the input voltage increases from 0 to 3 V. But, the input capacitance of a grounded gate NMOS (ggNMOS) with a device dimension of 400 μm/0.5 μm varies from 1.83 to 1.12 pF, when the input voltage increases from 0 V to 3 V for an IC with 3 V VDD power supply.

This analog ESD protection circuit had been practically fabricated in a 0.35-μm silicided CMOS process with an operational amplifier as its input circuit. Both the inverting and non-inverting input pins are protected by this analog ESD protection circuit. The silicide-blocking layer is also drawn on the devices Mn1, Mp1, and Mn3 to improve their ESD robustness, but without using the additional ESD-implantation process. The test results of the maximum sustaining ESD voltage under different pin combinations are summarized in Table 1, which includes the analog pin-to-pin ESD stress. The failure criterion is defined as the leakage current at the pad exceeds 1 μA under 5 V voltage bias after any ESD zapping. As shown in Table 1, this analog ESD protection circuit can successfully provide analog pins with HBM (MM) ESD level of 6000 V (400 V) in all ESD-stress conditions.

To verify turn-on efficiency of this analog ESD protection circuit during the pin-to-pin ESD stress, a voltage pulse generated from a pulse generator (hp 8118 A) is applied to the inverting pin of an operational amplifier, whereas the non-inverting pin of this operational amplifier is relatively grounded and both the VDDA and VSSA pins are floating. The experimental setup to monitor turn-on efficiency under the positive pin-to-pin ESD stress is shown in Fig. 3(a). The measured voltage waveform under the positive pin-to-pin ESD stress is shown in Fig. 3(b). The original voltage pulse generated from pulse generator has a pulse height of 8 V and a pulse width of 200 ns. The 8 V voltage pulse has a rise time around $\sim$10 ns, which is similar to the rise time (5–15 ns) of an HBM ESD pulse. The drain breakdown voltage of NMOS Mn1 in the 0.35-μm silicide CMOS process without additional ESD implantation is 8.5 V. Therefore, the voltage pulse with a pulse height of 8 V does not cause drain breakdown on Mn1 in the analog ESD protection circuit.

Table 1
ESD level of the analog ESD protection circuit in human-body-model (HBM) and machine-model (MM) ESD stresses under different pin combinations

	Pin combination in ESD test				
	PS-mode	NS-mode	PD-mode	ND-mode	Pin-to-pin
HBM (V)	6000	− 8000	7000	− 7000	6000
MM (V)	400	− 400	400	− 400	400

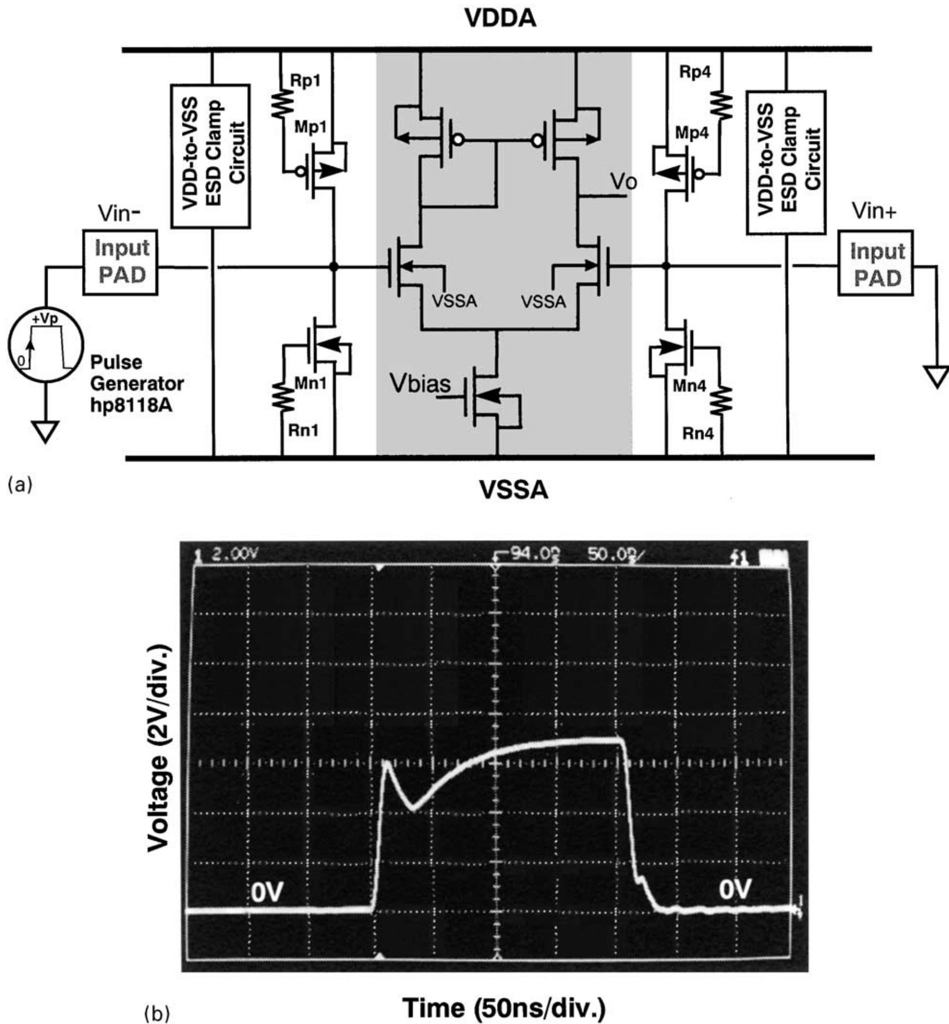
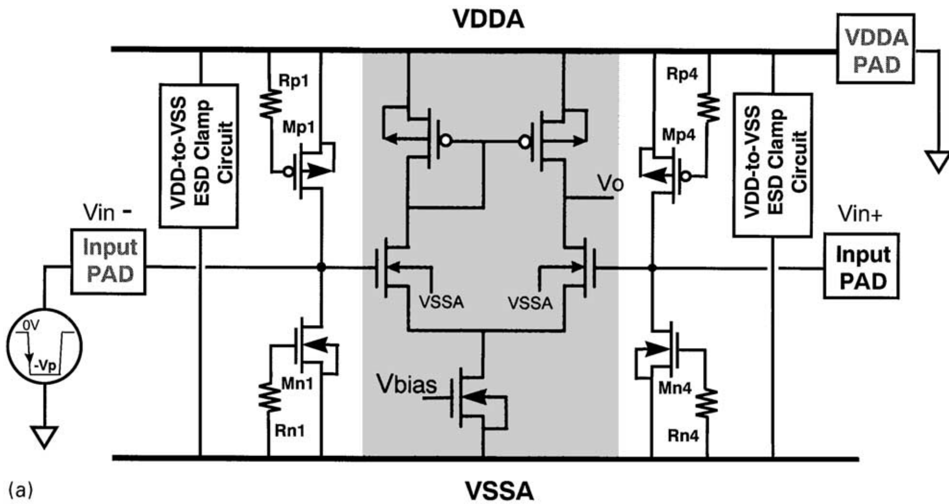


Fig. 3. (a) The experimental setup to verify turn-on efficiency of the analog ESD protection circuit during the positive pin-to-pin ESD stress condition. (b) The degraded voltage waveform when an 8 V voltage pulse is applied to the inverting input pin under the pin-to-pin ESD stress condition.

By applying such a voltage pulse to the analog pin, the turn-on efficiency of this analog ESD protection circuit can be clearly verified. While such a positive voltage pulse is applied to the analog pin as that shown in Fig. 3(a), it is clamped by the analog ESD protection circuit and the degraded voltage waveform is shown in Fig. 3(b). The pulse generator has a limited output current capability. The voltage pulse will be degraded if the analog ESD protection circuit is turned on, because the pulse generator cannot deliver enough current to sustain the voltage on the pad. The



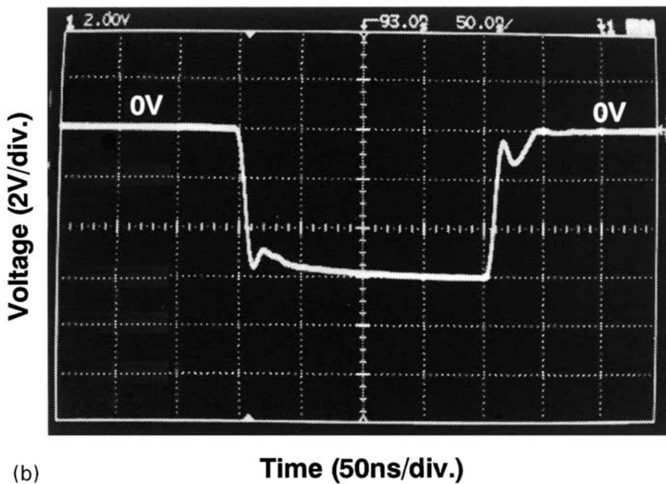


Fig. 4. (a) The experimental setup to verify turn-on efficiency of the analog ESD protection circuit during the ND-mode ESD stress. (b) The degraded voltage waveform when the negative (-8 V) voltage pulse is applied to the inverting input pin under the ND-mode ESD stress condition.

degraded voltage waveform proves that this analog ESD protection circuit can be actually turned on to clamp overstress voltage during the pin-to-pin ESD stress.

The turn-on efficiency of this analog ESD protection circuit during the ND-mode ESD stress is also verified with the experimental setup shown in Fig. 4(a). While the negative voltage pulse with a pulse height of -8 V and a pulse width of 200 ns is applied to the analog input pin under ND-mode ESD stress condition, it is clamped by the analog ESD protection circuit and the degraded voltage waveform on the pad

is shown in Fig. 4(b). This has practically verified the turn-on effectiveness of this analog ESD protection circuit.

From experimental verification, the positive or negative voltage pulses are really clamped by this analog ESD protection circuit. Mn1 and Mp1 in this analog ESD protection circuit are operated in diode forward-based condition, rather than the drain breakdown condition, therefore it can sustain a much high ESD level even if Mn1 and Mp1 only have much smaller device dimensions. With such smaller device dimensions in Mn1 and Mp1, the total junction capacitance connected to the input pad can be actually reduced for high-frequency applications.

3. Layout design on the input capacitance

For high-precision and high-frequency analog applications, the input capacitance generated from ESD protection devices needs to be kept not only small enough but also as constant as possible. In this Section, the input capacitance of this analog ESD protection circuit is calculated. A design model to optimize device dimensions and layout spacings on the ESD protection devices is developed to keep the input capacitance almost constant.

3.1. Calculation on the input capacitance

The main nonlinear source on the input capacitance comes from voltage-dependent junction capacitance at the drain regions of Mn1 and Mp1 in the analog ESD protection circuit. Such a drain junction capacitance increases while the magnitude of reverse-biased voltage across the junction decreases. The total input capacitance looking into the pad with this analog ESD protection circuit can be calculated as:

$$C_{\text{in}} = C_{\text{PAD}} + C_{\text{n}} + C_{\text{p}}, \tag{1}$$

where C_{PAD} is the parasitic capacitance of the bond pad. A bond pad structure formed by different metal layers and different layout area results in different parasitic capacitance to the substrate. Typically, a bond pad with a pad size of $96 \times 96\,\mu\text{m}^2$ and four metal layers in a 0.35-μm CMOS process has a parasitic capacitance of $\sim 0.67\,\text{pF}$. This bond pad capacitance can be further reduced, if the pad size is drawn smaller. C_{p} (C_{n}) is the drain capacitance of Mp1 (Mn1), which includes junction capacitance and the drain-to-gate overlapped capacitance. The drain junction capacitance of NMOS or PMOS is strongly voltage-dependent. When the signal voltage level on the input pad increases, the drain junction capacitance of Mn1 decreases but the drain junction capacitance of Mp1 increases. On the contrary, the drain junction capacitance of Mn1 increases but the drain junction capacitance of Mp1 decreases, when the signal voltage level on the input pad decreases. With complementary structure on ESD clamp devices, the total input capacitance can be kept almost constant if suitable device dimensions and layout spacings are selected to draw Mn1 and Mp1 devices.

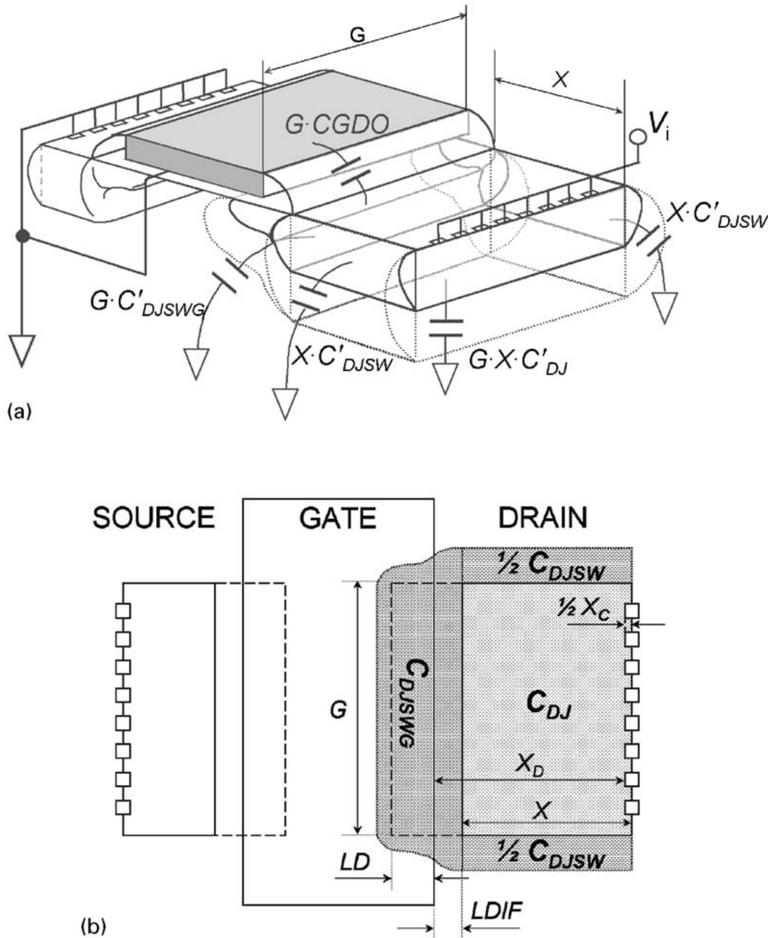


Fig. 5. (a) The three-dimension structure of a single-finger MOS device. (b) The corresponding layout top view of a single-finger MOS device with specified layout spacings.

The ESD protection NMOS and PMOS are generally drawn in the multi-finger structure with central drain to save total layout area in the I/O cells. The three-dimension structure of a single-finger NMOS (or PMOS) device is shown in Fig. 5(a), whereas the layout top view with the specified layout spacings is shown in Fig. 5(b). An MOS device with multi-finger structure can be realized by combining such single-finger structures with sharing drain and source regions between every two adjacent fingers. The finger length of a single poly finger is defined as G, which is also the channel width of the finger-type MOS device. The spacing from the center of drain contact to the edge of lightly-doped drain region is marked as X, which will be used in the following equations to calculate junction capacitance for the drain bottom plane. The clearance between the poly gate and the drain contact is marked

as X_D, and the width of drain contact is marked as X_C. Therefore, the spacing X defined in Fig. 5 can be written as

$$X = X_D + \frac{1}{2}X_C - LDIF, \tag{2}$$

where *LDIF* is the length of the lightly-doped drain diffusion adjacent to the gate. This *LDIF* is an extracted device parameter and given in the *SPICE* parameters of a CMOS process.

The drain region of MOS device with a single poly finger, which is shown in Fig. 5, has three different junction capacitances (C_{DJ}, C_{DJSW}, and C_{DJSWG}) and one drain-to-gate overlapped capacitance (C_{GD}). The equation of each capacitance is listed as [13]:

$$C_{GD} = CGDO\,G, \tag{3}$$

$$C_{DJ} = G\,X\,C'_{DJ}, \tag{4}$$

$$C_{DJSW} = 2X\,C'_{DJSW}, \tag{5}$$

$$C_{DJSWG} = G\,C'_{DJSWG}, \tag{6}$$

where

$$C'_{DJ} = CJ\left(1 + \frac{V_R}{PB}\right)^{-MJ} \mathrm{F/m^2}, \tag{7}$$

$$C'_{DJSW} = CJSW\left(1 + \frac{V_{SW}}{PBSW}\right)^{-MJSW} \mathrm{F/m}, \tag{8}$$

$$C'_{DJSWG} = CJSWG\left(1 + \frac{V_{SWG}}{PBSWG}\right)^{-MJSWG} \mathrm{F/m}. \tag{9}$$

C'_{DJ} is the junction capacitance per unit area of the drain bottom plane. C'_{DJSW} and C'_{DJSWG} are the junction capacitance per unit length of the drain region at the sidewall with field oxide and the sidewall with poly gate, respectively. The *SPICE* parameters used to calculate the capacitance of NMOS and PMOS devices in a 0.35-μm silicided CMOS process are summarized in Table 2 [14].

Substituting above equations into Eq. (1) with relative device parameters for Mn1 and Mp1, the total input capacitance C_{in} of the analog ESD protection circuit can be

Table 2
SPICE parameters on the drain capacitance of NMOS and PMOS devices in a 0.35-μm silicided CMOS process

	NMOS	PMOS
CGDO	2.79e-10 F/m	2.31e-10 F/m
CJ	1.01893e-3 F/m^2	1.46829e-3 F/m^2
CJSW	3.057956e-10 F/m	4.173308e-10 F/m
CJSWG	1.524314e-10 F/m	1.013197e-10 F/m
MJ	0.3075043	0.5464087
MJSW	0.1929617	0.3948903
MJSWG	0.1929617	0.3948903
PB	0.6944474 V	0.9191281 V
PBSW	0.6944494 V	0.9191281 V
PBSWG	0.6944494 V	0.9191281 V
LDIF	1.2e-7 m	1.2e-7 m

expressed as

$$
\begin{aligned}
C_{\mathrm{in}} = C_{\mathrm{PAD}} + k_{\mathrm{n}}\Bigg\{ & G_{\mathrm{n}}\, CGDO_{\mathrm{n}} + G_{\mathrm{n}}X_{\mathrm{n}}\, CJ_{\mathrm{n}}\left(1+\frac{V_{\mathrm{i}}}{PB_{\mathrm{n}}}\right)^{-MJ_{\mathrm{n}}} \\
& + G_{\mathrm{n}}\, CJSWG_{\mathrm{n}}\left(1+\frac{V_{\mathrm{i}}}{PBSWG_{\mathrm{n}}}\right)^{-MJSWG_{\mathrm{n}}} \\
& + 2X_{\mathrm{n}}\, CJSW_{\mathrm{n}}\left(1+\frac{V_{\mathrm{i}}}{PBSW_{\mathrm{n}}}\right)^{-MJSW_{\mathrm{n}}}\Bigg\} \\
+ k_{\mathrm{p}}\Bigg\{ & G_{\mathrm{p}}\, CGDO_{\mathrm{p}} + G_{\mathrm{p}}X_{\mathrm{p}}\, CJ_{\mathrm{p}}\left(1+\frac{V_{\mathrm{DD}}-V_{\mathrm{i}}}{PB_{\mathrm{p}}}\right)^{-MJ_{\mathrm{p}}} \\
& + G_{\mathrm{p}}\, CJSWG_{\mathrm{p}}\left(1+\frac{V_{\mathrm{DD}}-V_{\mathrm{i}}}{PBSWG_{\mathrm{p}}}\right)^{-MJSWG_{\mathrm{p}}} \\
& + 2X_{\mathrm{p}}\, CJSW_{\mathrm{p}}\left(1+\frac{V_{\mathrm{DD}}-V_{\mathrm{i}}}{PBSW_{\mathrm{p}}}\right)^{-MJSW_{\mathrm{p}}}\Bigg\}, \qquad (10)
\end{aligned}
$$

where k_{n} (k_{p}) is the finger number of the poly gate in the multi-finger Mn1 (Mp1) layout; G_{n} (G_{p}) is the finger length of the poly gate in the multi-finger Mn1 (Mp1) layout; X_{n} (X_{p}) is the layout spacing from the drain contact to the poly gate, defined in Eq. (2), in the multi-finger Mn1 (Mp1) layout; and V_{i} is input voltage level on the pad.

3.2. Layout design to minimize capacitance variation

When layout spacings in Mn1 and Mp1 are modified, the total input capacitance of the analog ESD protection circuit can be adjusted. Based on Eq. (10), the desired layout parameters to minimize variation on the voltage-dependent input capacitance can be obtained. The partial differential equation of (10) on the input voltage is

derived as

$$\begin{aligned}\frac{\partial C_{\rm in}}{\partial V_{\rm i}} = k_{\rm n}\Bigg\{ & -MJ_{\rm n}G_{\rm n}X_{\rm n}\frac{CJ_{\rm n}}{PB_{\rm n}}\left(1+\frac{V_{\rm i}}{PB_{\rm n}}\right)^{-MJ_{\rm n}-1} \\ & -MJSWG_{\rm n}\,G_{\rm n}\frac{CJSWG_{\rm n}}{PBSWG_{\rm n}}\left(1+\frac{V_{\rm i}}{PBSWG_{\rm n}}\right)^{-MJSWG_{\rm n}-1} \\ & -2MJSW_{\rm n}\,X_{\rm n}\frac{CJSW_{\rm n}}{PBSW_{\rm n}}\left(1+\frac{V_{\rm i}}{PBSW_{\rm n}}\right)^{-MJSW_{\rm n}-1}\Bigg\} \\ + k_{\rm p}\Bigg\{ & MJ_{\rm p}\,G_{\rm p}X_{\rm p}\frac{CJ_{\rm p}}{PB_{\rm p}}\left(1+\frac{V_{\rm DD}-V_{\rm i}}{PB_{\rm p}}\right)^{-MJ_{\rm p}-1} \\ & +MJSWG_{\rm p}\,G_{\rm p}\frac{CJSWG_{\rm p}}{PBSWG_{\rm p}}\left(1+\frac{V_{\rm DD}-V_{\rm i}}{PBSWG_{\rm p}}\right)^{-MJSWG_{\rm p}-1} \\ & +2MJSW_{\rm p}\,X_{\rm p}\frac{CJSW_{\rm p}}{PBSW_{\rm p}}\left(1+\frac{V_{\rm DD}-V_{\rm i}}{PBSW_{\rm p}}\right)^{-MJSW_{\rm p}-1}\Bigg\}. \end{aligned} \tag{11}$$

If the value of Eq. (11) were equal to zero, the input capacitance would be independent to the input voltage level. Unfortunately, the layout parameters ($K_{\rm n}$, $K_{\rm p}$, $G_{\rm n}$, $G_{\rm p}$, $X_{\rm n}$, and $X_{\rm p}$) on Mn1 and Mp1 devices with the specified *SPICE* parameters in a 0.35-μm silicided CMOS process cannot keep this $\partial C_{\rm in}/\partial V_{\rm i}$ always zero, while the input signal has a voltage swing from 0 V to VDD (3 V).

In analog applications, the analog input signal generally has a common reference voltage, indicated as $V_{\rm com}$ in this paper. For symmetrical analog input signals with a maximum amplitude of ΔV, the minimum ($V_{\rm min}$) and maximum ($V_{\rm max}$) voltage level of analog input signals can be written as

$$V_{\rm min} = V_{\rm com} - \Delta V, \tag{12}$$

and

$$V_{\rm max} = V_{\rm com} + \Delta V. \tag{13}$$

According to the mean value theorem [15], if input capacitances at the voltage levels of $V_{\rm min}$ and $V_{\rm max}$ are kept the same, the condition of $\partial C_{\rm in}/\partial V_{\rm i} = 0$ is located within this analog input voltage range. Therefore, the input capacitance can have a minimized variation within the analog input voltage range between $V_{\rm min}$ and $V_{\rm max}$. Substituting $V_{\rm min}$ and $V_{\rm max}$ into Eq. (10), the condition of $C_{\rm in}(V_{\rm max}) = C_{\rm in}(V_{\rm min})$ to keep the minimum variation on input capacitance can be obtained as

$$k_{\rm n}\{\alpha G_{\rm n}X_{\rm n} + \beta G_{\rm n} + 2\gamma X_{\rm n}\} = k_{\rm p}\{\eta G_{\rm p}X_{\rm p} + \theta G_{\rm p} + 2\kappa X_{\rm p}\}, \tag{14}$$

where

$$\alpha = CJ_{\rm n}\left[\left(1+\frac{V_{\rm min}}{PB_{\rm n}}\right)^{-MJ_{\rm n}} - \left(1+\frac{V_{\rm max}}{PB_{\rm n}}\right)^{-MJ_{\rm n}}\right], \tag{15}$$

$$\beta = CJSWG_{\mathrm{n}}\left[\left(1+\frac{V_{\min}}{PBSWG_{\mathrm{n}}}\right)^{-MJSWG_{\mathrm{n}}}-\left(1+\frac{V_{\max}}{PBSWG_{\mathrm{n}}}\right)^{-MJSWG_{\mathrm{n}}}\right], \quad (16)$$

$$\gamma = CJSW_{\mathrm{n}}\left[\left(1+\frac{V_{\min}}{PBSW_{\mathrm{n}}}\right)^{-MJSW_{\mathrm{n}}}-\left(1+\frac{V_{\max}}{PBSW_{\mathrm{n}}}\right)^{-MJSW_{\mathrm{n}}}\right], \quad (17)$$

$$\eta = CJ_{\mathrm{p}}\left[\left(1+\frac{V_{\mathrm{DD}}-V_{\max}}{PB_{\mathrm{p}}}\right)^{-MJ_{\mathrm{p}}}-\left(1+\frac{V_{\mathrm{DD}}-V_{\min}}{PB_{\mathrm{p}}}\right)^{-MJ_{\mathrm{p}}}\right], \quad (18)$$

$$\theta = CJSWG_{\mathrm{p}}\left[\left(1+\frac{V_{\mathrm{DD}}-V_{\max}}{PBSWG_{\mathrm{p}}}\right)^{-MJSWG_{\mathrm{p}}}-\left(1+\frac{V_{\mathrm{DD}}-V_{\min}}{PBSWG_{\mathrm{p}}}\right)^{-MJSWG_{\mathrm{p}}}\right], \quad (19)$$

$$\kappa = CJSW_{\mathrm{p}}\left[\left(1+\frac{V_{\mathrm{DD}}-V_{\max}}{PBSW_{\mathrm{p}}}\right)^{-MJSW_{\mathrm{p}}}-\left(1+\frac{V_{\mathrm{DD}}-V_{\min}}{PBSW_{\mathrm{p}}}\right)^{-MJSW_{\mathrm{p}}}\right]. \quad (20)$$

By applying the device parameters of Mn1 and Mp1 summarized in Table 2 into Eqs. (14)–(20), the condition to keep the input capacitance with minimum variation under the voltage levels of $V_{\mathrm{DD}} = 3\,\mathrm{V}$, $V_{\mathrm{com}} = 1.5\,\mathrm{V}$, and $\Delta V = 0.5\,\mathrm{V}$ can be found as

$$\begin{aligned} &k_{\mathrm{n}}\{1.029515\times10^{-4}\,G_{\mathrm{n}}X_{\mathrm{n}} + 1.098674\times10^{-11}\,G_{\mathrm{n}} + 2.204072\times10^{-11}\,X_{\mathrm{n}}\} \\ &\quad = k_{\mathrm{p}}\{2.011205\times10^{-4}\,G_{\mathrm{p}}X_{\mathrm{p}} + 1.156346\times10^{-11}G_{\mathrm{p}} + 4.762930\times10^{-11}X_{\mathrm{p}}\}. \end{aligned} \quad (21)$$

Therefore, if the layout parameters (K_{n}, K_{p}, G_{n}, G_{p}, X_{n}, and X_{p}) on the multi-finger Mn1 and Mp1 devices are correctly chosen to meet the condition in Eq. (21), the minimum variation on input capacitance of this analog ESD protection circuit can be achieved within the desired input voltage range. This implies that only choosing suitable device dimensions and layout spacings in the multi-finger Mn1 and Mp1 devices can minimize the variation on input capacitance of ESD protection circuit. This is quite useful to design this analog ESD protection circuit with an almost-constant input capacitance for high-precision analog applications in a given CMOS process.

3.3. Calculation results

Now, if $k_{\mathrm{p}} = k_{\mathrm{n}} = 2$ and $G_{\mathrm{p}} = G_{\mathrm{n}} = 25\,\mu\mathrm{m}$ are chosen with the voltage levels of $V_{\mathrm{DD}} = 3\,\mathrm{V}$, $V_{\mathrm{com}} = 1.5\,\mathrm{V}$, and $\Delta V = 0.5\,\mathrm{V}$, the relation between layout spacings of X_{n} and X_{p} to meet the condition of Eq. (21) is calculated in Fig. 6(a), where X_{n} is found to be linearly dependent on X_{p}. Based on this condition with the specified layout parameters, the relation between the total input capacitance (without including C_{PAD}) and the input voltage level is calculated from Eq. (10) and shown in Fig. 6(b). The simulation results from *HSPICE* on the total input capacitance (without including C_{PAD}) of the analog ESD protection circuit are also included in

Fig. 6(b) to verify the accuracy of the derived design model. The model calculated results agree very well to the *HSPICE* simulated results in Fig. 6(b) under many sets of different layout parameters, where each set of different layout parameters meets the condition of Eq. (21). As shown in Fig. 6(b), if the layout parameters X_n and X_p

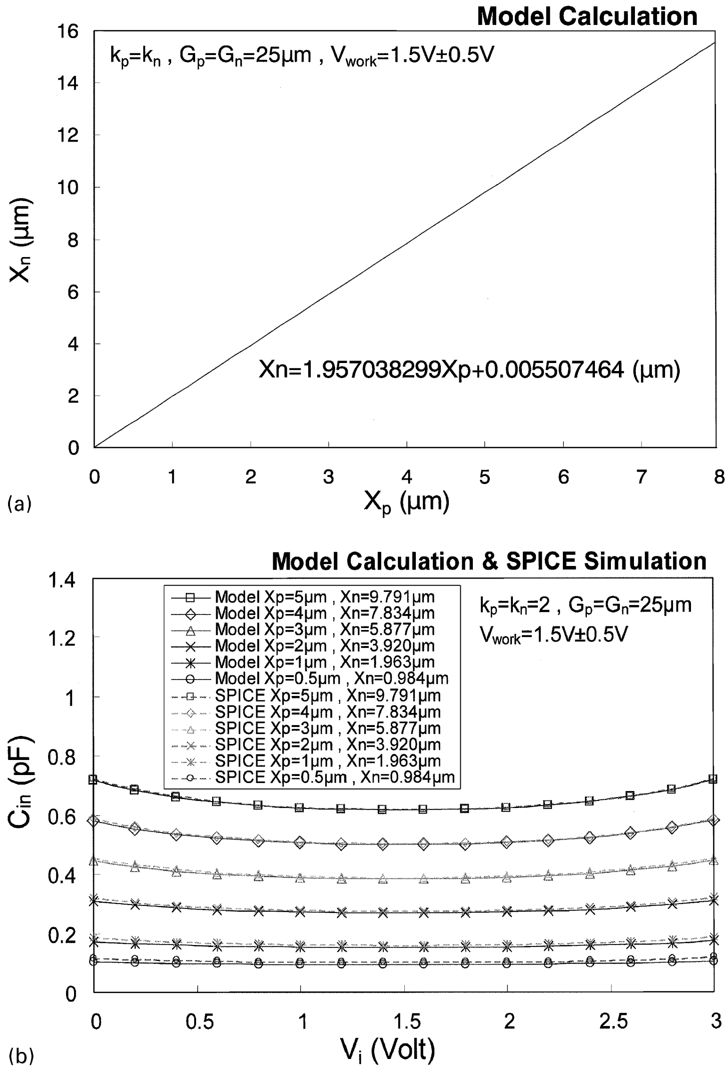


Fig. 6. (a) The relation between layout parameters X_n and X_p to meet the condition in Eq. (21) with the analog common reference voltage biased at 1.5 V. (b) The relation between the total input capacitance and the input voltage level under different layout parameters X_n and X_p. (c) The relation between the variation percentage on the input capacitance and the input voltage level under different layout parameters X_n and X_p. (d) The relation between the calculated $\partial C_{in}/\partial V_i$ value and the input voltage level under different layout parameters X_n and X_p.

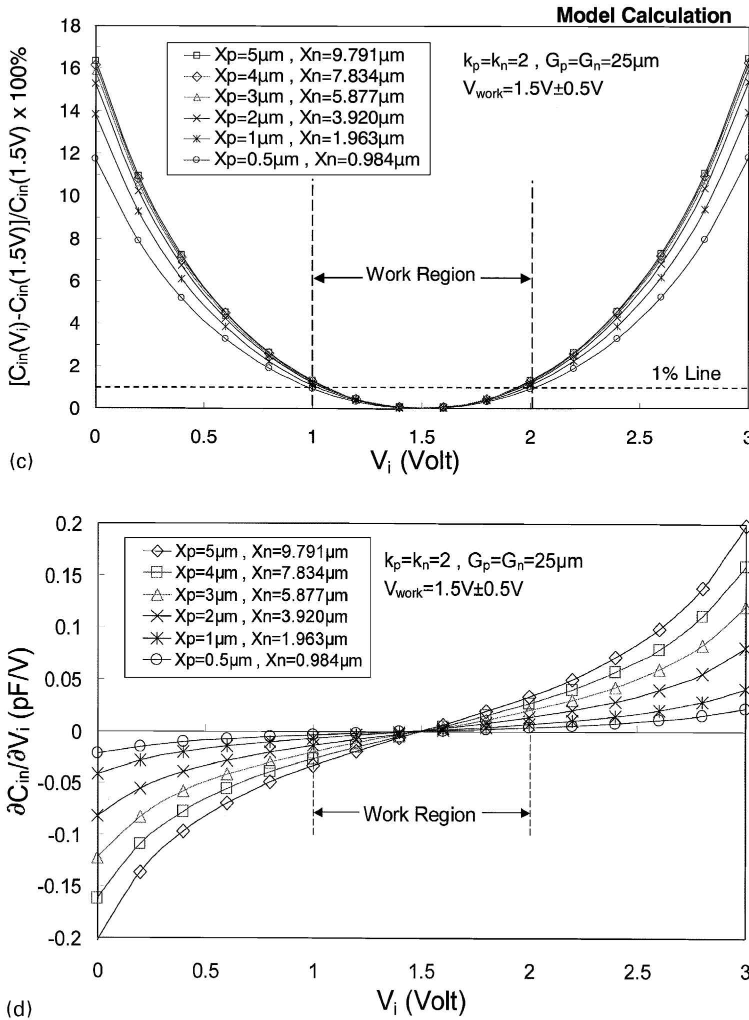


Fig. 6. (*Continued*).

are chosen with smaller values, the analog ESD protection circuit also has a smaller input capacitance. Besides, the analog ESD protection circuit has the smallest input capacitance, when the input voltage level is biased at the analog common reference voltage V_{com}. The percentage of variation on the input capacitance in Fig. 6(b) with respect to the smallest input capacitance at $V_{com} = 1.5\,V$ under different layout parameters are calculated and drawn as a function of input voltage in Fig. 6(c). If the layout parameters X_n and X_p are chosen with smaller values, the analog ESD protection circuit also has a smaller variation percentage on its input capacitance. Based on such layout parameters found by Eq. (21), the relation between the partial differential value of $\partial C_{in}/\partial V_i$ calculated from Eq. (11) and the input voltage is shown

in Fig. 6(d). The $\partial C_{in}/\partial V_i$ has a value of zero when the input voltage level just biased at the V_{com} of 1.5 V. Within the desired analog input voltage range of 1–2 V, the variation percentage on input capacitance is found within 1% in the work region shown in Fig. 6(c). With such a small 1% variation on the input capacitance, this analog ESD protection circuit is very suitable for high-frequency and high-precision analog applications.

In Fig. 6(a)–(d), the input capacitance is calculated with the analog common reference voltage (V_{com}) chosen at 1.5 V, which is equal to the half of 3 V VDD. If analog input signals have different common reference voltages, the input capacitance with minimum variation within the desired input voltage range can be still found from above equations. For example, if the voltage levels of $V_{DD} = 3$ V, $V_{com} = 1.0$ V, and $\Delta V = 0.5$ V are chosen with $k_p = k_n = 2$ and $G_p = G_n = 25\,\mu m$, the relation between X_n and X_p to sustain the condition of Eq. (14) becomes $X_n = 1.01604\,X_p - 0.04261968$. Based on this condition, the relation between the input capacitance and the input voltage level is calculated in Fig. 7(a), and the variation percentage on input capacitance (without including C_{PAD}) is shown in Fig. 7(b) under many sets of layout parameters. Because the analog common reference voltage (V_{com}) is chosen at 1.0 V in Fig. 7, the input capacitance has the smallest capacitance when the input voltage level is biased at 1 V. Within the desired analog input voltage range of 0.5–1.5 V, the variation percentage on input capacitance is also within 1% in the work region shown in Fig. 7(b).

On the contrary, if the analog common reference voltage (V_{com}) is chosen at 2.0 V for analog applications with a higher input voltage level, the relation between X_n and X_p to sustain the condition of Eq. (14) becomes $X_n = 3.75596\,X_p + 0.09672$ with the other parameters of $V_{DD} = 3$ V, $\Delta V = 0.5$ V, $k_p = k_n = 2$, and $G_p = G_n = 25\,\mu m$. Based on this condition, the relation between the input capacitance (without including the C_{PAD}) and the input voltage level is calculated in Fig. 8(a), and the variation percentage on input capacitance is shown in Fig. 8(b) under many sets of layout parameters. Because the analog common reference voltage (V_{com}) is chosen at 2.0 V in Fig. 8, the input capacitance has the smallest capacitance when the input voltage level is biased at 2 V. Within the desired analog input voltage range of 1.5–2.5 V, the variation percentage of the input capacitance is also within 1% in the work region shown in Fig. 8(b). This has shown the flexibility of the derived design model to find suitable layout parameters for minimizing the voltage-dependent variation on input capacitance of the analog ESD protection circuit.

The calculated results in Figs. 6–8 are all based on the same layout parameters of $k_p = k_n = 2$ and $G_p = G_n = 25\,\mu m$ but with different layout parameters of X_n and X_p. The layout parameter of X_n (X_p) has been defined in Eq. (2) and Fig. 5 for Mn1 (Mp1) in the analog ESD protection circuit. For the most general analog applications with the analog common reference voltage (V_{com}) biased at $V_{DD}/2$ (= 1.5 V), the relation between X_n and X_p has been shown in Fig. 6(a), where X_n is almost two times of X_p to meet the condition in Eq. (21). For example, if X_p is chosen at 4 μm, the corresponding X_n must be drawn about 8.07 μm. With such a wider X_n, the layout area of Mn1 is increased but the W/L of Mn1 still keeps the same, as comparing to the original layout design with the same X_n and X_p.

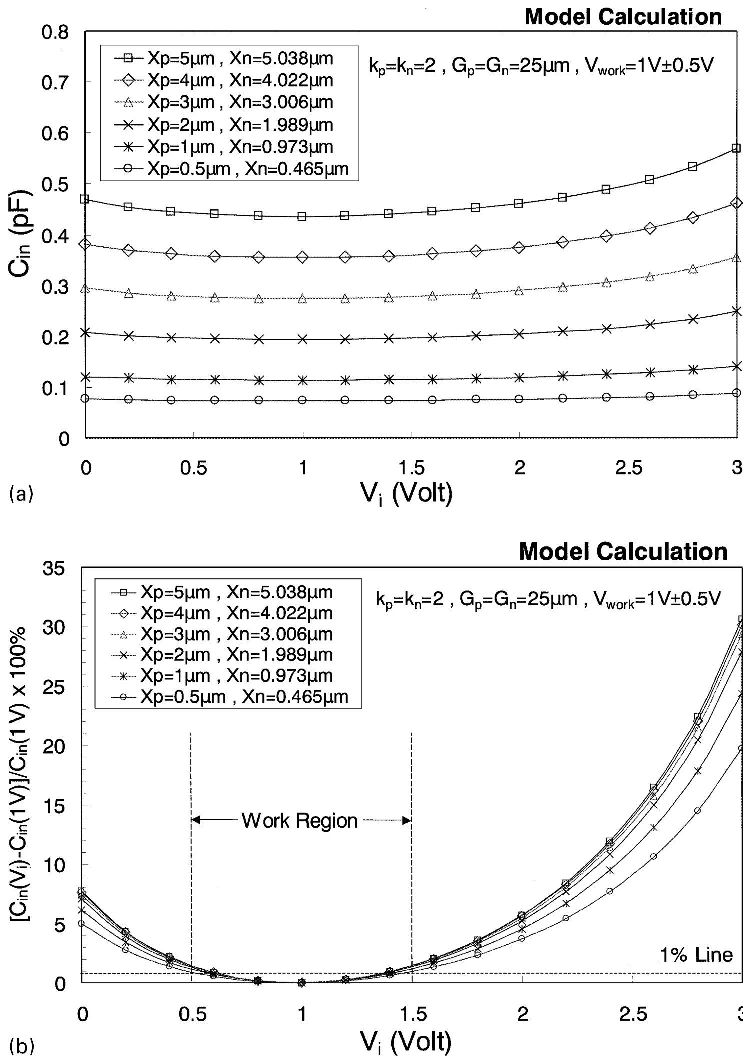


Fig. 7. The relations between (a) the total input capacitance, and (b) the variation percentage on the input capacitance, of the analog ESD protection circuit and the input voltage level under different layout parameters X_n and X_p, which meet the condition in Eq. (14) with an analog common reference voltage biased at 1.0 V.

If the finger number (k_n) of Mn1 is increased from 2 to 4, the ratio between X_n and X_p can be found at around 1.0 under the condition of $G_p = G_n$. Moreover, the total device dimension (W/L) of Mn1 can be increased when the finger number (k_n) of Mn1 is increased from 2 to 4. The relation between the X_n/X_p ratio and the finger length G_p (G_n) to meet the condition of Eq. (21) is further calculated in Fig. 9(a), where the other parameters are $V_{DD} = 3\,V$, $V_{com} = 1.5\,V$, $\Delta V = 0.5\,V$, $k_p = 2$, and $k_n = 4$. In Fig. 9(a), the X_n/X_p ratio is kept around 1 with only slight variation (from

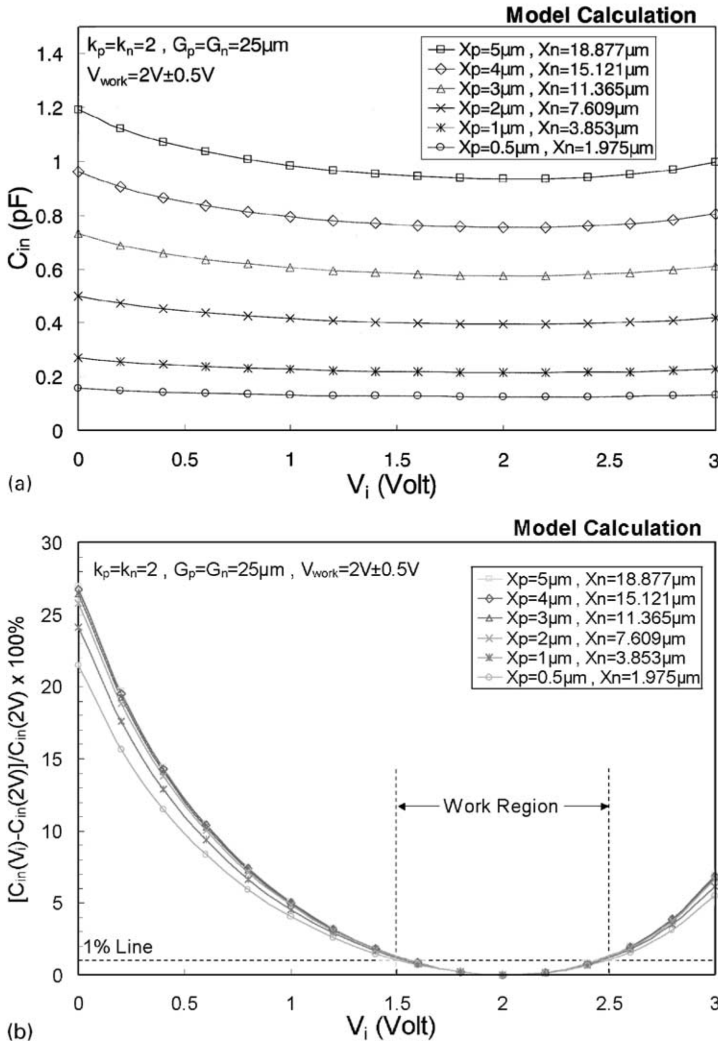
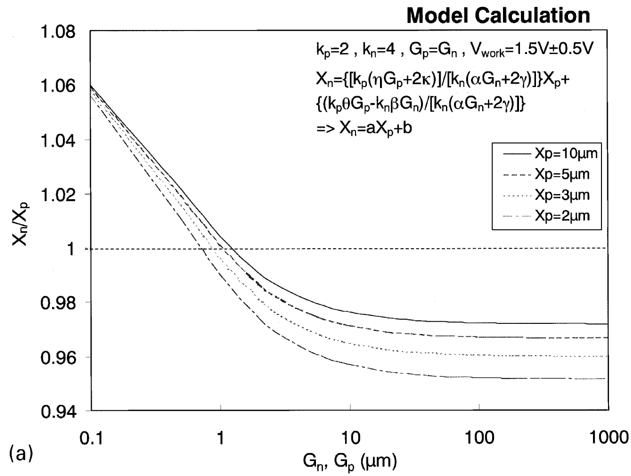
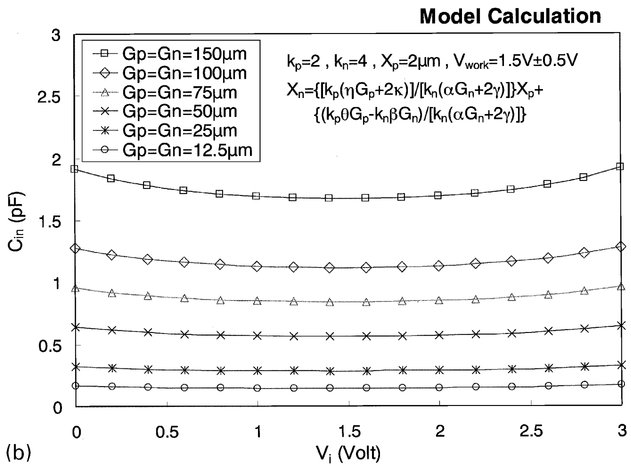
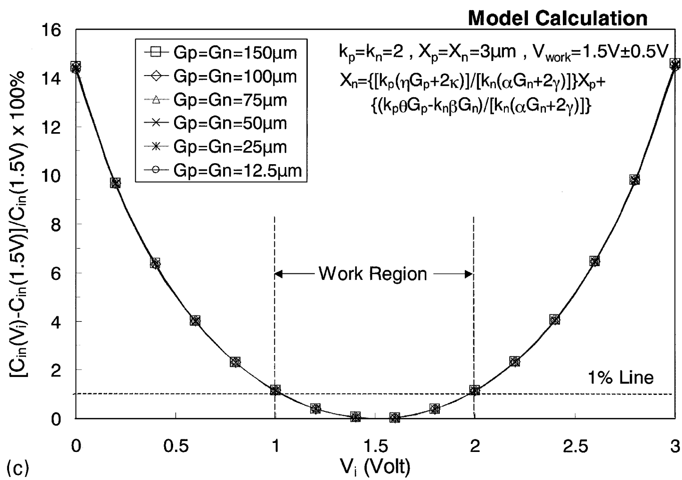


Fig. 8. The relations between (a) the total input capacitance, and (b) the variation percentage on the input capacitance, of the analog ESD protection circuit and the input voltage level under different layout parameters X_{n} and X_{p}, which meet the condition in Eq. (14) with an analog common reference voltage biased at 2.0 V.

Fig. 9. (a) The relation between the ratio of $X_{\mathrm{n}}/X_{\mathrm{p}}$ and the finger lengths G_{n} and G_{p} to meet the condition in Eq. (21) with $k_{\mathrm{p}} = 2$, $k_{\mathrm{n}} = 4$, and $V_{\mathrm{work}} = 1.5 \pm 0.5\,\mathrm{V}$. (b) The relation between the total input capacitance of the analog ESD protection circuit and the input voltage level under different layout parameters G_{n} and G_{p}. (c) The relation between the variation percentage on the input capacitance and the input voltage level under different layout parameters G_{n} and G_{p}.


Model Calculation
kp=2 , kn=4 , Gp=Gn , Vwork=1.5V±0.5V
Xn={[kp(ηGp+2κ)]/[kn(αGn+2γ)]}Xp+
{(kpθGp-knβGn)/[kn(αGn+2γ)]}
=> Xn=aXp+b
Xp=10µm
Xp=5µm
Xp=3µm
Xp=2µm
Xn/Xp
Gn, Gp (µm)
(a)


Model Calculation
Gp=Gn=150µm
Gp=Gn=100µm
Gp=Gn=75µm
Gp=Gn=50µm
Gp=Gn=25µm
Gp=Gn=12.5µm
kp=2 , kn=4 , Xp=2µm , Vwork=1.5V±0.5V
Xn={[kp(ηGp+2κ)]/[kn(αGn+2γ)]}Xp+
{(kpθGp-knβGn)/[kn(αGn+2γ)]}
Cin (pF)
Vi (Volt)
(b)


Model Calculation
Gp=Gn=150µm
Gp=Gn=100µm
Gp=Gn=75µm
Gp=Gn=50µm
Gp=Gn=25µm
Gp=Gn=12.5µm
kp=kn=2 , Xp=Xn=3µm , Vwork=1.5V±0.5V
Xn={[kp(ηGp+2κ)]/[kn(αGn+2γ)]}Xp+
{(kpθGp-knβGn)/[kn(αGn+2γ)]}
Work Region
1% Line
[Cin(Vi)-Cin(1.5V)]/Cin(1.5V) x 100%
Vi (Volt)
(c)

1.06 to 0.95), even if the finger length G_p (G_n) of Mp1 (Mn1) has a wide-range variation from 0.1 to 1000 μm in the 0.35-μm silicided CMOS process. Based on the chosen layout parameters, the relation between input capacitance and input voltage level is calculated in Fig. 9(b), and the variation percentage on input capacitance is shown in Fig. 9(c) under different sets of layout parameters G_p and G_n. The variation percentage on input capacitance under different layout parameters G_p and G_n is almost the same, as that shown in Fig. 9(c). Within the chosen $V_{work} = 1.5\,V \pm 0.5\,V$, the variation percentage on input capacitance is still kept below 1%.

From above detailed calculations and analyses on the input capacitance, the derived design model to find suitable layout parameters for minimizing the input capacitance variation can help the analog ESD protection circuit to be well realized in general CMOS processes. The input capacitances calculated and shown in Figs. 6–9 only include the junction capacitances of ESD protection NMOS and PMOS in the analog ESD protection circuit. The bond pad capacitance (C_{PAD}) with a wide metal plate to the substrate is essentially a constant capacitor. This bond pad capacitance (C_{PAD}) can be further reduced 50% by a low-C layout design [16]. In the silicon-on-insulator (SOI) CMOS process, ESD protection diodes can be stacked from the pad to VDD and VSS to further reduce the total input junction capacitance. By using the same concept of this design model, the optimized layout for the stacked SOI diodes can be found to further minimize the voltage-dependent variation on input capacitance of ESD protection circuits for more high-precision and high-frequency applications.

If the pure junction diodes are used in this analog ESD protection circuit to replace Mn1 and Mp1 devices, similar calculation as that shown in this design model can be also derived to find the optimized layout for minimizing variation on the voltage-dependent input capacitance. The design model described in this paper has been derived under the layout condition of Mn1 and Mp1 devices having even number of poly gate fingers. If Mn1 and Mp1 devices are drawn with an odd number of total poly gate fingers, an additional sidewall junction capacitance ($G\,C'_{DJSW}$) should be added into the capacitance equation in Eq. (10) with some modification. But, such a layout style of ESD protection NMOS having an odd number of total poly gate fingers is not recommended in IC products, because the parasitic device interaction between the unguarded drain diffusion and a nearby N+ diffusion often causes some unexpected ESD damages to lower the overall ESD level [17].

4. Conclusion

An analog ESD protection circuit with a very low and almost constant input capacitance, high ESD level, but no series resistance, has been successfully designed and verified in a 0.35-μm silicided CMOS process. The ESD test results and turn-on verifications have shown that this analog ESD protection circuit can effectively protect the analog circuits, especially the differential input stage under the pin-to-pin ESD stress condition. A design model to optimize the device dimensions and layout spacings of ESD protection devices has been clearly developed to keep the input

capacitance as constant as possible in general CMOS processes. If analog input signals have different common reference voltages, this design model can still find suitable device dimensions and layout spacings on ESD protection devices to keep the input capacitance with minimum variation during the desired input voltage range. This has shown the flexibility of the derived model for minimizing voltage-dependent variation on input capacitance of the ESD protection circuit. With suitable layout parameters on the input ESD clamp devices, the variation of total input capacitance of the analog ESD protection circuit can be designed below 1% while the analog input signal has an input voltage swing of 1 V. With a much small and almost constant input capacitance, this analog ESD protection circuit is very suitable for current-mode, high-frequency, and high-precision circuit applications with high enough ESD reliability.

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