Analysis on the Dependence of Layout Parameters on ESD Robustness of CMOS Devices for Manufacturing in Deep-Submicron CMOS Process

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Abstract—**The layout dependence on ESD robustness of NMOS and PMOS devices has been experimentally investigated in details. A lot of CMOS devices with different device dimensions, layout spacings, and clearances have been drawn and fabricated to find the optimized layout rules for electrostatic discharge (ESD) protection. The main layout parameters to affect ESD robustness of CMOS devices are the channel width, the channel length, the clearance from contact to poly-gate edge at drain and source regions, the spacing from the drain diffusion to the guardring diffusion, and the finger width of each unit finger. Non-uniform turn-on effects have been clearly investigated in the gate-grounded large-dimension NMOS devices by using EMMI (*EMi*ssion *MI*croscope) observation. The optimized layout parameters have been verified to effectively improve ESD robustness of CMOS devices. The relations between ESD robustness and the layout parameters have been explained by both transmission line pulsing (TLP) measured data and the energy band diagrams.**

Index Terms—**Energy band diagram, electrostatic discharge (ESD), second breakdown, snapback.**

I. Introduction

To SUSTAIN reasonable electrostatic discharge (ESD) robustness in deep-submicron CMOS integrated circuits (ICs), on-chip ESD protection circuits must be added into the chips [1]. ESD level of commercial IC products is generally required to be greater than 2kV under human-body-model (HBM) ESD stress [2]. The typical design of efficient ESD protection circuits in a CMOS IC is shown in Fig. 1 to protect the internal circuits against ESD damage [3]. But, circuit designers often confuse on how to optimize those ESD protection devices such as Mn1, Mn2, Mn3, Mp1, and Mp2 in Fig. 1. To design area-efficient ESD protection circuits, the ESD protection devices are desired as robust as possible in a limited layout area. To sustain the required ESD level, on-chip ESD protection circuits are often drawn with larger device dimensions. Such ESD protection devices with larger device dimensions are often realized with multiple fingers to reduce total layout area [4]. The device structure of finger-type NMOS with some specified layout parameters is shown in Fig. 2. Some layout parameters can affect ESD robustness of those ESD protection devices [5]–[7].

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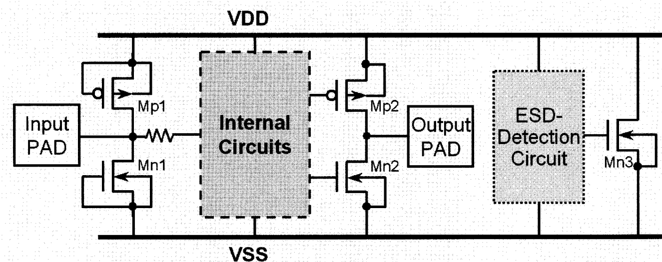

Fig. 1. Typical on-chip ESD protection circuits in a CMOS IC.

To optimize the turn-on efficiency of CMOS devices during ESD stress, the turn-on mechanisms of CMOS devices with different layout parameters under high current stress must be investigated. By using the TLP (transmission line pulsing) measurement technique [8], [9], turn-on characteristics of CMOS devices under high current stress can be analyzed. From the investigation of layout parameters on ESD robustness of CMOS device, the optimized parameters can be used to enhance the turn-on efficiency of CMOS device under ESD stress.

In this work, the dependences of layout parameters on ESD robustness of NMOS and PMOS devices are investigated through the fabricated testchips. To clearly understand the physical mechanisms on ESD current distribution through the device, the TLP measured data and energy band diagram are used to clearly explain the impacts from layout parameters.

II. Turn-On Mechanism of MOSFET Under ESD Stress

To illustrate turn-on behavior of gate-grounded MOSFET during ESD stress, one unit-finger structure of a multiple-finger NMOS device is shown in Fig. 3, where two parasitic diodes D_S and D_D can be found in the p–n junctions between source/drain and guardring. The parasitic lateral BJT with a base resistance (R_B) under the NMOS is also indicated in Fig. 3. When the $P+$ guardring, source, and gate of this NMOS are connected to ground, the parasitic diode D_D between drain and substrate is reverse biased under the positive ESD stress (V_{ESD}). Some reverse-biased current $(I_{\rm SDD})$ in Fig. 3 can flow into the substrate due to positive ESD zapping on the drain of NMOS. The reverse-biased current will increase base voltage of the parasitic lateral BJT. Due to the different distances from the base region to the $P+$ guardring, the base voltage of parasitic lateral BJT in the central region of finger-type NMOS is higher than that in the sided regions in Fig. 3. When the base voltage in the central region is increased up to trigger on the parasitic

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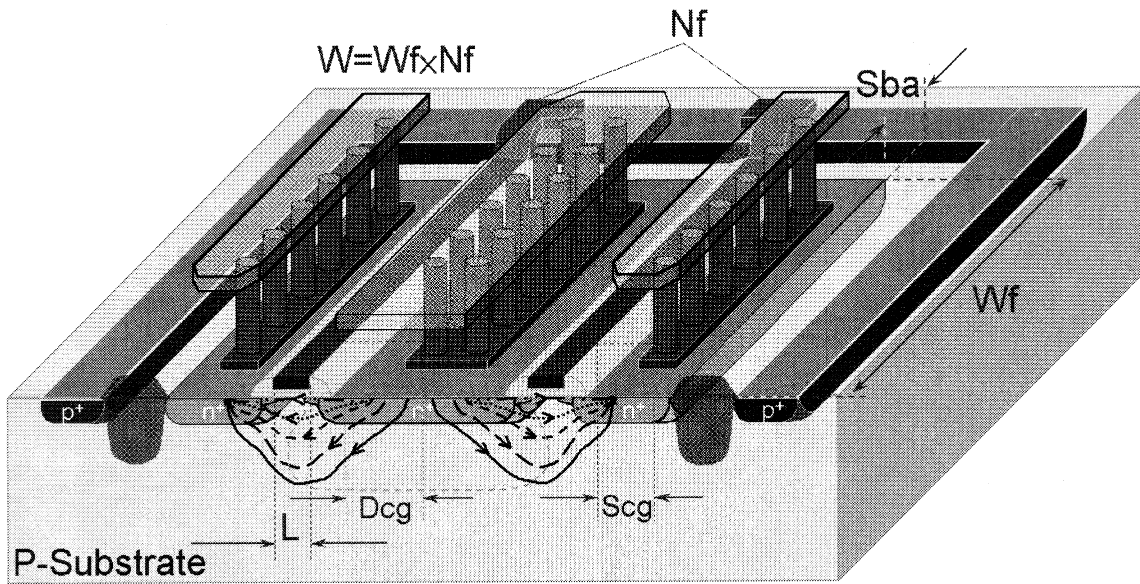

Fig. 2. 3-D structure of finger-type NMOS device with layout parameters.

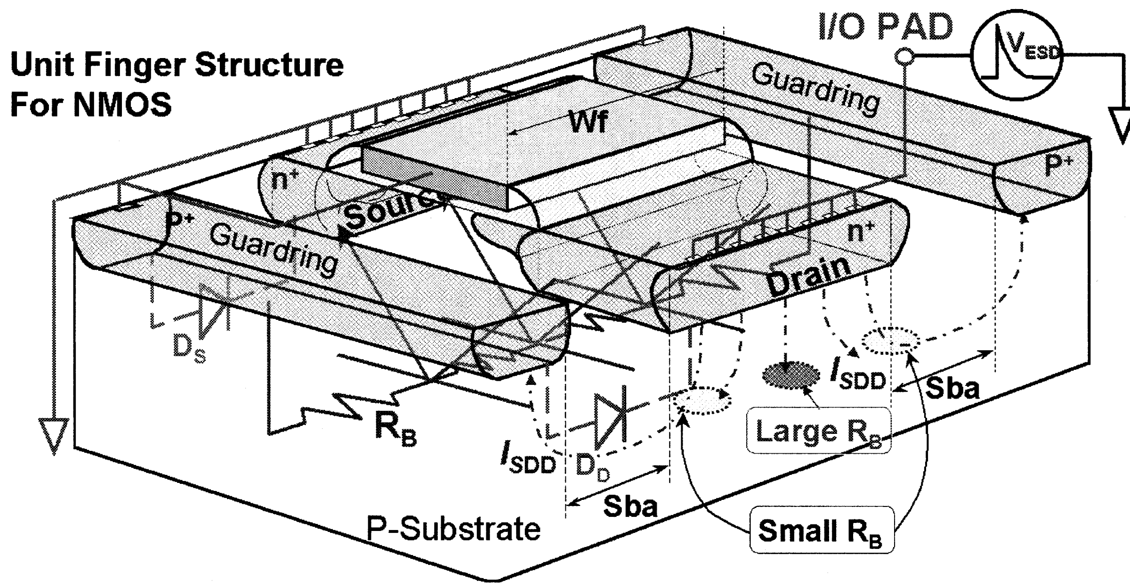

Fig. 3. Illustration of the parasitic devices and layout parameters in a unit-finger structure of a multiple-finger NMOS.

lateral BJT, the NMOS will enter into its snapback region. Under higher ESD stress, the local snapback turned-on region may be extended into more area along the finger structure of NMOS. But, the lateral BJT in the central region of NMOS is still first triggered into snapback to cause the nonuniform turn-on issue among the multiple fingers of NMOS device.

To understand turn-on behavior of the parasitic lateral BJT in NMOS, the energy band diagrams of half unit-finger NMOS device under ESD stress are analyzed in Fig. 4. To simply analyze the variation of energy band diagrams, only conduction band variations on the x–y and y–z planes along the half unit-finger structure are illustrated in Fig. 4. Because the voltage drop implies the negative variation of energy band, electrons will flow from source to drain. Because the reverse-biased current pulls down the energy band of base region in the parasitic lateral BJT, the depletion layer of reverse-biased junction can modulate the base width. The lower energy band barrier and shorter effective base width cause the fast turn on of the parasitic lateral BJT located at the central region of the NMOS. Therefore, during positive ESD stress, the multiple fingers of NMOS cannot be uniformly turned on. Only some regions of several fingers in the NMOS were turned on and, therefore, damaged by ESD.

To verify the turn-on uniformity, different current pulses are applied to the drain of a gate-grounded NMOS, which has a device dimension of $W/L = 300$ μm/0.5 μm in a 0.35-μm silicided CMOS process. The measurement setup is shown in Fig. 5(a), where the current pulse has different pulse heights. The corresponding current versus voltage (I–V) curve of the gate-grounded NMOS is drawn in Fig. 5(b). The EMMI photographs on the gate-grounded NMOS during the stresses of different current pulses are shown in Fig. 5(c)–(k) to observe its turn-on behavior. From the hot spots in Fig. 5(c)–(f), the re-

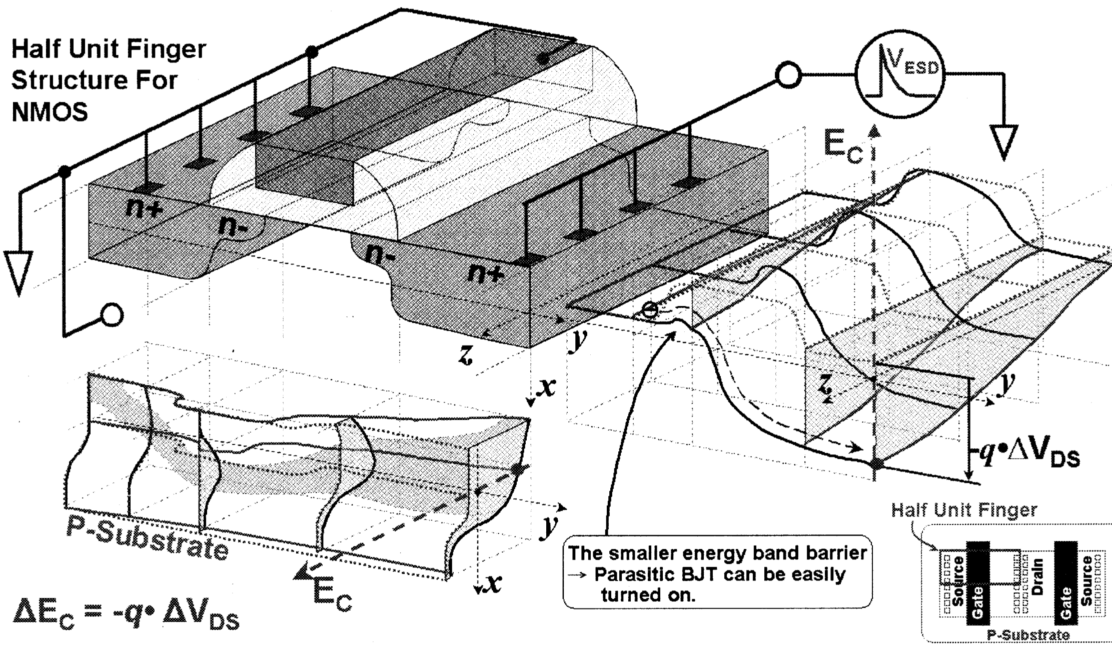

Fig. 4. Analysis of conduction energy band diagrams for a half unit-finger NMOS during positive ESD stress.

verse-biased breakdown current in the gate-grounded NMOS is initially flowing toward the guardring. When the base potential is increased up to trigger on the parasitic lateral BJT, the hot spots become to locate at the central regions of the finger-type NMOS, as those shown in Fig. 5(g)–(k). Because the short-channel NMOS has an obvious snapback I–V curve, as that shown in Fig. 6(a), the turned-on central fingers in Fig. 5(k) cause the ESD current mainly discharging through those fingers. If the turned-on region cannot be extended to full regions of all fingers before second breakdown occurs in NMOS, the turned-on central region in Fig. 5(k) will be burned out by the over-heating ESD current. This often causes a low ESD level, even if the multiple-finger NMOS has a large device dimension. On the contrary, the PMOS has no obvious snapback I–V curve, as that shown in Fig. 6(b). The PMOS eventually has good uniform turn-on efficiency.

Depending on the doping profile of impurities in channel region and some layout parameters of MOSFET, ESD voltage can lower the energy band of surface channel to turn on the parasitic lateral BJT. Generally, there are three current paths in MOSFET during ESD stress. The first path is the strong-inversion current along surface channel of MOSFET when some positive voltage is coupled to the gate [10]. This current path is shown as the Path1 in Fig. 7(a). The second path is formed by the drain-induced barrier lower in lightly doped drain (LDD) region nearby the surface channel, as the Path2 shown in Fig. 7(b), where the gate is biased at 0V. The third path is formed by the parasitic lateral BJT in MOSFET [11], but it is far away from the channel surface of MOSFET, which is shown as the Path3 in Fig. 7(c) with a 0-V gate bias. During positive ESD stress, a high voltage is applied on the drain of MOSFET to pull down the energy band of drain. The corresponding 2-D energy band diagrams on the $x - y$ plane of NMOS under different conditions are illustrated in Fig. 7(d) with a positive gate bias, in Fig. 7(e) with lowered energy band nearby LDD, and in Fig. 7(f) with lowered energy band far away from surface, respectively [11], [12]. Such electron flowing paths (Path1, Path2, and Path3) have been clearly indicated in those band diagrams. To further understand such turn-on paths, one-dimension energy band diagrams along the A-A' lines of Fig. 7(a)–(c) in the x axis direction are drawn in Fig. 7(g)–(i), respectively. High electric field across the gate oxide can be found in Fig. 7(g) and (h), but it isn't found in Fig. 7(i) during ESD stress. With different current paths, the NMOS during ESD stress may be damaged by different failure mechanisms. However, the layout parameters of MOSFET can affect the current paths along the MOSFET during ESD stress. Therefore, the ESD robustness of MOSFET can be further improved by the optimized layout parameters.

III. Layout Dependence

To design robust ESD protection devices, layout spacings are the major considerations for finger-type CMOS devices. The main layout parameters to affect ESD robustness of the ESD protection devices are the channel width (W), the channel length (L), the clearance from contact to poly-gate edge at drain (Dcg) and source (Scg) regions, the spacing from the drain diffusion to the guardring diffusion (Sba), and the finger width (Wf) of each unit finger, which have been indicated in Fig. 2 with the 3-D device structure. When the dependences of ESD current paths on the layout parameters are well understood, ESD protection devices can be optimized to perform high ESD robustness.

The layout factors to affect ESD robustness of CMOS devices have been practically investigated by the fabricated testchips in a 0.35-μm silicided CMOS process. The ZapMaster ESD tester, produced by Keytek Instrument Corp., is used to measure HBM ESD level of the fabricated testchips. The failure criterion is generally defined at 1-μA leakage current under 1.1 times $V_{\rm DD}$ bias, when the device is kept in its off state. To investigate the snapback behavior of device during high ESD stress, transmis-

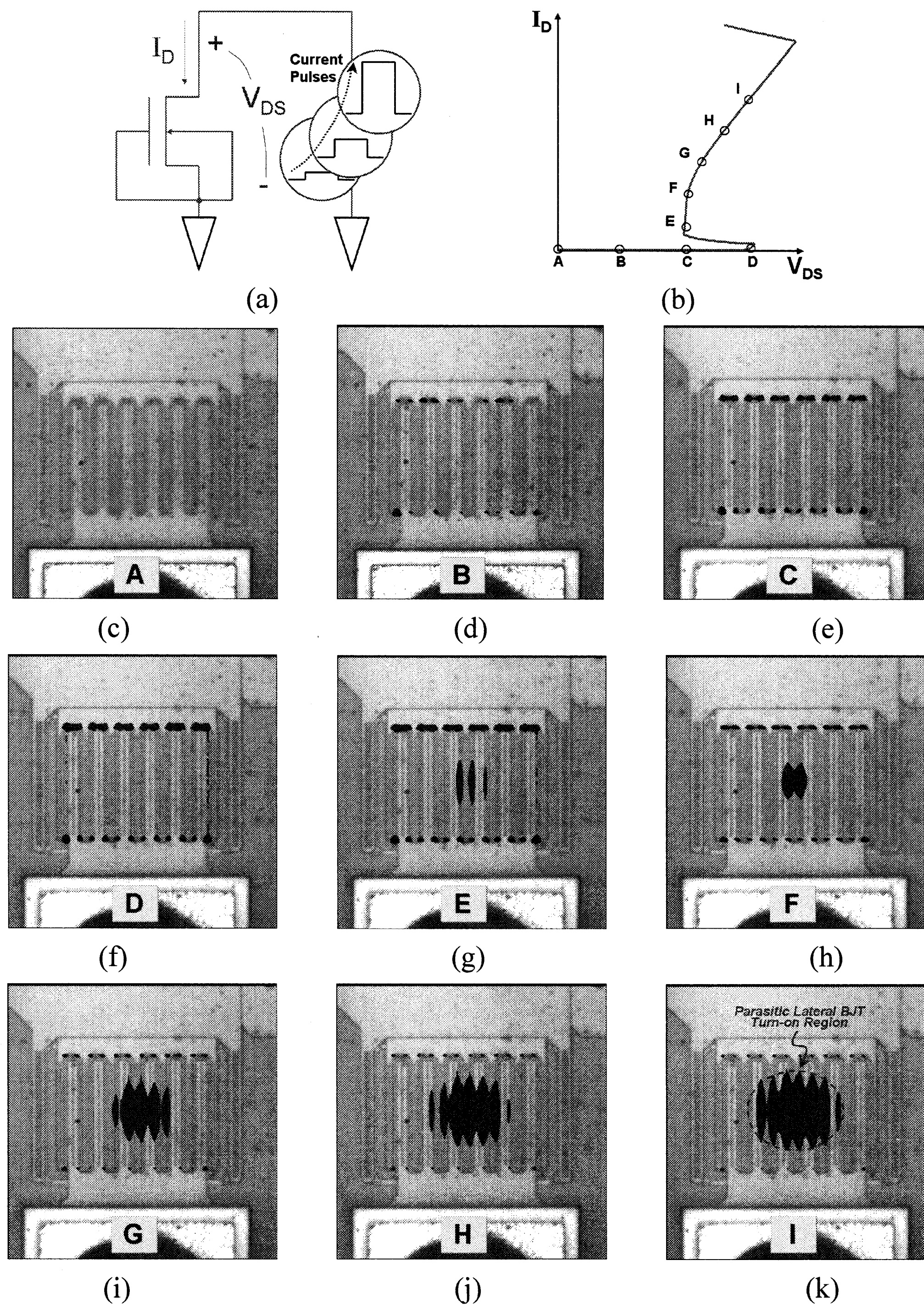

Fig. 5. EMMI photographs on a gate-ground NMOS ($W/L = 300$ μm/0.5 μm) to observe its turn-on behavior under the stress of different pulsed currents. (a) Measurement setup. (b) Corresponding I–V curve of a gate-grounded NMOS. (c)–(f) Hot spots in the gate-grounded NMOS before it enters into snapback region. (g)–(k) Hot spots in the gate-grounded NMOS after it enters into snapback region.

sion line pulsing (TLP) technique has been widely used to measure the second breakdown characteristics of devices [8], [9]. The TLP measured results are also shown and analyzed in the following.

A. Channel Width Dependence and Silicide Effect

To discharge more ESD current, the channel widths of ESD protection devices are often designed with larger dimension. However, if nonuniform turn-on effect is considered, the MOSFET with a larger channel width cannot sustain high ESD level as expectation. The NMOS and PMOS devices with different W have been fabricated in a 0.35-μm silicided CMOS process. Each unit-Wf of the NMOS and PMOS devices in this investigation is kept as 50 μm. The NMOS and PMOS devices with or without the salicide-blocking layer to block the silicided diffusion on the drain region are also drawn in the testchips to investigate their ESD levels. For both NMOS and PMOS devices in this investigation, the channel length (L), the

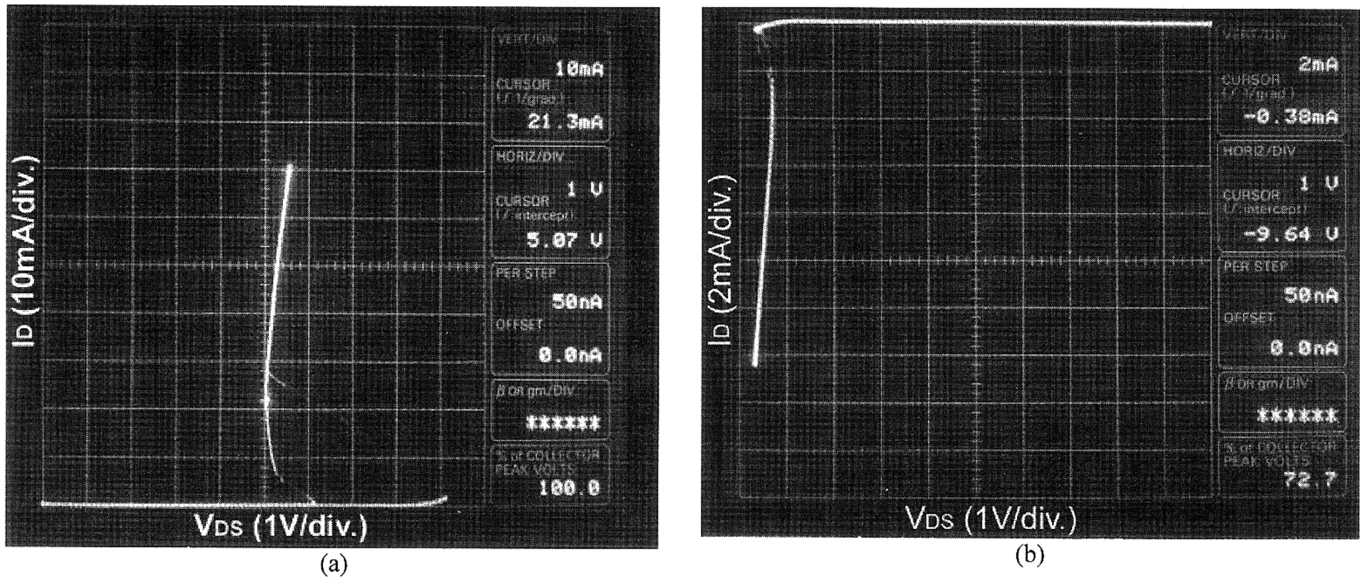

Fig. 6. Measured snapback I–V curves of (a) NMOS, and (b) PMOS, with a channel length of 0.35 μm.

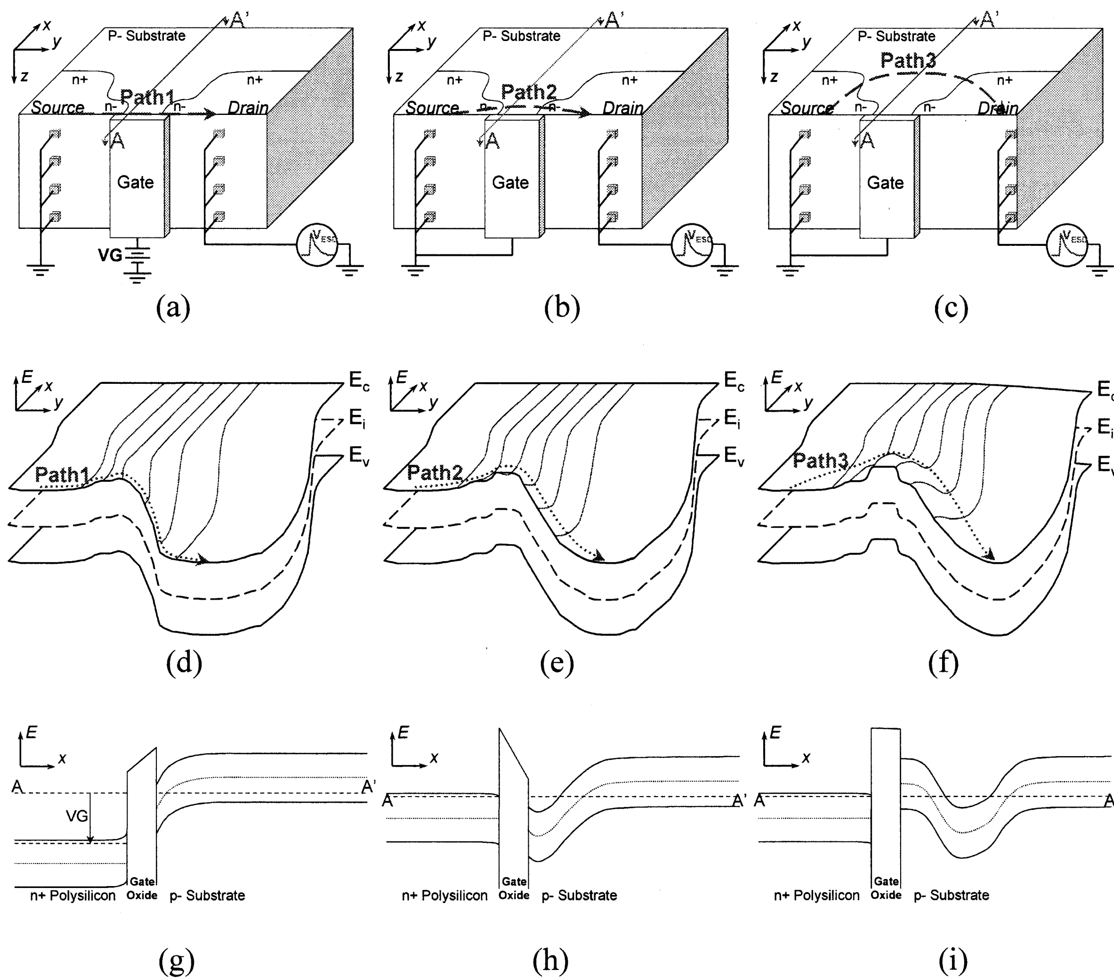

Fig. 7. Illustrations of energy band diagram for a nonsilicided NMOS with different stress conditions. (a)–(c) show devices under different biases. (d)–(f) show 2-D band diagrams of NMOS in the corresponding conditions of (a)–(c), respectively. (g)–(i) show the x axis band diagrams along the line A-A' of NMOS in (a)–(c), respectively. A gate voltage of VG is applied on the gate of NMOS in (a).

clearance from the drain contact to polygate edge (Dcg), the clearance from the source contact to polygate edge (Scg), and the spacing from the drain diffusion to the guardring diffusion (Sba) are kept at 0.8, 3, 1, and 4 μm, respectively.

The transmission line pulsing generator (TLPG) in Fig. 8(a) is used to measure the second breakdown current and the snapback turn-on resistance of NMOS. The corresponding circuit for TLPG measurement with a pulsewidth of 100 ns on a gate-grounded NMOS is shown in Fig. 8(b). The TLP-measured I–V characteristics and the corresponding leakage current of NMOS with $W/L = 200\ \mu$m/0.8 μm are shown in Fig. 8(c). The second breakdown current is indicated as It_2 in Fig. 8(c). The snapback turn-on resistance is defined as the voltage variation over current variation near to the second breakdown point in the TLP-measured I–V curve. The snapback turn-on resistance can be expressed as

$$R_{\text{device}} \equiv \frac{\partial V_{\text{DS}}}{\partial I_D}. \tag{1}$$

From the TLP-measured results, the relation between second breakdown current (It_2) and HBM ESD level (V_{ESD}) can be approximated as [13], [14]

$$\text{HBM } V_{ESD} \approx (1500 + R_{\text{device}}) \times \text{It}_2. \tag{2}$$

The snapback turn-on resistances of finger-type NMOS devices with different channel widths, but with the same unit-finger width and channel length, are shown in Fig. 8(d). For an NMOS with channel width of 50 μm, the turn-on resistance R_{50} in Fig. 8(d) is 6.83 Ω. If the NMOS with longer channel width can be uniformly turned on, the dependence of snapback turn-on resistance on the channel width can be shown by the ideal curve in Fig. 8(d), which is drawn with the dashed line. In this ideal case, the snapback turn-on resistance of NMOS with channel width of 600 μm should be only 0.57 Ω. But, the experimental result on the snapback turn-on resistance $R_{600} (= 1.64\ \Omega)$ of NMOS with 600-μm channel width in Fig. 8(d) is far from the ideal resistance. This implies that the finger-type gate-grounded NMOS device with a longer channel width cannot be uniformly turned on during ESD stress.

The relations between the device W and the HBM ESD level of NMOS and PMOS devices in a 0.35-μm CMOS process are investigated in Fig. 9(a) and (b), respectively. In Fig. 9(a), the NMOS is stressed under the positive-to-V_{SS} ESD stress, whereas the PMOS is stressed under the negative-to-V_{DD} ESD stress in Fig. 9(b). In Fig. 9(a), the HBM ESD level of the NMOS device is increased while the device channel width is increased. If the device channel width is increased, more fingers are drawn and connected in parallel to form the large-dimensional NMOS device. The ESD robustness of such large-dimensional device may be increased while the device channel width is increased. But, in Fig. 9(a), the ESD level (3.4 kV) of the silicide-blocking NMOS with a channel width of 600 μm is less than that (3.5kV) of the NMOS with a channel width of 400 μm. This is due to the nonuniform turn-on issue among the multiple fingers of a large-dimensional device. In the finger-type NMOS, if the base current can not uniformly trigger on the distributed parasitic lateral BJTs along the NMOS, the ESD current will be concentrated in some local area to cause the nonuniform turn-on phenomena in the NMOS under ESD stress.

In Fig. 9(b), the HBM ESD levels of the PMOS with or without silicided diffusion are both increased as the device channel width is increased. The ESD level of the silicided PMOS with a channel width of 400 μm is around -2.45 kV, but that of the silicide-blocking PMOS with the same device dimension and layout style is -4.45 kV. This verifies the effectiveness of the silicide-blocking process used to improve ESD level in deep-submicron CMOS technologies. The continue increase of ESD level, when the channel width of PMOS has been increased, is due to the less snapback characteristics of PMOS. The snapback characteristics of a PMOS have been shown in Fig. 6(b). As comparing the I–V curves between Fig. 6(a) and (b), the PMOS with less snapback characteristics leads to a more turn-on uniformity among its multiple fingers. Therefore, it has a continue increase on its ESD level, when the channel width of PMOS is increased.

In Fig. 9(b), the NMOS with silicide-blocking process can sustain much higher ESD level than that with the silicided diffusion [15]. NMOS devices with or without silicide-blocking mask have different turn-on resistances in the TLP-measured I–V curves of Fig. 10. The turn-on resistance of the silicided NMOS with $W/L = 200\ \mu$m/0.8 μm is only 2.45 Ω, but that of the silicide-blocking NMOS with the same device dimension and layout style is 4.06 Ω. However, the It_2 of silicide-blocking NMOS is 103% higher than that of the silicided NMOS.

To explain the degradation on ESD robustness of silicided NMOS device, the energy band diagrams of NMOS with or without the silicided diffusion are compared in Fig. 11(a) and (b), respectively. A positive ESD stress is applied to the drain of NMOS, whereas the gate, source, and bulk of NMOS are connected to ground. The energy band diagrams are analyzed along both the lines A-A' and B-B' in Fig. 11(a) with silicided diffusion, and in Fig. 11(b) without silicided diffusion. The E_C and E_{V} in Fig. 11 are the conduction and valance energy levels, respectively. In Fig. 11(b), the $V_{\text{RD}}(V_{\text{RS}})$ is the voltage drop on the drain (source) diffusion, and the R_D (R_S) is the effective sheet resistance of drain (source) diffusion. The V_{act} is defined as the active turn-on voltage of parasitic lateral BJT in the NMOS. The regions G and S in Fig. 11 are defined as the effective current discharging regions through the NMOS under positive ESD stress. From Fig. 11(a), the drain voltage can pull down the band diagram at the drain silicided diffusion because of the silicided diffusion with a low resistance and close to the LDD structure. The major voltage drop of drain bias (V_{DS}) is located along the surface channel of MOSFET. Therefore, the energy band on the surface channel will be lowered. This effect of drain-induced barrier lowering can enhance the channel current forming in the NMOS device. Major ESD current will flow into the turned-on region G in Fig. 11(a), which is very close to the interface between gate oxide and surface channel of NMOS. With a shallower current path, ESD current can easily damage the surface channel and the gate oxide of NMOS. But, a silicide-blocking diffusion can reduce the turn-on probability of Path2 in Fig. 7. The energy band diagram in Fig. 11(b) can explain this phenomenon. The drain p–n junction near the surface channel is connected in series with a larger sheet resistance in the silicide-blocking NMOS, but the p–n junction at the bottom of drain diffusion has a smaller sheet resistance (R_D).

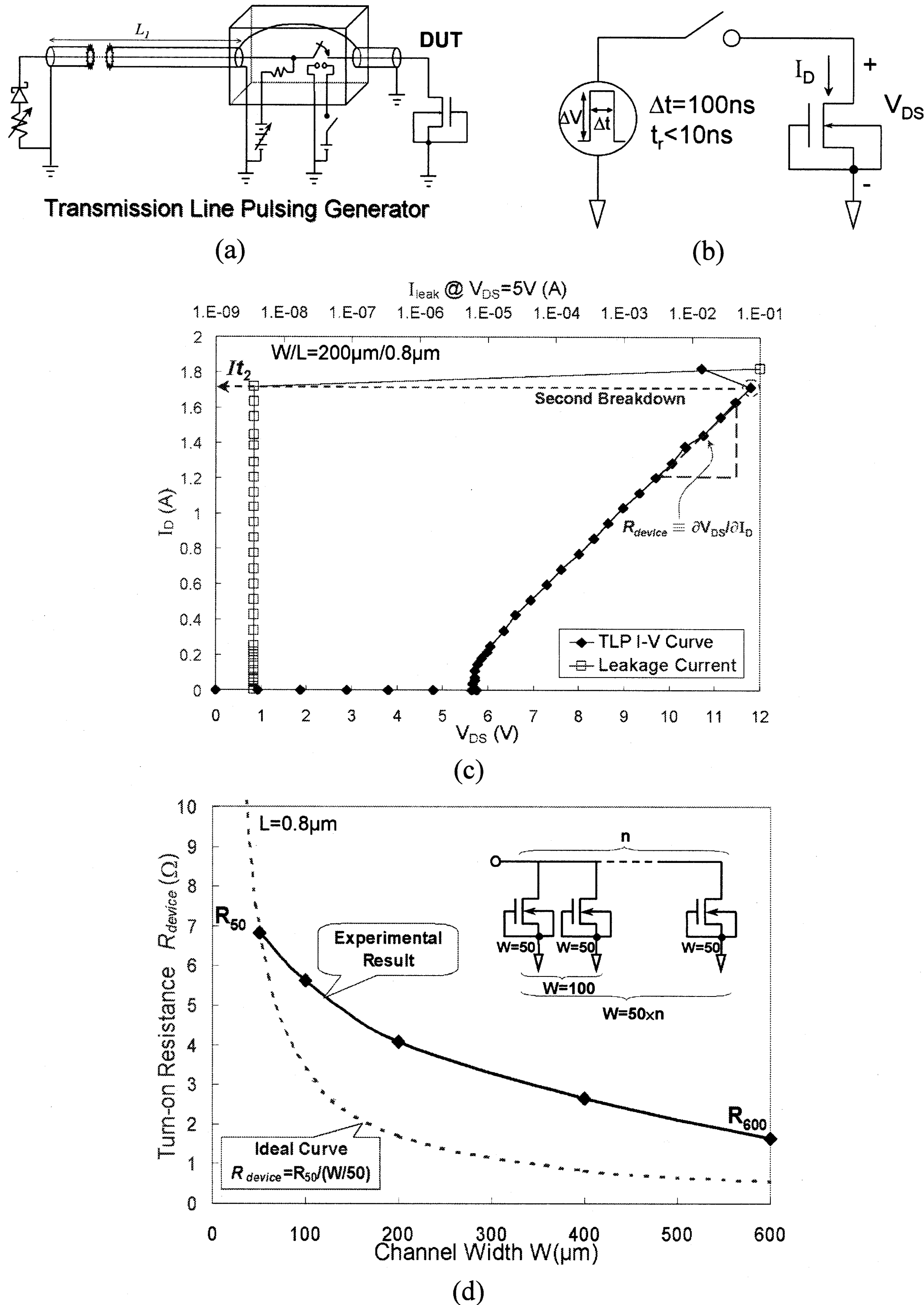

Fig. 8. (a) Illustration of transmission line pulsing generator (TLPG). (b) Corresponding circuit for TLPG measurement on a gate-grounded NMOS. (c) Measured I–V characteristics and leakage currents of NMOS by TLP with a pulsewidth of 100 ns. (d) Turn-on resistances of finger-type NMOS devices with different channel widths, but with the same unit-finger width and channel length.

The sheet resistance of silicide-blocking drain diffusion can reduce the voltage drop on the channel surface. So, the ESD current is discharged through the parasitic lateral BJT, which is far away from the channel surface. The silicide-blocking drain diffusion can avoid ESD overstress on the surface channel or the gate oxide, therefore the silicide-blocking NMOS has a much higher ESD robustness.

B. Channel Length Dependence

The TLP-measured I–V curves of gate-grounded NMOS devices with different channel lengths ($L = 0.35$ μm, 0.8 μm, 1.2 μm, and 1.5 μm) are compared in Fig. 12. The layout style and other parameters are all kept the same ($W = 200$ μm, Wf $= 50$ μm, Dcg $= 3$ μm, Scg $= 1$ μm, and Sba $= 4$ μm),

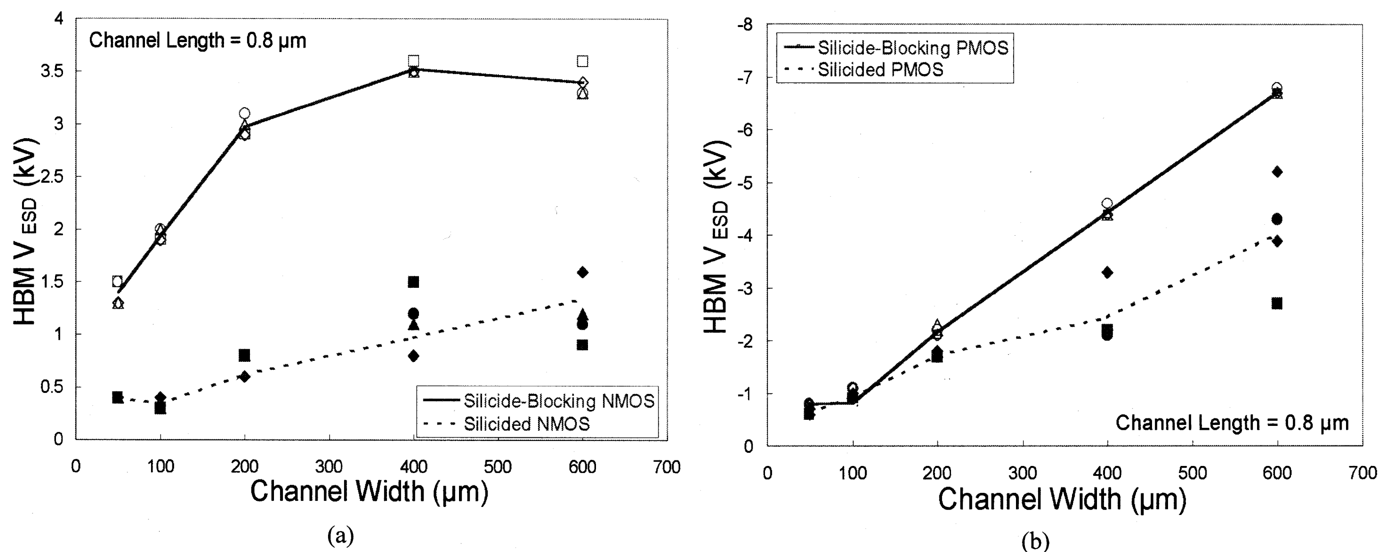

Fig. 9. Dependence of HBM ESD level on the channel width of (a) NMOS, and (b) PMOS, with or without silicided diffusion.

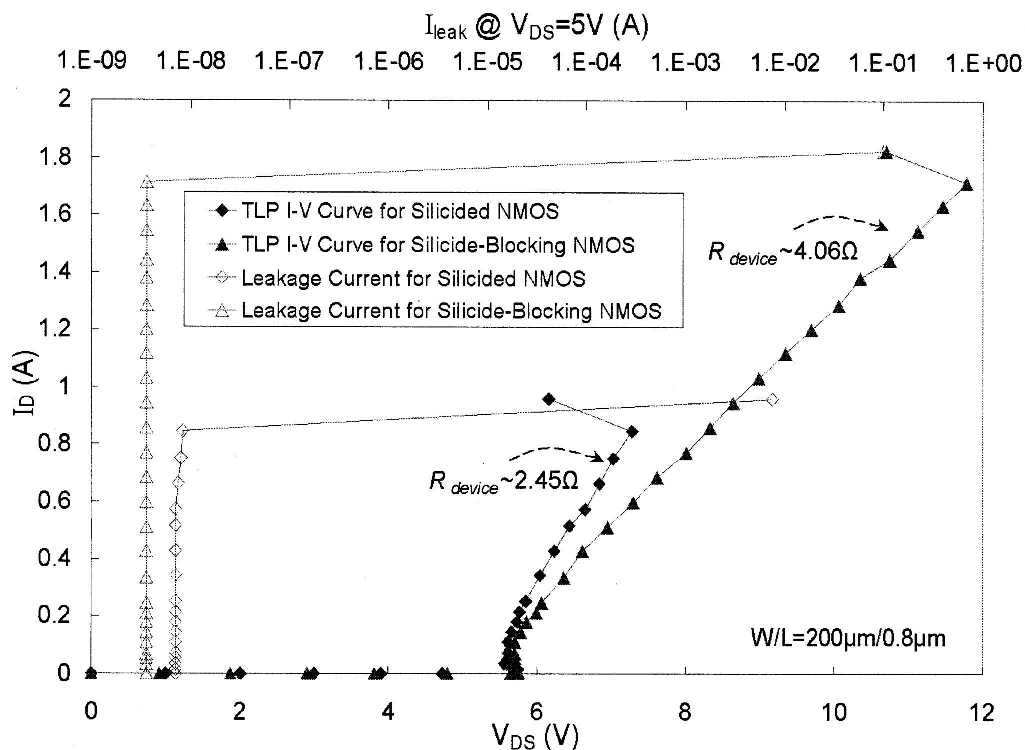

Fig. 10. TLP measured I–V curves of NMOS devices with or without silicided diffusion, but with the same device dimension of $W/L = 200$ μm/0.8 μm.

but only the channel length is different under this investigation. Both NMOS and PMOS are fabricated with the silicide-blocking layer to block silicided diffusion on both drain and source regions. Generally, the Scg parameter is drawn with a small clearance. During positive ESD stress, the resistance of R_S can be considered as a small constant value. To simplify the analysis, the sum of R_D and R_S is defined as $R_{\rm DS}$. Therefore, the snapback turn-on resistance $R_{\rm device}$ can be re-written as

$$R_{\rm device} = {\rm R_{DS}} + \partial \frac{\rm V_{act}}{\partial {\rm I_D}} \equiv {\rm R_{DS}} + {\rm R_{BJT}} \tag{3}$$

where the effective turn-on resistance $R_{\rm BJT}$ of parasitic lateral BJT is defined as $\partial V_{\rm act}/\partial I_D$. The $V_{\rm act}$ is the active turn-on voltage of parasitic lateral BJT in the NMOS. The current I_D is a function of effective base width (W_B), turn-on area (A_D and A_S) in drain/source edge, voltage drop between base and emitter ($V_{\rm BE}$), and voltage drop between base and collector ($V_{\rm BC}$) in the parasitic lateral BJT [16]. It can be further expressed as

$$\begin{aligned} I_D =& q A_s n_i^2 \left[\frac{D_B}{L_B N_B}\left(\frac{L_B}{W_B}\right)\right]\left(e^{q^{V_{\rm BE}}/{\rm kT}} - 1\right) \\ &- q A_D n_i^2 \left[\frac{D_C}{L_C N_C} + \frac{D_B}{L_B N_B}\left(\frac{L_B}{W_B} + \frac{W_B}{2L_B}\right)\right] \\ &\times \left(e^{-q^{V_{\rm CB}/{\rm kT}}} - 1\right). \end{aligned} \tag{4}$$

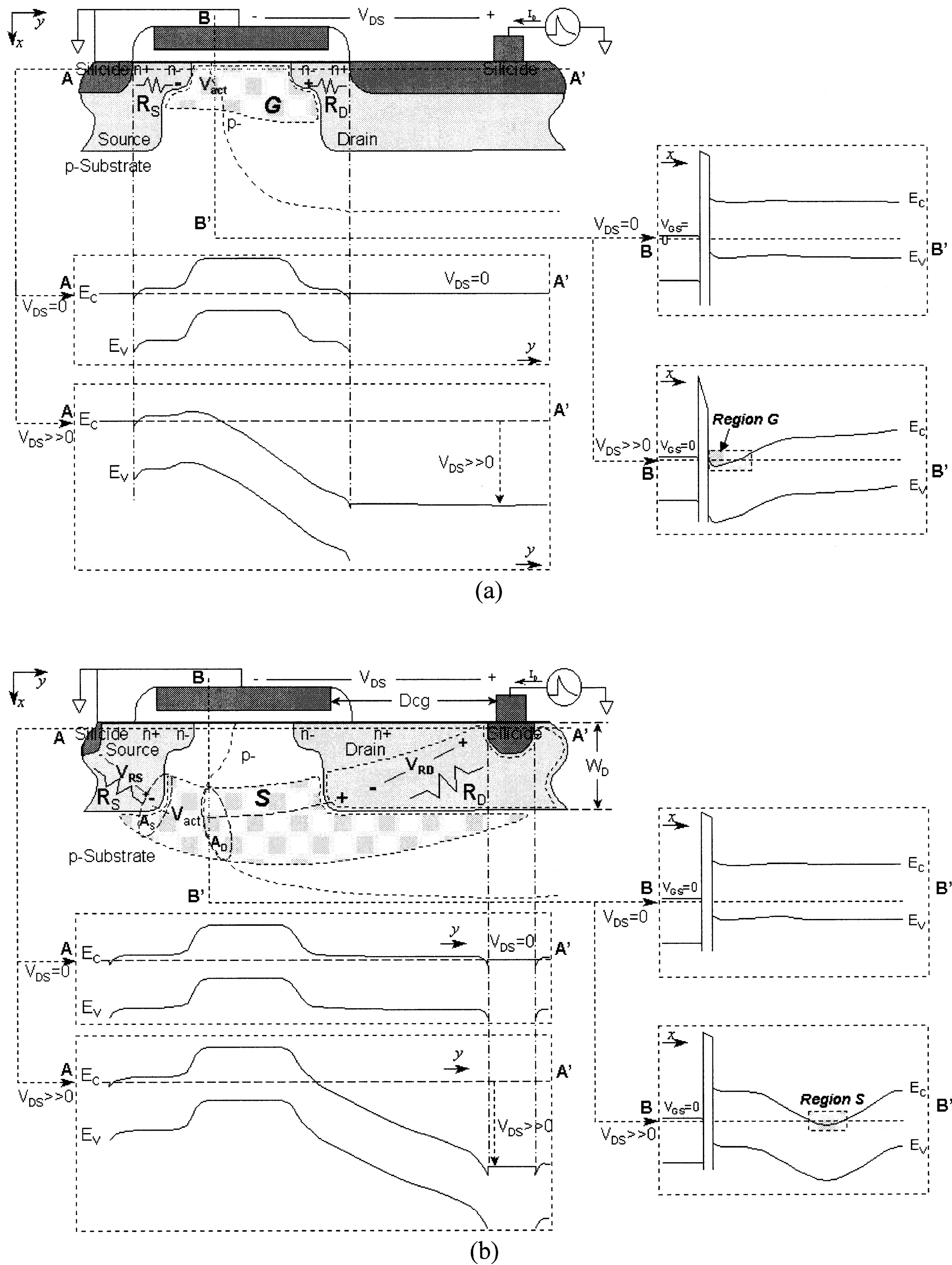

Fig. 11. Illustration of the variation on energy band of gate-grounded NMOS (a) with and (b) without silicided diffusion.

The turn-on areas of A_D and A_S imply two effective turn-on areas in the base region of parasitic lateral BJT among multiple fingers of NMOS. The active turn-on voltage $V_{\rm act}$ between collector and emitter of parasitic lateral BJT is the sum of base-to-emitter voltage $V_{\rm BE}$ and collector-to-base voltage $V_{\rm CB}$. Generally, $V_{\rm BE}$ is larger than kT/q, and $V_{\rm CB}$ is a large reversed bias on the p–n junction of drain diffusion during positive ESD stress. The effective base width (W_B) is a function of NMOS's channel length (L) and depletion width (W'_B) of the reverse-biased p–n junction between the drain diffusion and the bulk of NMOS. It

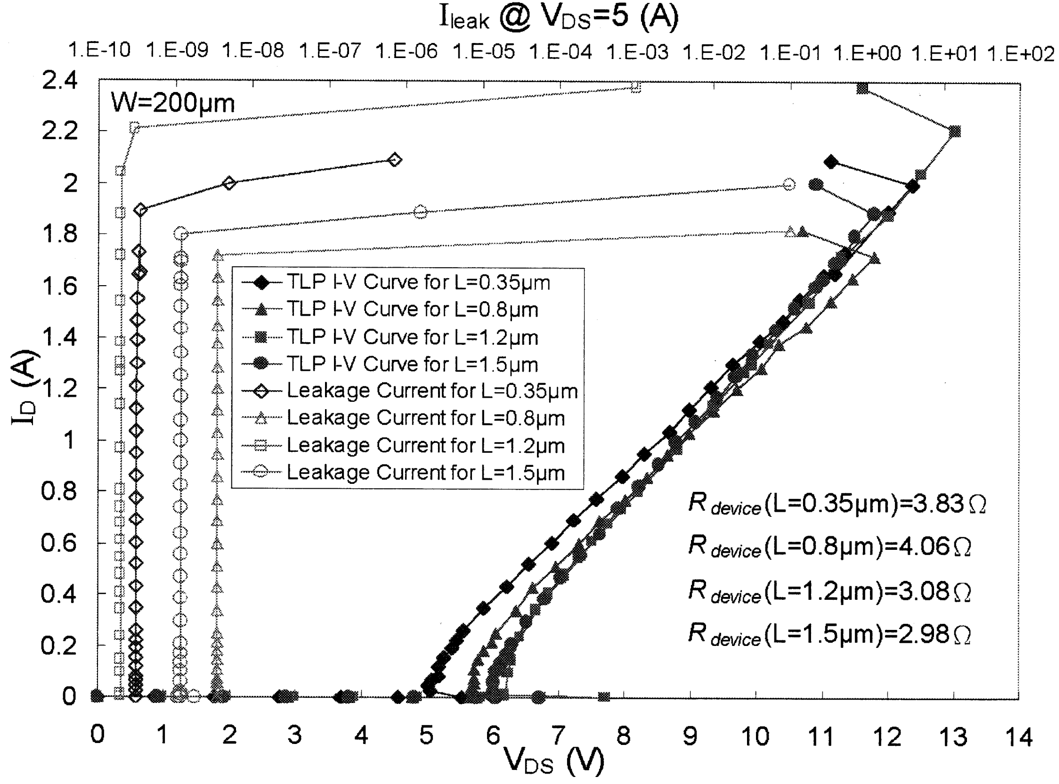

Fig. 12. TLP measured results for gate-grounded NMOS devices with different channel lengths (L =0.35, 0.8, 1.2, and 1.5 μm).

can be expressed as

$$L \approx W_B + W_B'. \tag{5}$$

To simply analyze the geometric effect, the base concentration of N_B in (4) is assumed as a constant distribution in the bulk of NMOS.

To further analyze the geometric layout effect in (4), two assumptions will be discussed in the following analysis. First, the turn-on areas (A_S and A_D) of parasitic lateral BJT are further assumed as constant values in the following discussion. Under the same ESD stress, when the L of NMOS is increased, $V_{\rm BE}$ or $V_{\rm CB}$ must be increased to keep the I_D as a constant current in (4). So, $V_{\rm act}$ must be increased when the L of NMOS is increased in this assumption. From (3) and (4), the effective turn-on resistance $(R_{\rm BJT})$ of parasitic lateral BJT can be approximated as

$$\begin{aligned} R_{\rm BJT} \approx & \frac{kT}{q^2 A_S n_i^2}\left[\frac{L_B N_B}{D_B}\left(\frac{W_B}{L_B}\right)\right] e^{-qV_{\rm BE}/{\rm kT}} \\ &+ \frac{kT}{q^2 A_D n_i^2}\left[\frac{D_C}{L_C N_C} + \frac{D_B}{L_B N_B}\left(\frac{L_B}{W_B}\right)\right]^{-1} \\ &\times e^{q^{V_{\rm CB}/{\rm kT}}}. \end{aligned} \tag{6}$$

From aforementioned discussion, NMOS with a longer channel length has a larger $R_{\rm BJT}$ under the same ESD stress. If the effective diffusion sheet resistances $(R_{\rm DS})$ of NMOS with different channel lengths were the same, the NMOS with a longer channel length should have a larger turn-on resistance under ESD stress.

But from the experimental results of Fig. 12, the NMOS with channel length of 1.2 μm has a lower turn-on resistance of 3.08 Ω than that with a channel length of 0.8-μm, which has a 4.06-Ω turn-on resistance. So, the NMOS with channel length of 1.2 μm must have a very low sheet resistance. The effective sheet resistance in NMOS is decreased, when the channel length of NMOS is increased under the same ESD stress, to have a lower turn-on resistance $(R_{\rm device})$ in the TLP-measured results of Fig. 12. With this assumption of fixed turn-on area, the variation of channel length from shorter to longer in MOSFET can cause the moving of the turned-on region in the parasitic lateral BJT from the sideward to the bottom of drain diffusion in the MOSFET device structure.

On another assumption, if the turn-on areas of A_S and A_D are not fixed at some local regions, the $V_{\rm BE}$ and $|V_{\rm BC}|$ can be fixed in certain voltages for NMOS devices with different channel lengths. While $V_{\rm BE}$ and $|V_{\rm BC}|$ are fixed, W_B' is kept as a constant value for MOSFET devices with different channel lengths. To sustain the same ESD stress in the turned-on parasitic lateral BJTs with different effective base widths, the turn-on areas of A_S and A_D must be increased when the channel length of MOSFET is increased. The ratios of A_S/W_B and A_D/W_B must be kept at constant values to limit the I_D as a constant current in (4). Then, the $R_{\rm BJT}$ will be a constant resistance from (6) in this assumption. Therefore, the larger turn-on areas can reduce the effective sheet resistances in the drain/source regions of MOSFET. This can explain why the gate-grounded NMOS with a long channel length has a lower turn-on resistance measured by TLP in Fig. 12. In the actual case, the turn-on mechanism is operated between these two assumptions. The turn-on areas of

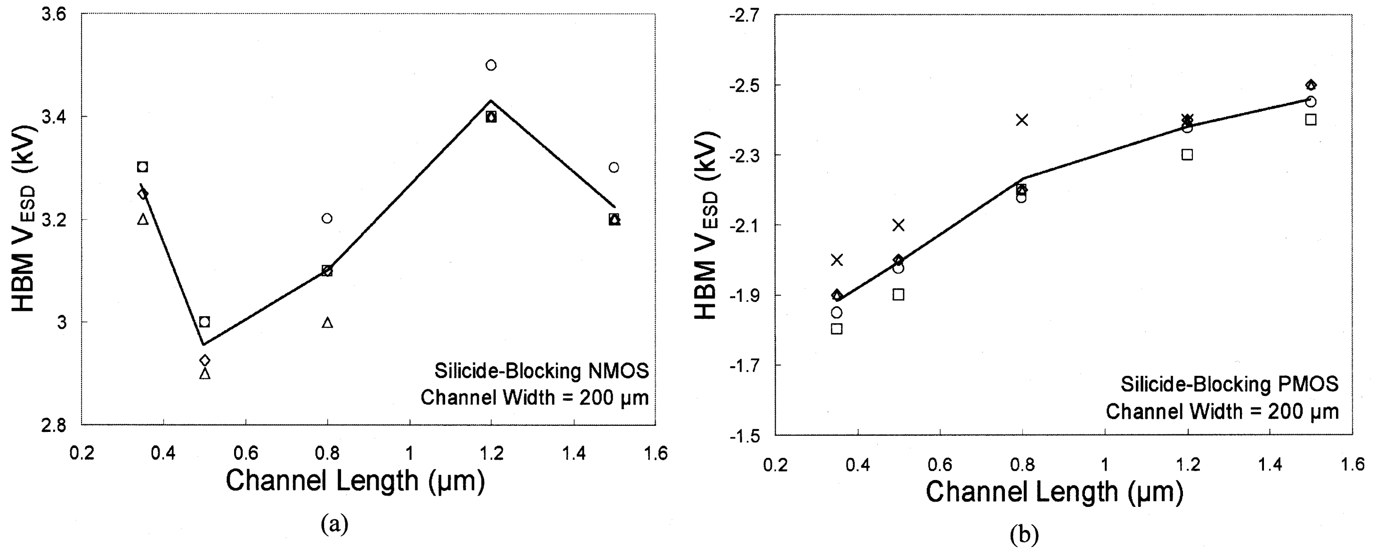

Fig. 13. Dependence of HBM ESD level on the channel length of (a) NMOS, and (b) PMOS, with a fixed W of 200 μm.

A_S, A_D and $R_{\rm BJT}$ can be increased, and the turned-on region can be moved or extended from the sideward to the bottom of drain/source diffusions in MOSFET, when the L of MOSFET with LDD structure is increased.

The dependences of L on the HBM ESD level of NMOS and PMOS devices in a 0.35-μm CMOS process are shown in Figs. 13(a) and (b), respectively. From the experimental results shown in Fig. 13(a), the HBM ESD level of NMOS with a minimum channel length of 0.35 μm is 3.25 kV, whereas that of NMOS with a channel length of 0.5 (0.8) μm is 2.9 (3.1) kV. When an NMOS has a shorter enough channel length, the efficiency and performance of the parasitic lateral BJT in the NMOS device is significantly improved. Therefore, it can sustain much higher ESD level than the NMOS with a medium channel length about 0.5 μm. On the contrary, the PMOS with a shorter channel length has a lower ESD level, as shown in Fig. 13(b). Even if the PMOS has a minimum channel length of 0.35 μm, its HBM ESD level is only -1.85 kV because the turn-on efficiency of lateral p–n–p BJT in PMOS is not improved.

Because the LDD structures of short channel length device induce a shorter effective base width nearby the channel surface of NMOS, the energy band of region G, as similar to that shown in Fig. 11(a), can be lowered by the drain-induced barrier lowing in the short channel length device. Therefore, the short channel length device has an extended current path to discharge ESD current. A voltage drop is established in the region S, as similar to that shown in Fig. 11(b), to trigger on the parasitic lateral BJT, and another channel current is also formed in the region G. The region G and S can be merged together to supply more area for heat dissipation under ESD stress. Owing to this phenomenon, NMOS device with shorter channel length can sustain higher ESD stress as the experimental data verified in Fig. 13(a). To avoid the hot carrier effect, the doping styles of the region G and S in NMOS device are different from that of PMOS device in the 0.35-μm CMOS process. There is no extended area in the region G to sustain more effective area for heat dissipation in PMOS device with shorter channel length. From this experimental investigation, the selection on the channel length of NMOS and PMOS for ESD protection is quite different in such a 0.35-μm silicided CMOS process.

C. Drain/Source Contact to Poly-Gate Edge

Because the Dcg parameter can cause the capacitance variation of the reverse-biased drain diffusion junction in NMOS under positive ESD stress, NMOS with different Dcg parameters will have different voltage drop $(\Delta V_{\rm CB})$ between the drain diffusion and the bulk of NMOS. When the Dcg parameter is increased, $\Delta V_{\rm CB}$ can be decreased because of the fixed total stress charge. To discharge the same ESD stress in the MOSFET with different Dcg parameters, a smaller $\Delta V_{\rm CB}$ will cause a larger turn-on area A_D (A_S) in the parasitic lateral BJT [17].

To investigate the I–V characteristics of the gate-grounded NMOS devices with different Dcg parameters during ESD stress, the TLP-measured I–V curves of NMOS devices with different Dcg parameters of 1.5 μm, 3 μm, and 5 μm are shown in Fig. 14. In silicide-blocking NMOS devices, all of the layout style and other parameters are kept the same ($W = 200$ μm, Wf $= 50$ μm, $L = 0.8$ μm, Scg $= 1$ μm, and Sba $= 4$ μm). From the previous discussion, the larger Dcg parameter can cause larger turn-on area in the parasitic lateral BJT of NMOS under ESD stress. Although a device with larger clearance of Dcg has larger turn-on area in NMOS, the device with larger Dcg parameter may have a larger sheet resistance in NMOS. A simple model of sheet resistance in the drain diffusion of NMOS can be calculated from Fig. 11(b), which is approximated as

$$R_D \approx \rho \frac{\sqrt{Dcg^2 + W_D^2}}{A_D}. \tag{7}$$

When the variation of Dcg parameter is larger than the variation of effective turn-on area in the parasitic lateral BJT, the NMOS with larger Dcg parameter has a larger sheet resistance under ESD stress. On the other hand, because the larger Dcg parameter can cause larger turn-on area A_D and less reverse-bi-

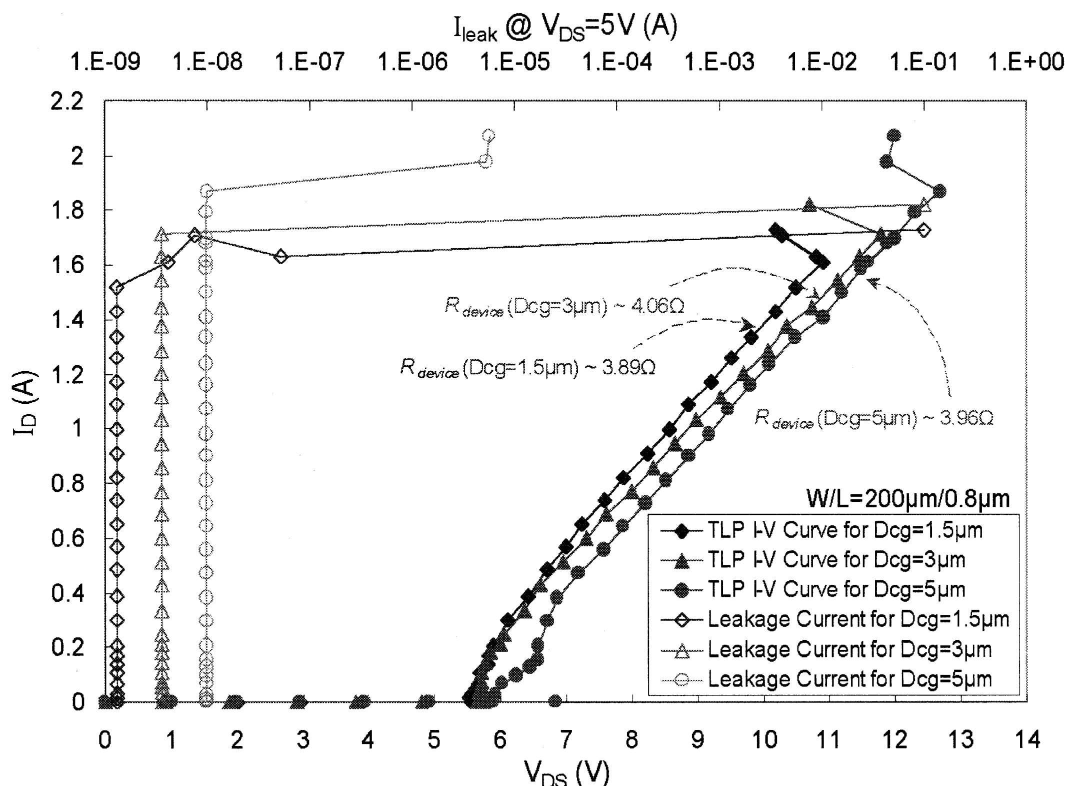

Fig. 14. TLP measured I–V curves for NMOS devices with different Dcg parameters (Dcg $= 1.5$ μm, 3 μm, and 5 μm).

ased voltage drop of $V_{\rm CB}$ in the parasitic lateral BJT under ESD stress, the effective turn-on resistance ($R_{\rm BJT}$) of parasitic lateral BJT can be decreased by the larger Dcg parameter. So, the total turn-on resistances ($R_{\rm device}$) of NMOS with different Dcg parameters are nearly the same, as that shown in Fig. 14. The turn-on resistances of the NMOS devices with Dcg of 1.5 μm, 3 μm, and 5 μm are 3.89 Ω, 4.06 Ω, and 3.96 Ω, respectively. But, the NMOS with larger Dcg parameter can sustain the higher ESD stress owing to the larger turn-on area A_D.

The dependence of clearance from the drain/source contact to the poly-gate edge (Dcg and Scg) on HBM ESD level of NMOS and PMOS devices is shown in Fig. 15(a) and (b), respectively. In this investigation, all of the layout style and other spacings are kept the same ($W = 200$ μm, Wf $= 50$ μm, $L = 0.8$ μm, and Sba $= 4$ μm), but only the Dcg and Scg are varied from 1 to 8 μm in the testchips. Both NMOS and PMOS are fabricated with the salicide-blocking layer to block the silicided diffusion on the drain and source regions. From the experimental results, the clearance variation on Scg from 1 to 5 μm at the source region (with a fixed Dcg of 3 μm at the drain region) only leads to slight variation on ESD level from 3.3 kV to 3.6 kV (-2.1 kV to -2.2 kV) in the salicide-blocking NMOS (PMOS) device. But, the clearance variation on Dcg from 1.5 to 8 μm at the drain region (with a fixed Scg of 1 μm at the source region) can cause significantly improvement on ESD level from 2.4 kV to 3.4 kV (-1.7 kV to -3.4 kV) in the silicide-blocking NMOS (PMOS) device. Therefore, the clearance of Dcg in both PMOS and NMOS devices for ESD protection is suggested greater than 3 μm to achieve better ESD robustness in this 0.35-μm CMOS process.

The shorter clearance of Dcg can induce a smaller sheet resistance in drain diffusion of NMOS. If the sheet resistance is smaller enough, the drain voltage can easily lower energy band in the region G of NMOS to generate the discharging path, which closes to the channel surface. But, the channel surface and gate oxide of NMOS are easily damaged by ESD stress because of the high current density in region G. If the NMOS has a longer clearance of Dcg, the current discharging path can be away from the channel surface of NMOS because of the larger sheet resistance in the drain diffusion. Therefore, the major ESD current can flow into the region S of NMOS, as that shown in Fig. 11(b). From aforementioned discussion, the larger clearance of Dcg can cause larger effective turn-on area in MOSFET to sustain higher ESD current stress.

D. Spacing From Drain Diffusion to Guardring Diffusion

The spacing from drain diffusion to $P+$ guardring diffusion in finger-type layout also has an obvious impact on ESD robustness of NMOS and PMOS devices. This spacing has been illustrated in Figs. 2 and 3 and marked as "Sba." In Fig. 3, the wider spacing Sba contributes a larger base resistance (R_B) to the parasitic lateral n–p–n (p–n–p) BJT in the NMOS (PMOS) device. The parasitic lateral BJT with a larger R_B makes itself to be triggered on more quickly and uniformly under ESD stress. The HBM ESD levels of NMOS and PMOS devices with different Sba spacings but the fixed other layout spacings ($W = 200$ μm, $L = 0.8$ μm, Dcg $= 3$ μm, Scg $= 1$ μm, and Wf $= 50$ μm) are investigated in Fig. 16(a) and (b), respectively. When this Sba spacing is increased from 3 μm to 5 μm, the HBM ESD level

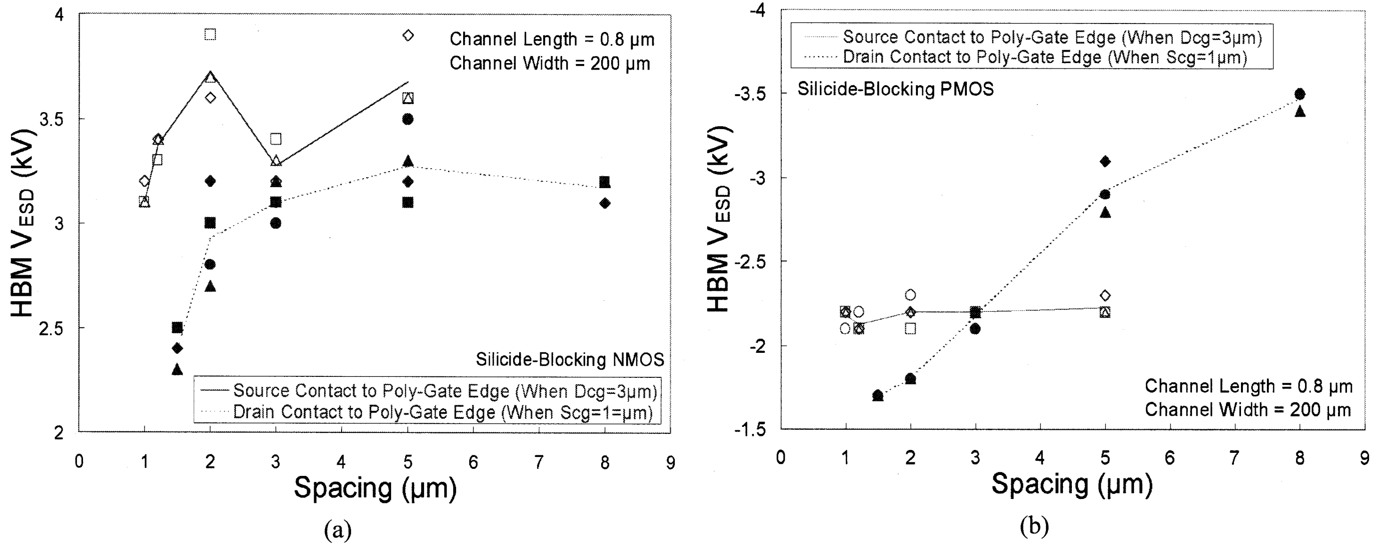

Fig. 15. The dependences of HBM ESD level on the clearance from the drain/source contact to poly-gate edge of silicide-blocking (a) NMOS, and (b) PMOS.

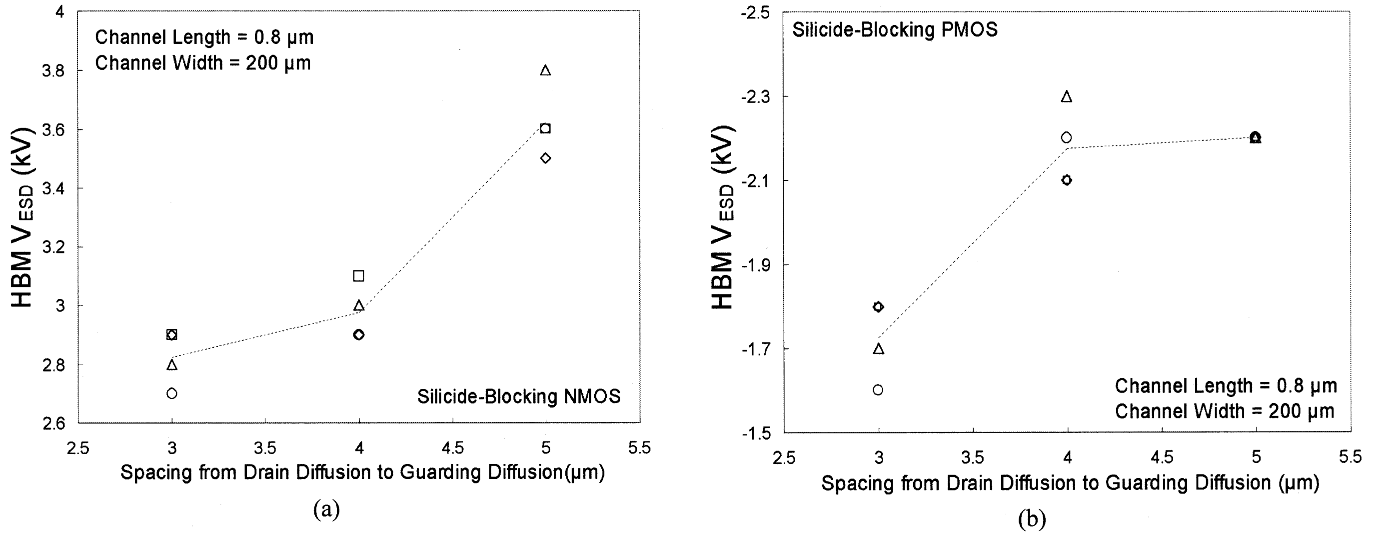

Fig. 16. Dependence of HBM ESD robustness on the Sba spacing of (a) NMOS and (b) PMOS.

of the NMOS (PMOS) is improved from 2.8 to 3.6 kV (from −1.7 kV to −2.2 kV). This investigation confirms the important effect of the layout spacing Sba on ESD robustness. Because the larger Sba can enhance the turn-on uniformity of lateral BJT for all fingers of MOSFET, the MOSFET can sustain higher ESD current.

E. Unit-Finger Width Dependence

In the finger-type layout, a large-dimensional device is traditionally drawn with multiple fingers in a parallel connection. If the Wf of every finger is shorter, more fingers must be used to construct the same device dimension. The large-dimension device with different numbers of unit finger and unit-finger width can cause different ESD performances, even if the device has the same W and L. To verify this issue, both NMOS and PMOS devices with the fixed channel width/length of 200 μm/0.8 μm, but different unit-finger widths are fabricated and investigated by ESD tester. The tested results are shown in Fig. 17(a) and (b). From the experimental results, the HBM ESD level of the NMOS with $W = 200\ \mu$m is deceased from 3 to 2.7 kV, while the NMOS is drawn with the finger number from 2 to 8 in the 0.35-μm silicided CMOS process. On the contrary, the PMOS drawn with four fingers leads to a slight higher ESD robustness.

The MOSFET with different unit-finger width has different geometrical layout area. The different geometrical layout can cause the different turn-on area of parasitic lateral BJT in the MOSFET. In Fig. 5(k), the major turn-on current of parasitic lateral BJT is concentrated in the central region of NMOS. The effective turn-on area ($A_{\text{effective}}$) of parasitic lateral BJT on the drain edge of MOSFET can be approximated as [17]

$$A_{\text{effective}} \approx (\text{Nf} - \alpha) \cdot (\text{Wf} - \beta) \cdot \sqrt{(\gamma \cdot \text{Dcg})^2 + [\delta \cdot (W_D + W_{B'})]^2}, \quad (8)$$

where α is a modified parameter of the finger number, and â is a modified parameter of the unit-finger width in MOSFET. The

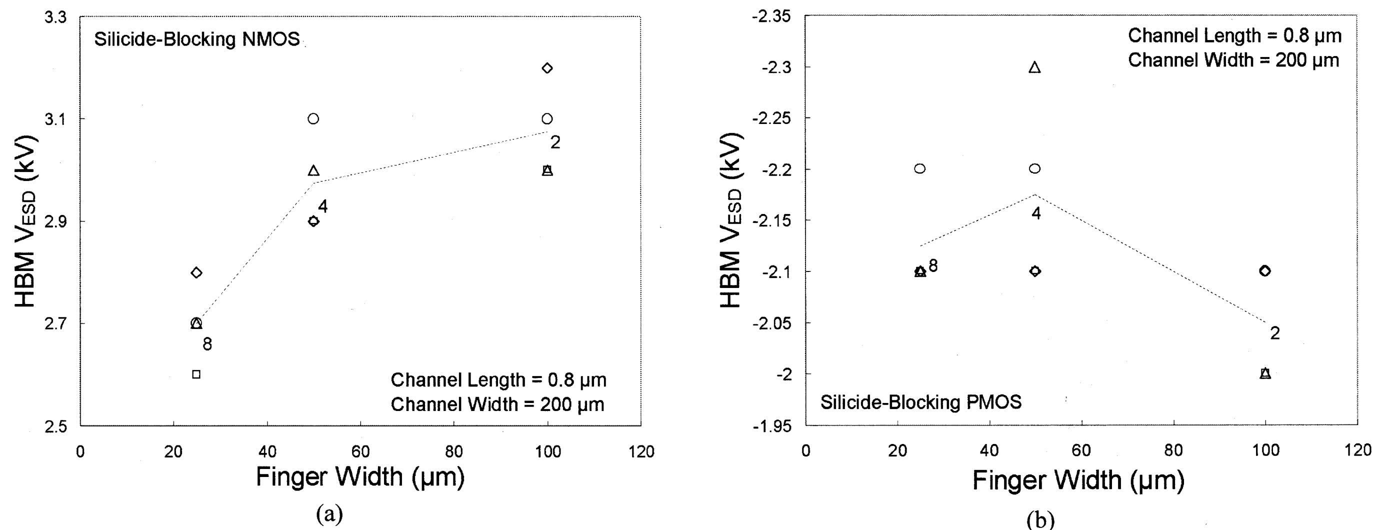

Fig. 17. The dependence of HBM ESD robustness on the finger width and finger number of (a) NMOS, and (b) PMOS, with $W/L = 200$ μm/0.8 μm in the finger-type layout.

TABLE I
THE DEVICE PARAMETERS AND CALCULATED EFFECTIVE TURN-ON AREA OF NMOS AND PMOS UNDER THE SAME TOTAL CHANNEL WIDTH ($W = 200$ μm) IN (8)

α	β	γ	δ	Nf	Wf (μm)	Dcg (μm)	W_D (μm)	$W_{B'}$ (μm)	$A_{effective}$ (μm^2)
NMOS									
0.18	8	0.7	0.4	8	25	3	0.02	0.6	281.11
0.18	8	0.7	0.4	4	50	3	0.02	0.6	339.27
0.18	8	0.7	0.4	2	100	3	0.02	0.6	354.07
PMOS									
0.18	2	0.8	0.1	8	25	3	0.02	0.5	431.77
0.18	2	0.8	0.1	4	50	3	0.02	0.5	440.17
0.18	2	0.8	0.1	2	100	3	0.02	0.5	428.16

γ and δ are weight coefficients of effective turn-on area on the bottom and sideward of drain diffusion in MOSFET. Because those devices with the same total channel width but different unit channel width have the same L and clearance of Dcg, the turn-on position and area per Wf are assumed to be fixed and be constant in the turned-on parasitic lateral BJT of MOSFET. To simply explain the unit-finger width effect, the parameters (α, β, γ, and δ) in (8) can be found with some suitable constants for NMOS or PMOS, which have been listed in Table I. Because the MOSFET with more effective turn-on area ($A_{\text{effective}}$) has larger turn-on volume for the heat dissipation, the larger turn-on area ($A_{\text{effective}}$) of MOSFET in Table I can sustain higher ESD stress. From the calculated effective turn-on areas ($A_{\text{effective}}$) of NMOS and PMOS devices under the same channel width in Table I, their variation completely match to the curve variation in Fig. 17(a) and (b).

IV. CONCLUSION

The dependence of layout spacings on ESD robustness of CMOS devices in silicided CMOS process has been detailedly investigated and discussed. To further explain the current distribution along the NMOS device structure under ESD stress, the energy band diagram is first used in the literature to clearly describe the dependence of ESD robustness on device layout parameters. From the explication of energy band diagrams, MOSFET with a discharging current path near to its channel and a smaller turn-on area of the parasitic lateral BJT often cause a low ESD robustness. Generally, the device with a wider channel width, a larger clearance from drain contact to the poly-gate edge, and a wider spacing from the drain diffusion to the guardring diffusion leads to a higher ESD robustness. When the channel length L of MOSFET with LDD structure is increased, the effective turn-on areas of MOSFET under ESD stress can be increased, and the turned-on region can be moved or extended from the sideward to the bottom of drain/source diffusions in MOSFET. With the analysis on energy band diagrams and experimental investigations, the optimized layout parameters can be found to enhance the turn-on efficiency of the parasitic lateral BJT in MOSFET, and therefore to improve ESD robustness of integrated circuits for manufacturing in deep-submicron CMOS processes.

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